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NTE1721 & NTE1723
Integrated Circuit
Pulse Width Modulator (PWM) Regulator

Description:

The NTE1721 and NTE1723 are pulse width modulator control–circuits designed to offer improved performance and lowered external parts count when implemented for controlling all types of switching power supplies. The no–chip +5.1V reference is trimmed to ±1% and the input common–mode range of the errror amplifier includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the C_T and the Discharge pins. These devices also feature a built–in soft–start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft–start circuitry and the output stages, provided instantaneous turn–off through the PWM latch with pulsed shutdown, as well as soft–start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft–start capacitor when V_{CC} is below nominal. The output stages are totem–pole design capable of sinking and sourcing in excess of 200mA. The output stages of the NTE1721 features NOR logic resulting in a low output for an off state while the NTE1723 utilizes OR logic which gives a high output when off.

Features:

- 8V to 35V Operation
- +5.1V ±1% Trimmed Reference
- 100Hz to 400kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse–by–Pulse Shutdown
- Dual Source/Sink Outputs: ±400mA Peak

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} . . . . . +40V
Collector Supply Voltage, V_C . . . . . +40V
Logic Inputs . . . . . –0.3V to +5.5V
Analog Inputs . . . . . –0.3V to V_{CC}
Output Current, Source or Sink, I_O . . . . . ±500mA
Reference Output Current, I_{ref} 50mA
Oscillator Charging Current 5mA
Power Dissipation (T_A = +25°C), P_D 1000mW
Derate Above 50°C . . . . . 10mW/°C
Power Dissipation (T_C = +25°C), P_D 2000mW
Derate Above 25°C . . . . . 16mW/°C
Operating Junction Temperature, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 100°C/W
Thermal Resistance, Junction–to–Case, R_{thJC} . . . . . 60°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1 Values beyond which damage may occur

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	8.0	–	35.0	V
Collector Supply Voltage	V_C	4.5	–	35.0	V
Output Sink/Source Current Steady State	I_O	0	–	±100	mA
Peak		0	–	±400	mA
Reference Load Current	I_{ref}	0	–	20	mA
Oscillator Frequency Range	f_{osc}	0.1	–	400	kHz
Oscillator Timing Resistor	R_T	2.0	–	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	–	0.2	µF
Deadtime Resistor Range	R_D	0.5	–	–	Ω
Operating Ambient Temperature Range	T_A	0	–	70	°C

Electrical Characteristics: (V_{CC} = +20V, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	V_{ref}	T_J = +25°C	5.0	5.1	5.2	V
Line Regulation	Reg_{line}	+8V ≤ V_{CC} ≤ +35V	–	10	20	mV
Load Regulation	Reg_{load}	0mA ≤ I_L ≤ 20mA	–	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$		–	20	–	mV
Total Output Variation (Includes Line and Load Regulation over Temperature	ΔV_{ref}		4.95	–	5.25	V
Short Circuit Current	I_{SC}	V_{ref} = 0V, T_J = +25°C	–	80	100	mA
Output Noise Voltage	V_n	10Hz ≤ f ≤ 10kHz, T_J = +25°C	–	40	200	μV_{rms}
Long Term Stability	S	T_J = +25°C, Note 2	–	20	50	mV/kHr
Oscillator Section (Tested at f_{osc} = 40kHz, R_T = 3.6kΩ, C_T = 0.001µF, R_D = 0Ω unless otherwise specified)						
Initial Accuracy		T_J = +25°C	–	±2	±6	%
Frequency Stability with Voltage	f_{osc}/V_{CC}	+8V ≤ V_{CC} ≤ +35V	–	±1	±2	%
Frequency Stability with Temperature	f_{osc}/T		–	±3	–	%
Minimum Frequency	f_{min}	R_T = 150kΩ, C_T = 0.2µF	–	50	–	Hz
Maximum Frequency	f_{max}	R_T = 2kΩ, C_T = 1.0nF	400	–	–	kHz
Current Mirror		I_{RT} = 2mA	1.7	2.0	2.2	mA
Clock Amplitude			3.0	3.5	–	V
Clock Width		T_J = +25°C	0.3	0.5	1.0	µs
Sync Threshold			1.2	2.0	2.8	V
Sync Input Current		Sync Voltage = +3.5V	–	1.0	2.5	mA
Error Amplifier Section (V_{CM} = +5.1V)						
Input Offset Voltage	V_{IO}		–	2.0	10.0	mV
Input Bias Current	I_{IB}		–	1.0	10.0	µA

Note 2. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Electrical Characteristics (Cont'd): (V_{CC} = +20V, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier Section (Cont'd) (V_{CM} = +5.1V)						
DC Open Loop Gain	A_{VOL}	$R_L \leq 10M\Omega$	60	75	–	dB
Low Level Output Voltage	V_{OL}		–	0.2	0.5	V
High Level Output Voltage	V_{OH}		3.8	5.6	–	V
Common Mode Rejection Ratio	CMRR	$+1.5V \leq V_{CM} \leq +5.2V$	60	75	–	dB
Power Supply Rejection Ratio	PSRR	$+8V \leq V_{CC} \leq +35V$	50	60	–	dB
PWM Comparator Section						
Minimum Duty Cycle	DC_{min}		–	–	0	%
Maximum Duty Cycle	DC_{max}		45	49	–	%
Input Threshold, Zero Duty Cycle	V_{TH}	f_{osc} = 40kHz, R_T = 3.6kΩ, C_T = 0.01µF, R_D = 0Ω	0.6	0.9	–	V
Input Threshold, Maximum Duty Cycle			–	3.3	3.6	V
Input Bias Current	I_{IB}		–	0.05	1.0	µA
Soft–Start Section						
Soft–Start Current		$V_{shutdown}$ = 0V	25	50	80	µA
Soft–Start Voltage		$V_{shutdown}$ = 2.0V	–	0.4	0.6	V
Shutdown Input Current		$V_{shutdown}$ = 2.5V	–	0.4	1.0	mA
Output Drivers (Each Output, V_{CC} = +20V)						
Output Low Level	V_{OL}	I_{sink} = 20mA	–	0.2	0.4	V
		I_{sink} = 100mA	–	1.0	2.0	V
Output High Level	V_{OH}	I_{sink} = 20mA	18	19	–	V
		I_{sink} = 100mA	17	18	–	V
Under Voltage Lockout	V_{UL}	V8 and V9 = High	6.0	7.0	8.0	V
Collector Leakage	$I_{C(leak)}$	V_C = +35V, Note 3	–	–	200	µA
Rise Time	t_r	C_L = 1.0nF, T_J = +25°C	–	100	600	ns
Fall Time	t_f	C_L = 1.0nF, T_J = +25°C	–	50	300	ns
Shutdown Delay	t_{ds}	V_{DS} = +3V, C_S = 0, T_J = +25°C	–	0.2	0.5	µs
Supply Current	I_{CC}	V_{CC} = +35V	–	14	20	mA

Note 3. Applies to NTE1721 **Only**, due to polarity of output pulses.

Application Information (Shutdown Options)**:**

Since both the compensation and soft–start terminals (Pin9 and Pin8) have current source pull–ups, either can readily accept a pull–down signal which only has to sink a maximum of 100µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin10 performs two functions: the PWM latch is immediately set providing the fastest turn–off signal to the outputs; and a 150µA current sink begins to discharge the external soft–start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft–start capacitor, thus, allowing, for example, a convenient implementation of pulse–by–pulse current limiting. Holding Pin10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn–on upon release.

Pin10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Pin Connection Diagram