MT91610

Programmable Ringing SLIC

Preliminary Information

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Features

- Transformerless 2W to 4W conversion
- Controls battery feed to line
- Programmable line impedance
- Programmable network balance impedance
- Off-hook and dial pulse detection
- Protects against GND short circuit
- Programmable gain
- Programmable constant current mode with constant voltage fold over
- Transformerless balanced ringing with automatic ring trip circuit. No mechanical relay
- Supports low voltage ringing
- Line polarity reversal
- On-hook transmission
- Power down and wake up capability
- Meter pulse injection
- Ground Key detection

Applications

Line interface for:

- PABX
- Intercoms
- Key Telephone Systems
- Control Systems

Package Information	
MT91610AQ	36 Pin QSOP Package
-40°C to +85°C	

Description

The Zarlink MT91610, with an external bipolar driver (Figure 4), provides an interface between a switching system and a subscriber loop. The functions provided by the MT91610 include battery feed, programmable constant current with constant voltage fold over for long loops, 2W to 4W conversion, off-hook and dial pulse detection, direct balance ringing with built in ring tripping, unbalance detection, user definable line and network balance impedance's and gain, and power down and wake up. The device is fabricated as a CMOS circuit in a 36 pin QSOP package.

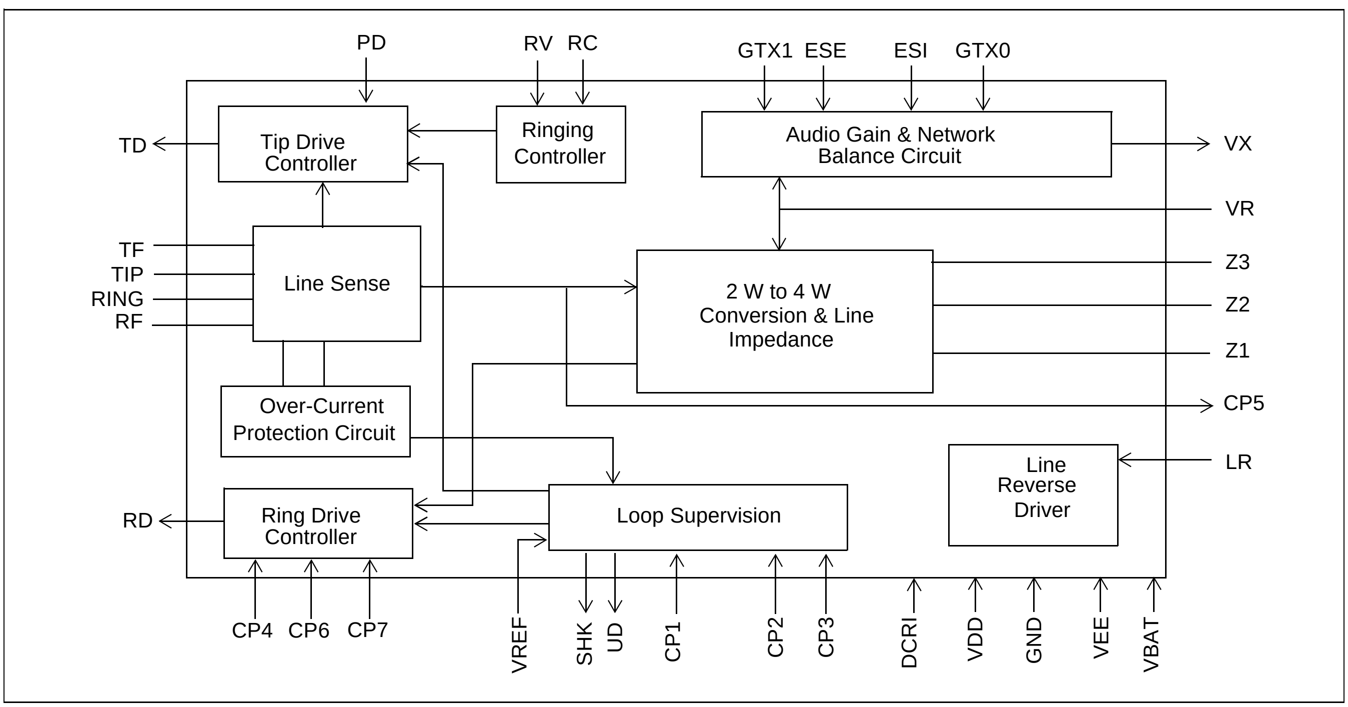


Figure 1 - Functional Block Diagram

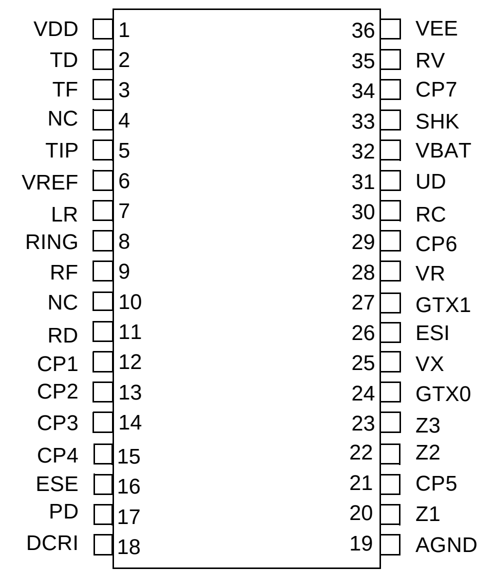


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	VDD	Positive supply rail, +5V.
2	TD	**Tip Drive (Output).** Controls the Tip transistor. Connects 330nF cap to GND.
3	TF	**Tip Feed (Output).** Connects to the Tip transistor and to TIP via the Tip feed resistor.
4	NC	**No Connection.** Left open.
5	Tip	**Tip.** Connects to the TIP lead of the telephone line.
6	VREF	**Reference Voltage (Input).** Used to set the subscribers loop constant current. A 0.1uF cap should be connected between this pin and GND for noise decoupling.
7	LR	**Line Reverse (Input).** This pin should be set to 0V for NORMAL polarity. Setting the pin to +5V reverses the polarity of Tip and Ring.
8	Ring	**Ring.** Connects to the RING lead of the telephone line.
9	RF	**Ring Feed (Output).** Connects to the RING lead via the Ring feed resistor.
10	NC	**No Connection.** Left open.
11	RD	**Ring Drive (Output).** Controls the Ring transistor. Connects 330nF cap to GND.
12	CP1	**CP1**. A 100nF capacitor should be connected between this pin and pin 13.
13	CP2	**CP2.** A 220nF capacitor for loop stability is connected between this pin and pin 14.
14	CP3	**CP3.** A 220nF capacitor for loop stability is connected between this pin and pin 13.
15	CP4	**CP4**. A 100nF cap should be connected between this pin and GND.
16	ESE	**External Signal Enable (Input)**. A logic ’1’ enables the MPI (Meter Pulse Input) to Tip / Ring. This pin should be set to logic ’0’ when not used.
17	PD	**Power Down (Input)**. A logic ’1’ power down the device. This pin should be set to logic ’0’ for normal operation.
18	DCRI	**DC voltage for Ringing Input (Input)** The positive voltage supply for balance ringing. The input DC voltage range is from 0V to +72V.
19	AGND	**Analog Ground.** 4 Wire Ground, normally connected to system ground.

Pin Description (continued)

Pin #	Name	Description
20	Z1	**Line Impedance Node 1**. A resistor of scaled value "k" is connected between Z1 and Z2. This connection can not be left open circuit.
21	CP5	**Line Impedance AC couple.** A 330 nF cap must be connected between this pin and Z1 (pin 20).
22	Z2	**Line Impedance Node 2**. This is the common connection node between Z1 and Z3.
23	Z3	**Line Impedance Node 3**. A resistive or complex network of scaled value "k" is connected between Z3 and Z2. This connection can not be left open circuit.
24	GTX0	**Gain Node 0**. This is the common node between Z3 and VX where resistors are connected to set the 2W to 4W gain.
25	VX	**Transmit Audio**. 4W analog signal from the SLIC.
26	ESI	**External Signal Input**. 12 / 16 KHz signal input.
27	GTX1	**Gain Node 1**. The common node between VR and the audio input from the CODEC or switching network where resistors are fitted to set the 4W to 2W gain.
28	VR	**Receive Audio**. 4W analog signal to the SLIC.
29	CP6	**Ringing Cap.** A 0.47uF cap should be connected between this pin and GND to filter out the ringing signal.
30	RC	**Ringing Control.** An active high (+5V) on this pin will set up the DC feed and gain of the SLIC to apply 20 Hz ringing. When low (0V) set the SLIC in normal constant current mode of operation.
31	UD	**UnBalance Detect.** Logic high (+5V) indicates an offset current between Tip and Ring.
32	VBAT	**VBAT.** The negative battery supply, typically at -48V.
33	SHK	**Switch Hook.** This pin indicates the line state of the subscribers telephone. The output can also be used for dial pulse monitoring. Logic high (+5V) indicates off hook condition.
34	CP7	**Deglitching Cap.** A 33nF should be connected between this pin and GND.
35	RV	**Ringing Voltage.** 20 Hz sinusoidal or square wave AC in for balance ringing.
36	VEE	Negative supply rail, -5V.

Functional Description

Refer to Figure 4 for MT91610 components designation.

The MT91610, with external bipolar transistors, functions as an Analog Line SLIC for use in a 4 Wire switched system. The SLIC performs all of the BORSH functions while interfacing to a CODEC or switching system.

2 Wire to 4 Wire Conversion

The SLIC performs 2 wire to 4 wire conversion by taking the 4 wire signal from an analog switch or voice CODEC, and converting it to a 2 wire differential signal at Tip and Ring. The 2 wire signal applied to tip and ring by the phone is converted to a 4 wire signal, which is the output from the SLIC to the analog switch or voice CODEC.

Gain Control

It is possible to set the Transmit and Receive gains by the selection of the appropriate external components.

The gains can be calculated by the following formulae:

2W to 4W gain

Gain 2 - 4 = 20 Log [R8 / R7]

4W to 2W gain

Gain 4 - 2 = 20 Log [0.891 * [R10 / R9)]

Impedance Programming

The MT91610 allows the designer to set the device's impedance across TIP and RING, (Z_{TR}), and network balance impedance, (Z_{NB}), separately with external low cost components.

The impedance (Z_{TR}) is set by R4, R5, while the network balance, (Z_{NB}), is set by R6, R8, (see Figure 4.)

The network balance impedance should be calculated once the 2W - 4W gain has been set.

Line Impedance

For optimum performance, the characteristic impedance of the line, (Z_o), and the device's impedance across TIP and RING, (Z_{TR}), should match. Therefore:

$Z_o = Z_{TR}$

The relationship between Z_o and the components that set Z_{TR} is given by the formula:

Z_o / (Ra+Rb) = kZ_o / R4
where kZ_o = R5
Ra = Rb

The value of k can be set by the designer to be any value between 500 and 2000. R4 and R5 should be greater than 100kΩ.

Network Balance Impedance

The network balance impedance, (Z_{NB}), will set the transhybrid loss performance for the circuit. The transhybrid loss of the circuit depends on both the 4 - 2 Wire gain and the 2 - 4 Wire gain.

The method of setting the values for R6 (or Z6... it can be a complex impedance) is given as below:

$R6 = R7 * (R9 / R10) * 2.2446689 * (Z_{NB} / Z_{NB} + Z_o)$

Please note that in the case of Z_o not equal to Z_{NB} (the THL compromized case) R6 is a complex impedance. In the general case of Z_o matched to Z_{NB} (the THL optimised case), R6 is just a single resistor.

Loop Supervision

The Loop Supervision circuit monitors the state of the phone line and when the phone goes "Off Hook" the SHK pin goes high to indicate this state. This pin reverts to a low state when the phone goes back "On Hook" or if the loop resistance is too high (>2.3KΩ)

When loop disconnect dialling is being used, SHK pulses to logic 0 indicate the digits being dialled. This output should be debounced.

Constant Current Control & Voltage Fold Over Mode

The SLIC employs a feedback circuit to supply a constant feed current to the line. This design is accomplished by sensing the sum of the voltages across the feed resistors, Ra and Rb, and comparing it to the input reference voltage, Vref, that determines the constant current feed current.

By using a resistive divider network, (Figure 3), it is possible to generate the required voltage to set the loop current, I_{LOOP}. This voltage can be calculated using the following formula:

$$I_{LOOP} = \frac{[V_{DD} * G] * 3}{(Ra + Rb)}$$

where, G = R2 / (R1 + R2)
I_{LOOP} is in Ampere.
R1= 200KΩ

From Figure 3 with Ra = Rb = 100 Ω
For I_{LOOP} = 20mA, R2 = 72.73 KΩ
For I_{LOOP} = 25mA, R2 = 100 KΩ
For I_{LOOP} = 30mA, R2 = 133.33 KΩ

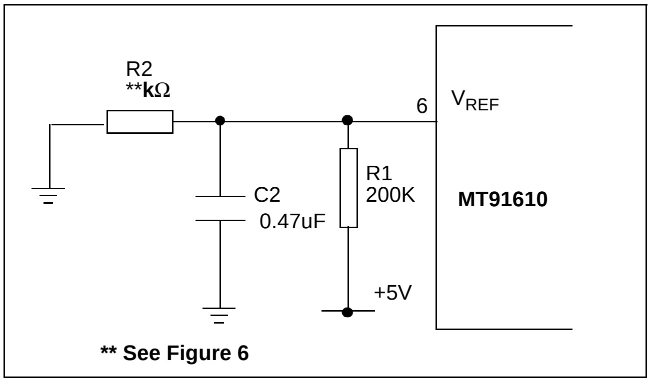


Figure 3 - Loop Setting

For convenience, a graph which plots the value of R2 (KΩ) versus the approximated loop current is shown in Figure 6. This graph implies the SLIC is operating in constant current mode.

As +5V is used as the reference voltage to generate the loop current, any noise on the +5V rail will deteriorate the PSR (Power Supply Rejection) parameter of the SLIC. It is therefore important to decouple +5V to GND. A 0.1uF cap at Vref pin (pin6) is recommended.

The MT91610 operating current mode is recommended to be between 20mA and 30mA. The device will automatically switch to voltage fold over mode should an unexpected long loop situation occur for a given programmed loop current. The lowest operational current should be 16mA with VBAT set at -48V. A typical Operating Current versus Loop Resistance with VBAT at -48V is shown in Figure 7. The actually loop current should settle to within +/- 2 mA of the targeted value.

UD & Line Drivers Overcurrent Protection

The Line Drivers control the external Battery Feed circuit which provide power to the line and allows bi-directional audio transmission.

The loop supervision circuitry provides bias to the line drivers to feed a constant current. Overcurrent protection is done by the following steps:

(A) External bipolar transistors to limit the current of the NPN drivers to 50mA (Figure 5, Q14, Q15, R9, R19).

(B) The local controller should monitor the Unbalance Detection output (UD) for any extended period of assertion (>5 seconds). In such case the controller should power down the device by asserting the PD pin, and poll the device every 5 seconds.

The UD output can be used to support GND START LOOP in a PaBX operation. Reference MSAN-180 for details.

Please note that this UD output should be disregarded and masked out if RC pin is active (ie set to +5V).

Powering Up / Down Sequence

AGND is always connected
Powering Up: +5V, -5V, VBAT
PD to +5V for 100ms; PD to 0V
Powering Down: VBAT, -5V, +5V

Balanced Ringing & Automatic Ring Tripping

Balanced Ringing is applied to the line by setting RC (pin 30) to +5V and connecting the ringing signal (20Hz) to RV (pin 35) as shown in Figure 4. A 1.2Vrms input will give approximately 60Vrms output across Tip and Ring, sufficient for short loop SLIC applications. The SLIC is capable of detecting an Off Hook condition during ringing by filtering out the large A.C. component. A 0.47uF cap should be connected to pin CP6 (pin 29) to form such filter. This filter allows a true Off Hook condition to be monitored at SHK (pin 33). When an Off Hook condition is detected by the SLIC, it will remove the 20Hz AC ringing voltage and revert to constant current mode. The local controller will, however, still need to deselect RC (set it to 0V).

The MT91610 supports short burst of ringing cadence. A deglitching input (CP7) is provided to ensure that the SHK pin is glitch free during the assertion and de-assertion of RC. A 33nF cap should be connected from this pin to GND.

A positive voltage source is required to be connected to the DCRI pin (Figure 5) for normal Ringing operation. The SLIC can perform ringing even with the DCRI input connected to 0V, however, it does require the VBAT to be lower than -48V (ie at -53V or lower) and the 20Hz AC input should be a 2Vrms square wave.

The MT91610 can also be used in applications requiring unbalanced ringing using an external relay. Reference MSAN-180 for details of this and equations related to ringing.

Line Reversal

The MT91610 can deliver Line Reversal, which is required in operation such as ANI, by simply setting LR (pin 7) to +5V. The device transmission parameters will cease during the reversal. The LR (pin 7) should be set to 0V for all normal loop operations.

Power Down And Wake Up

The MT91610 should normally be powered down to conserve energy by setting the PD pin to +5V. The SHK pin will be asserted if the equipment side (2 wire) goes off hook. The local controller should then restore power to the SLIC for normal operations by setting the PD pin to 0V.

Please note that there will be a short break (about 80ms) in the assertion time of SHK due to the time required for the loop to power up and loop current to flow. The local controller should be able to mask out this time.

Meter Pulse Injection

The MT91610 provides a gain path input (ESI) for meter pulse injection and an independent control logic input (ESE) for turning the meter pulse signal on and off.

Gain (meter pulse) = 20 Log [0.891 * (R10 / R11)]
with configuration targeting Z_o = 220 Ω + (820 Ω // 115nF)

Component Selection

Feed Resistors

The selection of feed resistors, Ra and Rb, can significantly affect the performance of the MT91610. The value of 100 Ω is used for both Ra and Rb.

The resistors should have a tolerance of 1% (0.1% matched) and a power rating of 0.5 Watt.

Calculating Component Values

There are five parameters a designer should know before starting the component calculations. These five parameters are:

1) characteristic impedance of the line Z_o
2) network balance impedance Z_{NB}
3) value of the feed resistors (Ra and Rb)
4) 2W to 4W transmit gain
5) 4W to 2W receive gain

The following example will outline a step by step procedure for calculating component values. Given:

Z_o = 600Ω, Z_{NB}= 600Ω, Ra=Rb= 100Ω
Gain 2 - 4 = -6dB, Gain 4 - 2 = -1 dB

Step 1: Gain Setting (R7, R8, R9, R10)

Gain 2 - 4 = 20 Log [R8 / R7]
-6 dB = 20 Log [R8 / R7]
∴ choose R7 = 300kΩ, R8 = 150kΩ.

Gain 4 - 2 = 20 Log [0.891 * [R10 / R9)]
-1 dB = 20 Log [0.891 * [R10/ R9)]
∴ choose R9 = 200kΩ, R10 = 200kΩ.

Step 2: Impedance Matching (R4, R5)

Z_o / (Ra+Rb) = kZ_o / R4,
where kZ_o = R5

Z_o / (Ra+Rb) = kZ_o / R4
600/(100+100) = k*(600)/R4
let k=500
∴ R4= 100kΩ

kZ_o = R5
500*600=R5
∴ R5= 300kΩ

Step 3: Network Balance Impedance (R6)

Optimised Case Z_o = Z_{NB}
R6 = R7 * (R9 / R10) * 2.2446689 * (Z_{NB} / Z_{NB} + Z_o)
R6 = 300kΩ * (1) * 1.1223344
∴ R6= 336.7kΩ

Step 4: The Loop Current (R2)

In order to remain in constant current mode during normal operation, it is necessary that the following equation holds:

{| I * Zt |} V < { | VBAT | - 6*VREF - 2} V
where,
I = Desirable Loop Current
Zt = Ra + Rb + maximum DC loop resistance
VBAT = Battery voltage
VREF= DC voltage at VREF pin

Given the parameters as follows:

Ra = Rb = 100 Ω

Expected maximum loop impedance = 1.6kΩ (including Ra and Rb)

Desirable Loop Current = 20mA

6*VREF=8V

Then | VBAT | (min) = 1600 * 0.020 +10 = 42V

Assume that the VBAT of 42V is available, then read the value of R2 from Figure 6, which is 72kΩ.

Step 5: Calculation Of Non-Clipping Sinusoidal Ringing Voltage At Tip Ring (VTR)

Assume the peak Ringing Current is less than 50mA, the ringing voltage (20Hz) at Tip and Ring is given as:

VTR (rms) = 0.707 * {| VBAT | + VDCRI - (15.6 * VREF)}

VDCRI= Positive DC voltage at DCRI pin

VBAT = Negative Battery voltage

VREF= Positive DC voltage at VREF pin

AC voltage at the RV input pin is therefore

RV (rms)~= VTR (rms) / 50

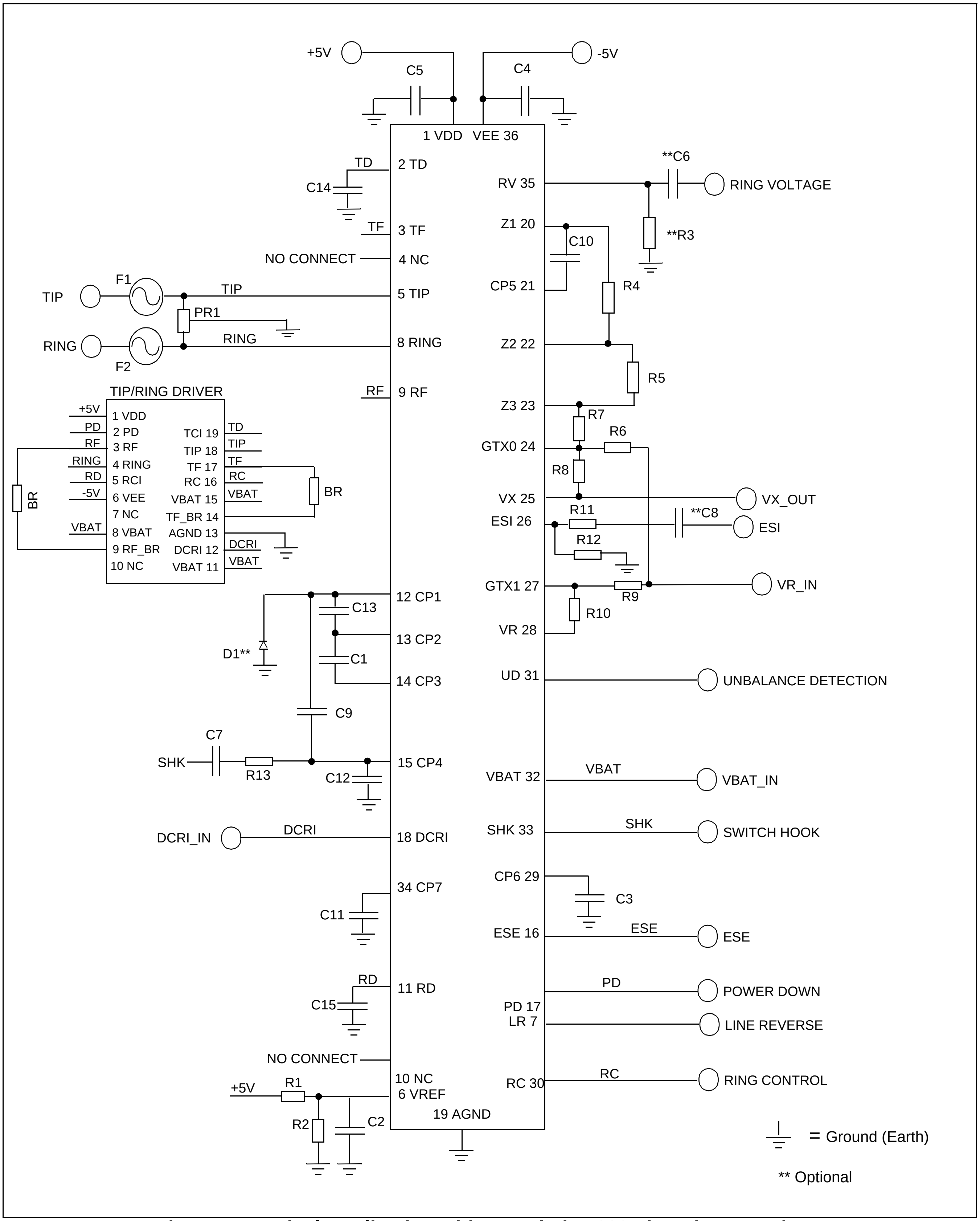


Figure 4 - Typical Application with a Resistive 600 ohm Line Impedance

Component List* for a Typical Application with a Resistive 600Ω Line Impendance - Refer to Figure 4 for component designation and recommended configuration

Resistor Values			
R1	200kΩ	R2	100kΩ (see Figure 6)
R3	200kΩ	R4	100kΩ
R5	300kΩ	R6	336k7Ω
R7	300kΩ	R8	150kΩ
R9	200kΩ	R10	200kΩ
R11	200kΩ	R12	10kΩ
R13	51kΩ		
Capacitor Values			
C1	220nF, 5%	C2	470nF, 5%
C3	470nF, 5%	C4	100nF, 5%
C5	100nF, 5%	C6	4.7uF, 5%
C7	100nF, 5%	C8	100nF, 5%
C9	10nF, 5%	C10	330nF, 5%
C11	33nF, 5%	C12	100nF, 5%
C13	100nF, 5%	C14	330nF, 5%
C15	330nF, 5%		

Note: All resistors are 1/8 W, 1% unless otherwise indicated.
*Assumes $Z_o = Z_{NB}$ = 600Ω, Gain 2 - 4 = -6dB, Gain 4 - 2 = -1dB.

D1 = 1N5819 Schottky Diode (Optional)

PR1 = This device must always be fitted to ensure damages does not occur from inductive loads. For simple applications PR1 can be replaced by a single TVS, such as 1.5KE220C, across tip and ring. For applications requiring lightning and mains cross protection further circuitry will be required and the following protection devices are suggested: P2353AA, P2353AB (Teccor), THBT20011, THBT20012, THBT200S (SGS-Thomson), TISP72290, TISP7360F3D (T.I.)

BR = Raychem TR600-150 or equivalent

F1, F2 = Teccor F1250T Slow-Blow Fuse

Protection Components

Figure 4 shows three possible combinations of protection. Depending on the application, the user can select whether to use a resettable or non-resettable protection scheme.

Method	Slow-Blow Fuse (F1, F2)	Varistor (PR1)	Breaker (BR)
1	in place	in place	short out
2	short out	in place	in place
3	in place	in place	in place

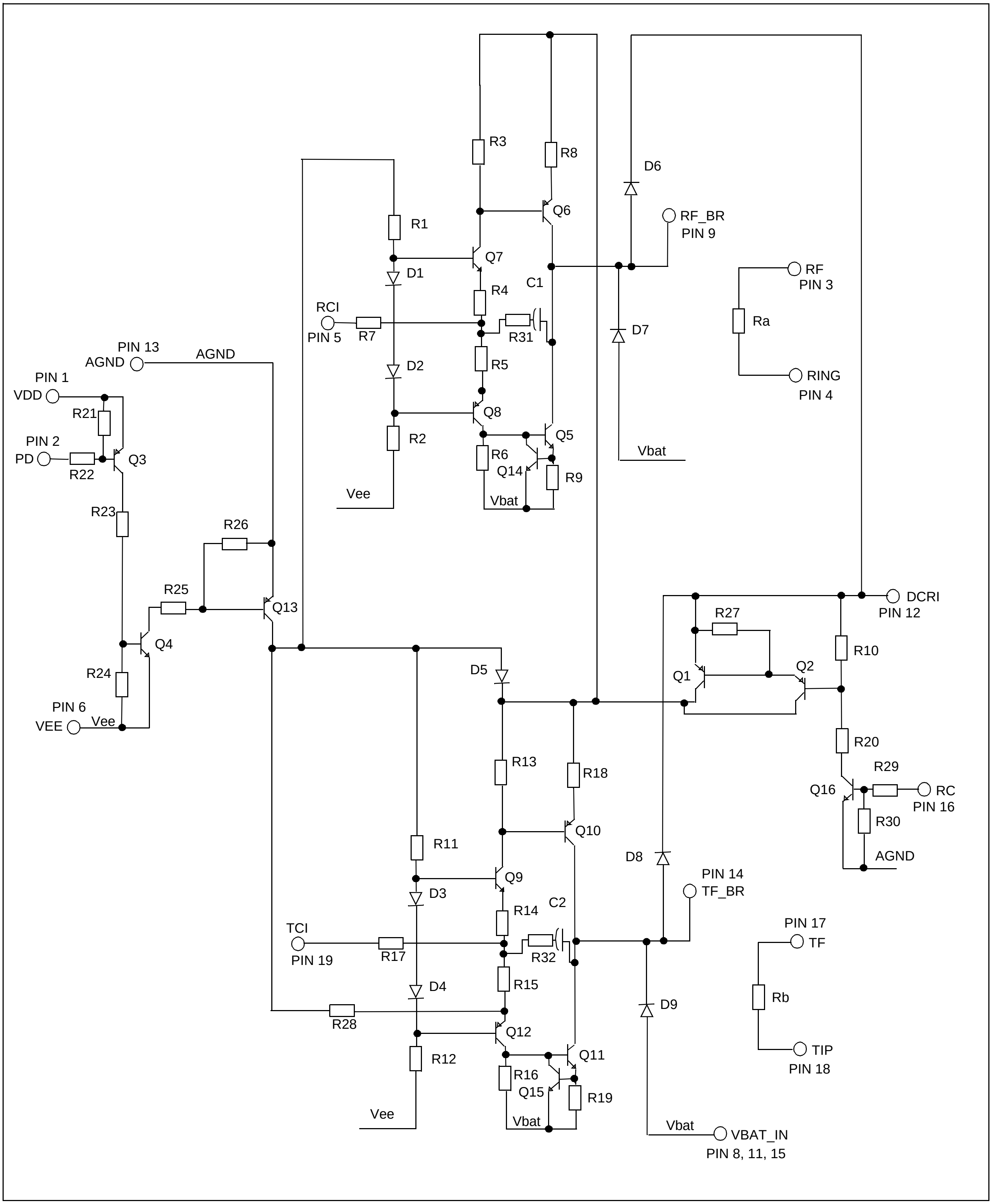


Figure 5 - Line Driver Stage

Component List for the TIP/RING Line Driver - Refer to Figure 5 for component designation and recommended configuration

Resistor Values			
Ra	100Ω %1, 0.1% matched, 0.5W	Rb	100Ω %1, 0.1% matched, 0.5W
R1	2k5Ω	R2	3k6Ω
R3	2k5Ω	R4	470Ω
R5	470Ω	R6	2k5Ω
R7	300Ω	R8	11Ω
R9	11Ω	R10	30kΩ
R11	2k5Ω	R12	3k6Ω
R13	2k5Ω	R14	470Ω
R15	470Ω	R16	2k5Ω
R17	300Ω	R18	11Ω
R19	11Ω	R20	25kΩ, 1/4W
R21	30kΩ	R22	20kΩ
R23	20kΩ	R24	20kΩ
R25	3kΩ	R26	30kΩ
R27	30kΩ	R28	5k1Ω
R29	20kΩ	R30	30kΩ
R31	1kΩ	R32	1kΩ
Capacitor Values			
C1	10nF, 5%	C2	10nF, 5%
Diodes and Transistors			
D1-D5	BAS16 or equivalent	D6-D9	BAW101 or equivalent
Q1	MMBTA92 or equivalent	Q2	MMBTA92 or equivalent
Q3	MMBTA92 or equivalent	Q4	MMBTA42 or equivalent
Q5	PZTA42 or equivalent	Q6	PZTA92 or equivalent
Q7	MMBTA42 or equivalent	Q8	MMBTA92 or equivalent
Q9	MMBTA42 or equivalent	Q10	PZTA92 or equivalent
Q11	PZTA42 or equivalent	Q12	MMBTA92 or equivalent
Q13	MMBTA92 or equivalent	Q14	MMBTA42 or equivalent
Q15	MMBTA42 or equivalent	Q16	MMBTA42 or equivalent

Note: All resistors are 1/8 W, 1% unless otherwise indicated.

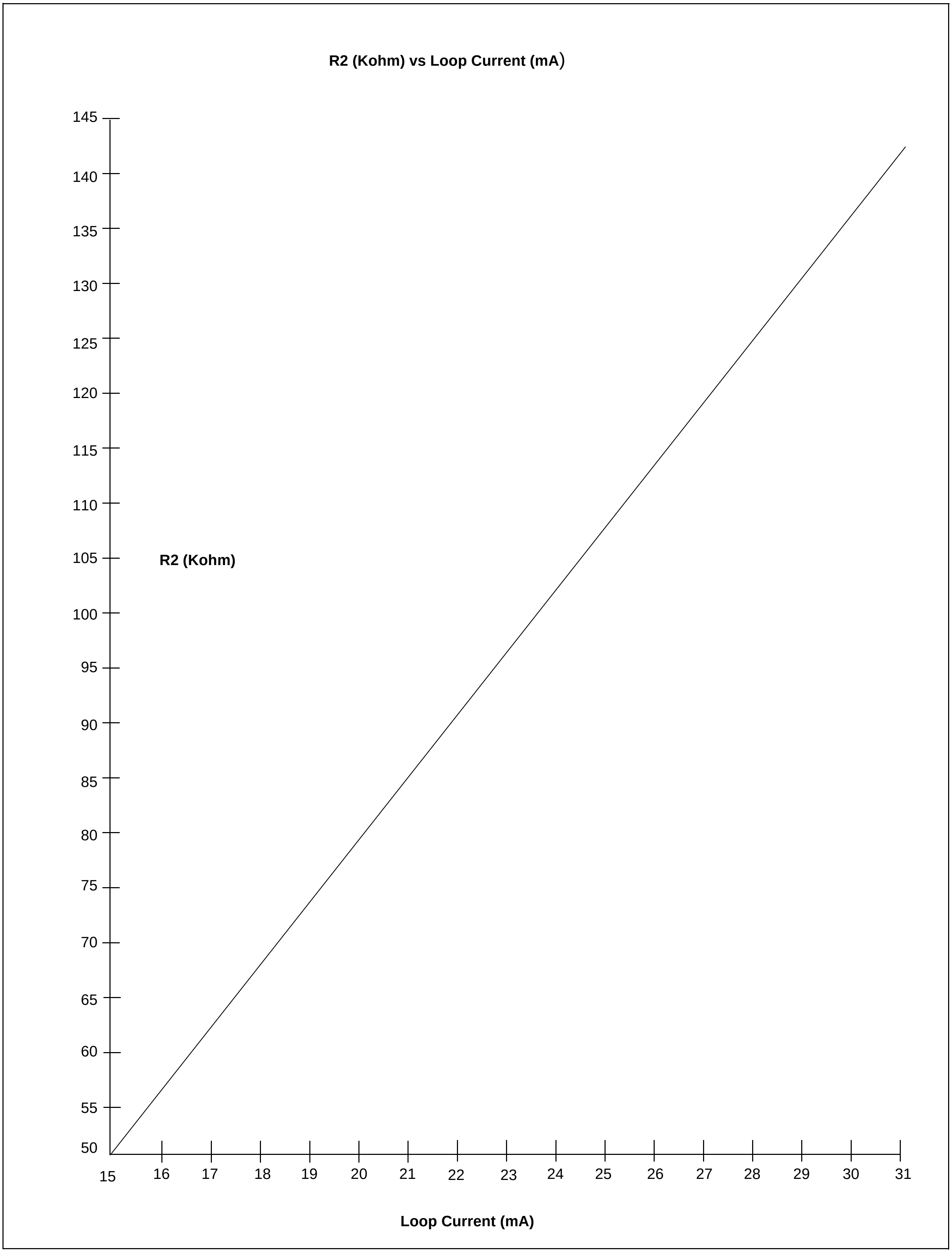


Figure 6 - Approximated R2 (Kohm) Versus Programmed Loop Current (mA) for constant current mode applications.

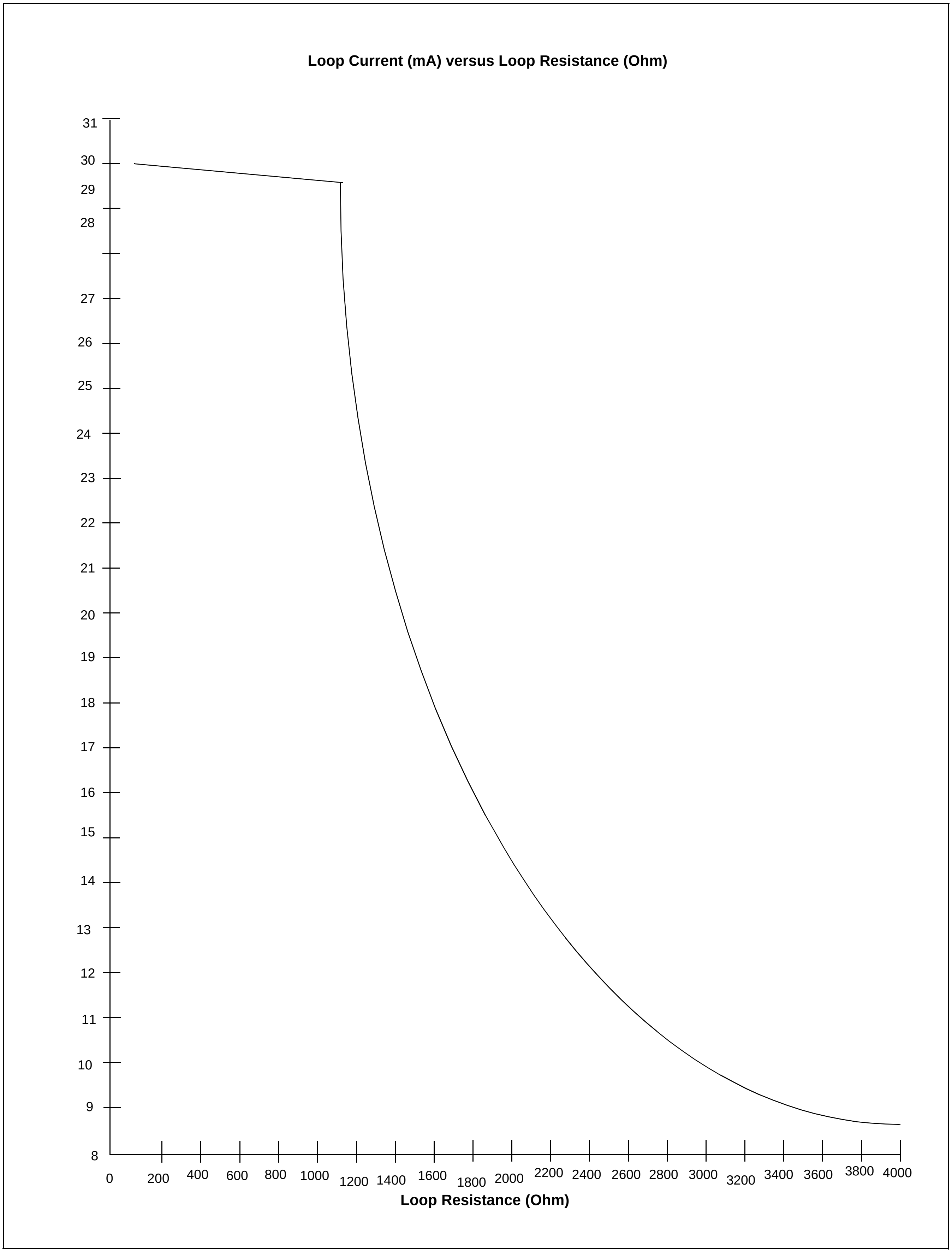


Figure 7 - Loop Current (mA) Versus Loop Resistance (ohm) for Vbat = -48V

Absolute Maximum Ratings*

	Parameter	Sym	Min	Max	Units	Comments
1	DC Supply Voltages	V_{DD} V_{EE} V_{BAT}	-0.3 +0.3 +0.3	+6.5 -6.5 -72	V V V	
2	Ringing Voltage	V_{RING}		100	V_{RMS}	Differentially across Tip & Ring
3	Voltage setting for Loop Current	V_{REF}	0	5	V	Note 1
4	Overvoltage Tip/GND Ring/GND, Tip/Ring	E_E		200	V	MAX 1ms (with power on)
5	Ringing Current	I_{RING}		35	mA	
6	Tip / Ring Ground over-current			50	mA	Note 2
7	Storage Temp	T_{STG}	-65	+150	°C	
8	Package Power Dissipation	P_{DISS}		0.10	W	+85°C max, V_{BAT} = -48V
9	ESD maximum rating			500	V	

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Note 1: Refer to Figure 3 & 6 for appropriate biasing values
Note 2: Tip and Ring drivers to be limited to about 50mA externally (Figure 5). If the UD pin is asserted for longer than 5 seconds, then PD should be asserted to power down the device. The device should then be checked (by de-asserting PD) every 5 seconds.

Recommended Operating Conditions

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Supply Voltages	V_{DD} V_{EE} V_{BAT} DCRI	4.75 -5.25 -72 5	5.00 -5.00 -48	5.25 -4.75 -22 72	V V V V	50mA current capability
2	Ringing Voltage	V_{RING}		60		V_{RMS}	Note 3
3	Ringing Frequency	F_{RING}	16	20	80	Hz	
4	Voltage setting for Loop Current	V_{REF}		1.67		V	I_{LOOP} = 25mA, VBAT = -48V Note 4
5	Operating Temperature	T_O	-40	+25	+85	°C	

‡ Typical Figures are at 25°C with nominal supply voltages and are for design aid only
Note 3: For a 1.2Vrms 20Hz input at RV terminal (Figure 4) and with RC pin set to +5V.
Note 4: Refer to Figure 3 & 6 for biasing values

DC Electrical Characteristics †

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current	I_{DD} I_{EE} I_{BAT}		8 6 28		mA mA mA	PD= 0V V_{BAT}= -48V $I_{BAT} \sim I_{LOOP}$ + 3 mA
2	Supply Current	I_{DD} I_{EE} I_{BAT}		300 300 1.8		uA uA mA	PD = 5V V_{BAT} = -48V
3	Constant Current Line Feed	I_{LOOP}		25		mA	V_{REF}=1.67V
4	Operating Loop Constant Current Mode (including the DC resistance of the Telephone Set)	R_{LOOP}		1600 400		Ω Ω	I_{LOOP} = 20mA V_{BAT} = -48V I_{LOOP} = 20mA V_{BAT} = -22V
5	Off Hook Detection Threshold	S_{HK}		12		mA	
6	RC, LR Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	 4.5		 0.5	 V V	 L_{IL} = -1µA L_{IH} = 1µA
7	PD, ESE Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	 4.5		 0.5	 V V	 L_{IL}= -1µA L_{IH} = 1µA
8	SHK Output Low Voltage Output High Voltage	 V_{OL} V_{OH}	 4.5		 0.5	 V V	 L_{OL} = 7.5mA L_{OH} = -1.5mA
9	UnBalance Detection Threshold	I_{UD}		12		mA	
10	UD Output Low Voltage Output High Voltage	 V_{OL} V_{OH}	 4.5		 0.5		 L_{OL} = 0.25mA L_{OH} = -0.25mA
11	DialPulseDistortion			1		ms	

† Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
‡ Typical Figures are at 25°C with nominal ±5V and are for design aid only.

AC Electrical Characteristics †

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Ring Trip Detect Time	Tt		90	200	mS	
3	Return Loss (2W)	RL	20	30		dB	300Hz to 3400Hz Note 5
4	Transhybrid Loss	THL	20	25		dB	300Hz to 3400Hz Note 5
5	Output Impedance at VX			10		Ω	AC small signal
6	Gain 4 to 2 Wire @ 1kHz		-1.5	-1	-0.5	dB	Note 5
7	Gain Relative to 1kHz			±0.15		dB	300Hz to 3400Hz
8	Gain 2W to VX @ 1kHz		-6.5	-6	-5.5	dB	Note 5
9	Gain Relative to 1kHz			±0.15		dB	300Hz to 3400Hz
10	Longitudinal to Metallic Balance at 2W	LCL	46	55		dB	Input 2Vrms, 1KHz
11	Total Harmonic Distortion @2W @VX	THD		 0.3 0.3	 1.0 1.0	 % %	 1Vrms, 1kHz @ 2W 1Vrms, 1KHz @ VR
12	Common Mode Rejection 2 Wire to Vx	CMR	45	50		dB	Input 2Vrms, 1KHz
13	Idle Channel Noise @2W @VX	NC		 12 12		 dBrnC dBrnC	 Cmessage Filter Fig. 4 Cmessage Filter Fig. 4
14	Power Supply Rejection Ratio at 2W and VX Vdd Vee	PSR		 23 23		 dB dB	 0.1Vp-p @ 1kHz I_{Loop} = 30 mA
15	Line Reversal Recovery Timing	TLRR		30	50	ms	Note 6

†Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡Typical Figures are at 25°C with nominal ±5V and are for design aid only.

Note 5: Refer to Figure 4 & 5 for set up and component values.

Note 6: TLRR is measured from the time when the LR pin is set to 0V (de-selected), to the time when the loop current is within 10% of its programmed steady state value.

Test Circuits

Figures 8,9,10,11,12 are for illustrating the principles involved in making measurements and do not necessarily reflect the actual method used in production testing.

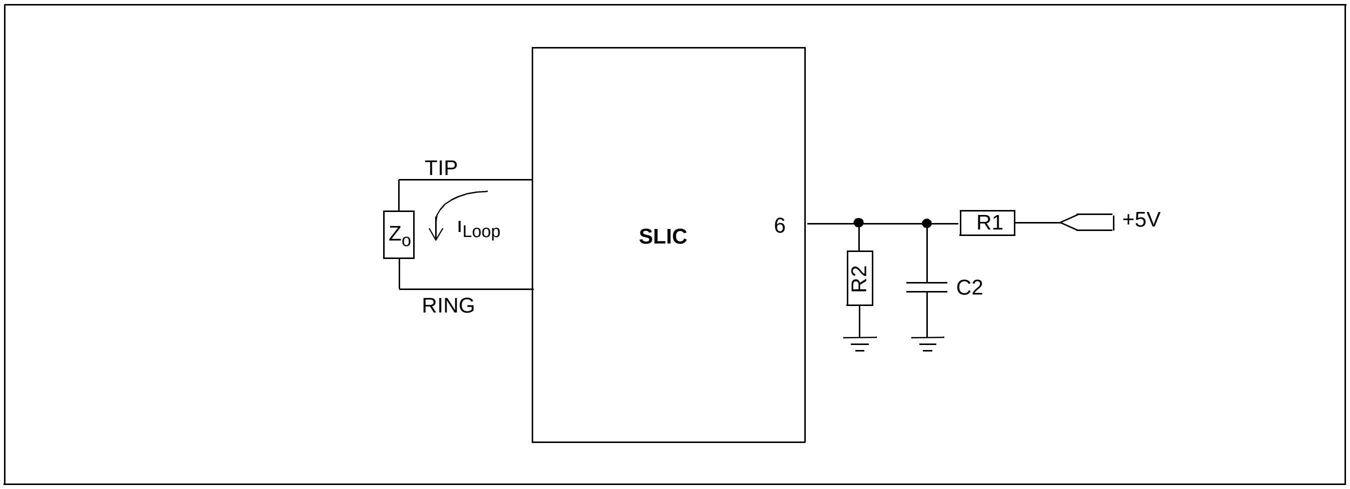


Figure 8 - Loop Current Programming

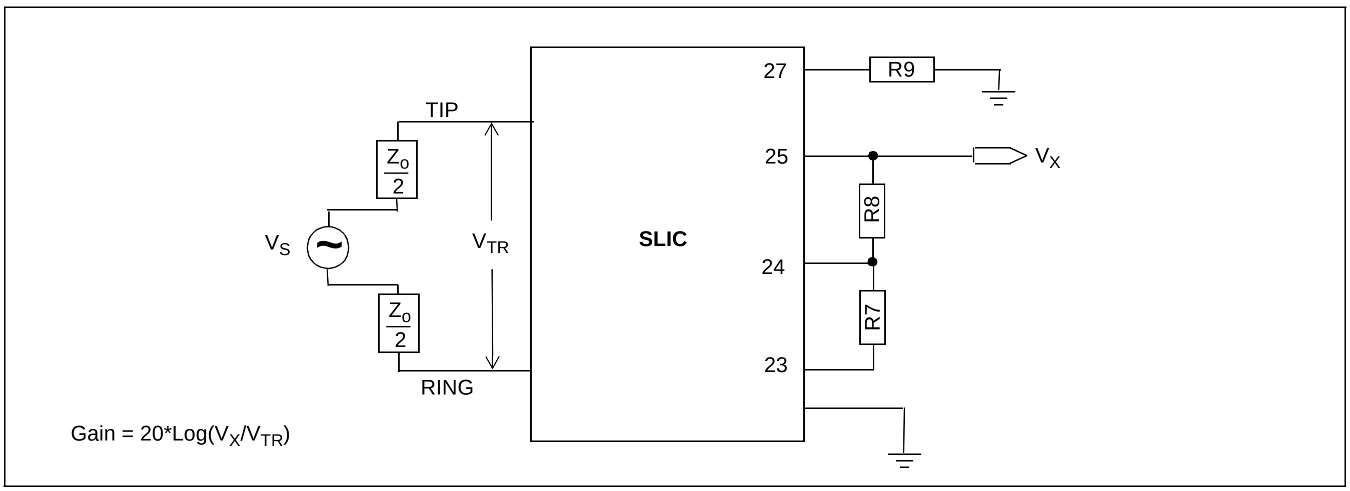


Figure 9 - 2-4 Wire Gain

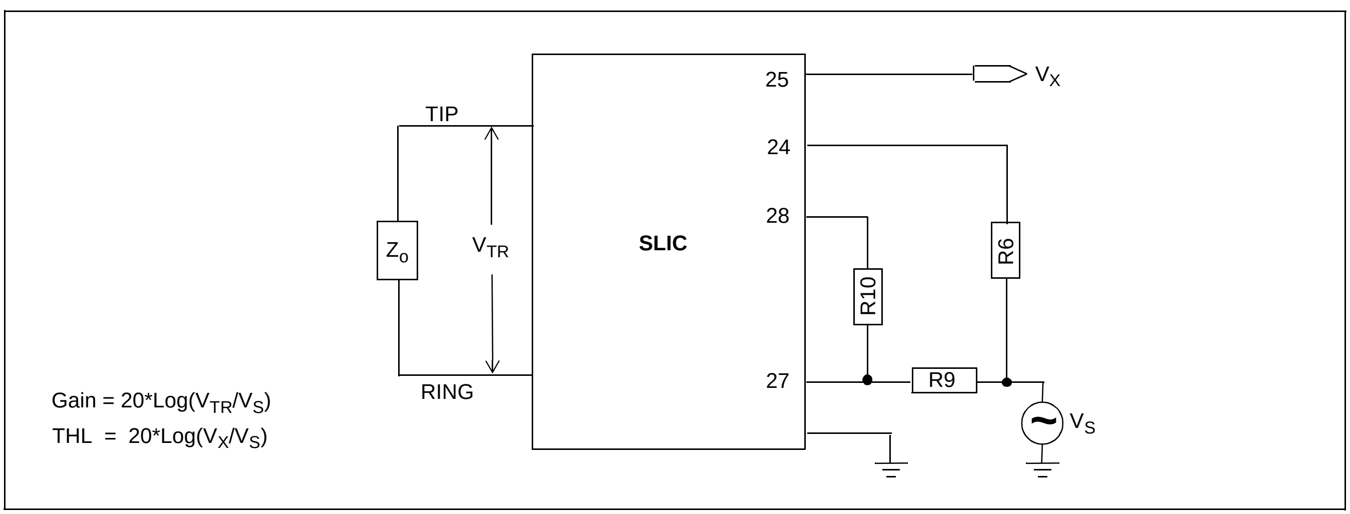


Figure 10 - 4-2 Wire Gain & Transhybrid Loss

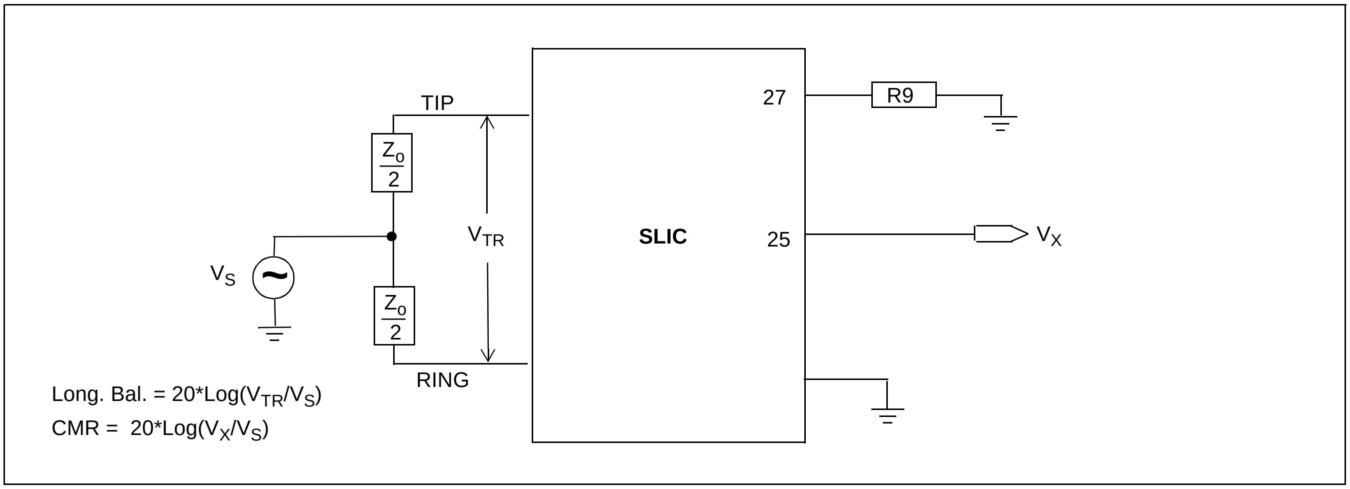


Figure 11 - Longitudinal Balance & CMR

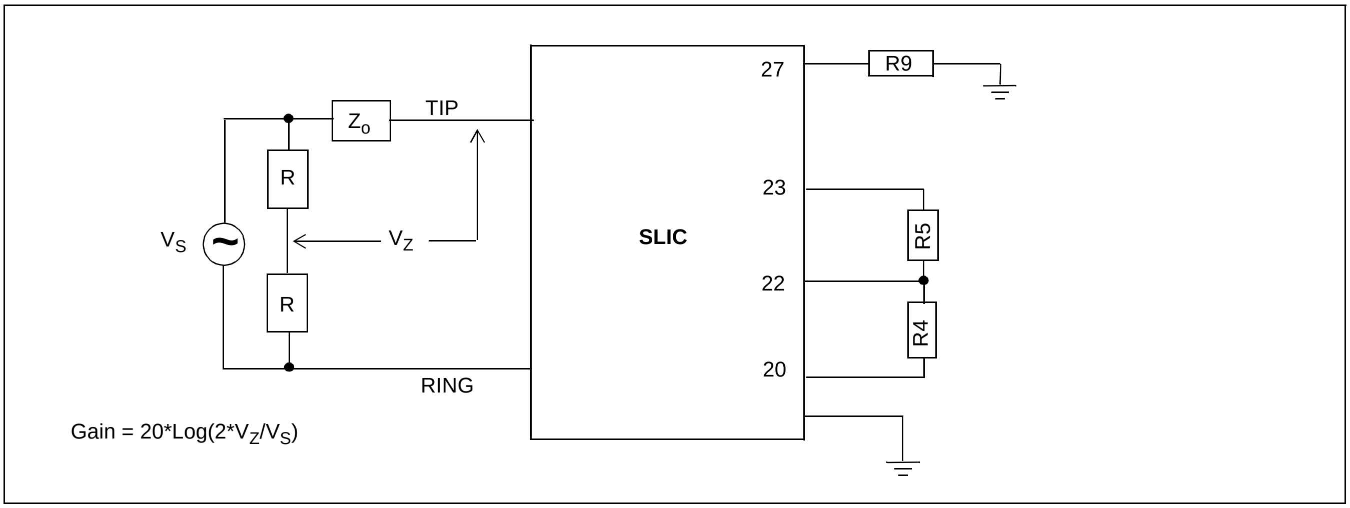
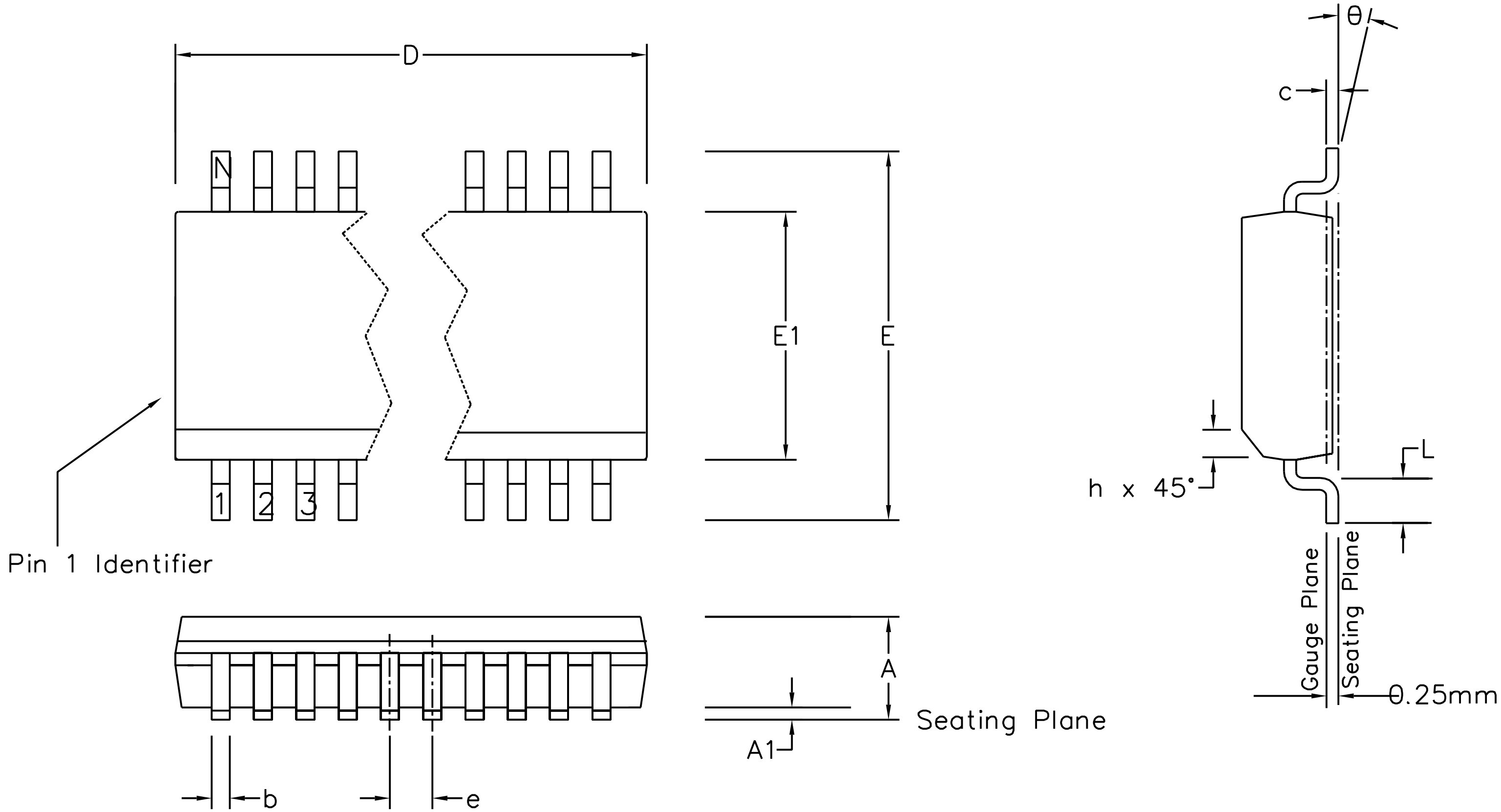


Figure 12 - Return Loss



Symbol	Altern. Dimensions in inches		Control Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.096	0.104	2.44	2.64
A1	0.004	0.012	0.10	0.30
D	0.598	0.612	15.20	15.54
E1	0.291	0.299	7.40	7.60
E	0.398	0.414	10.11	10.51
L	0.016	0.050	0.40	1.27
e	0.0315 BSC.		0.80 BSC.	
b	0.011	0.020	0.28	0.51
c	0.009	0.013	0.23	0.32
θ	0°	8°	0°	8°
h	0.010	0.030	0.25	0.75
	Pin features			
N	36			
NON JEDEC STANDARD DRAWING				

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M – 1982
2. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located at pin 1 position.
3. Controlling dimensions are in millimeters
4. D & E1 do not include mould flash or protrusion. But do include mold mismatch.
5. Dimension E1 does not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
6. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension.
7. Not to Scale

ISSUE	1	2	3	
ACN	6741	207728	212423	
DATE	14MAR95	5NOV99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

NP / N

Package Code DD

Package Outline for
36 lead SSOP
(7.5mm Body Width)

GPD00008

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