R80515
8-bit Microcontroller Megafunction

General Description

The R80515 is a fast, single-chip, 8-bit microcontroller that executes all ASM51 instructions. It has the same instruction set as the 80C31, but executes operations an average of 8 times faster.

The R80515 provides software and hardware interrupts, extra timer features, power management, and Infinion peripherals support. On-chip debugging is an option.

The microcode-free, strictly synchronous design was developed for reuse in ASICs and FPGAs.

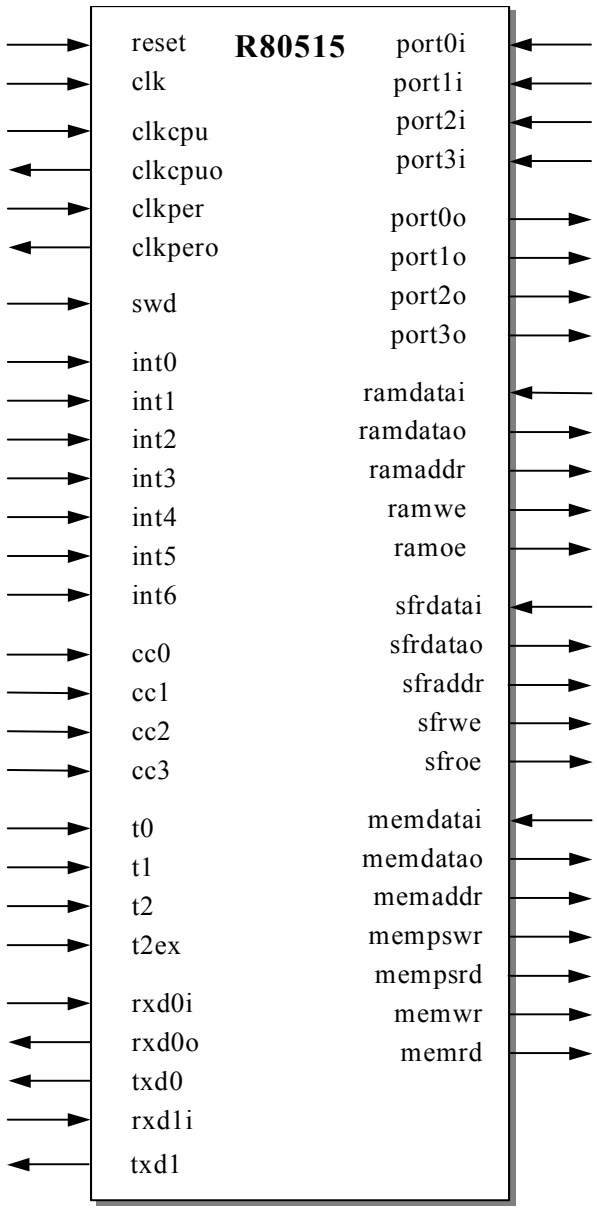
Features

- Single clock per machine cycle
- Reduced instruction cycle time up to 12 times
- 8-bit Control Unit
- 8-bit Arithmetic-Logic Unit
- Multiplication/Division Unit
    - 16 x 16-bit multiplication and division; 32 / 16-bit division
- Four 8-bit Input/Output ports
- Alternate port functions such as external interrupts & serial interface are separated, providing extra port pins when compared with the standard 8051
- Three 16-bit Timer/Counters
- Compare/Capture Unit
- Two Serial Peripheral Interfaces in full duplex mode
- Four priority/thirteen sources Interrupt Controller
- 15-bit Programmable Watchdog Timer
- Internal Data Memory interface can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface
    - Can address up to 64 K bytes of External Program Memory Space
    - Can address up to 64K bytes of External Data Memory Space
    - De-multiplexed address/data bus to allow easy connection to memories
    - Variable length MOVX to access fast/slow RAM or peripherals
    - Variable length code fetch and MOVC to access fast/slow program memory
    - Dual data pointer for fast data block transfers
- Special Function Registers interface: serves up to 74 external registers
- Power Management Unit
- Optional JTAG debugging

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Symbol



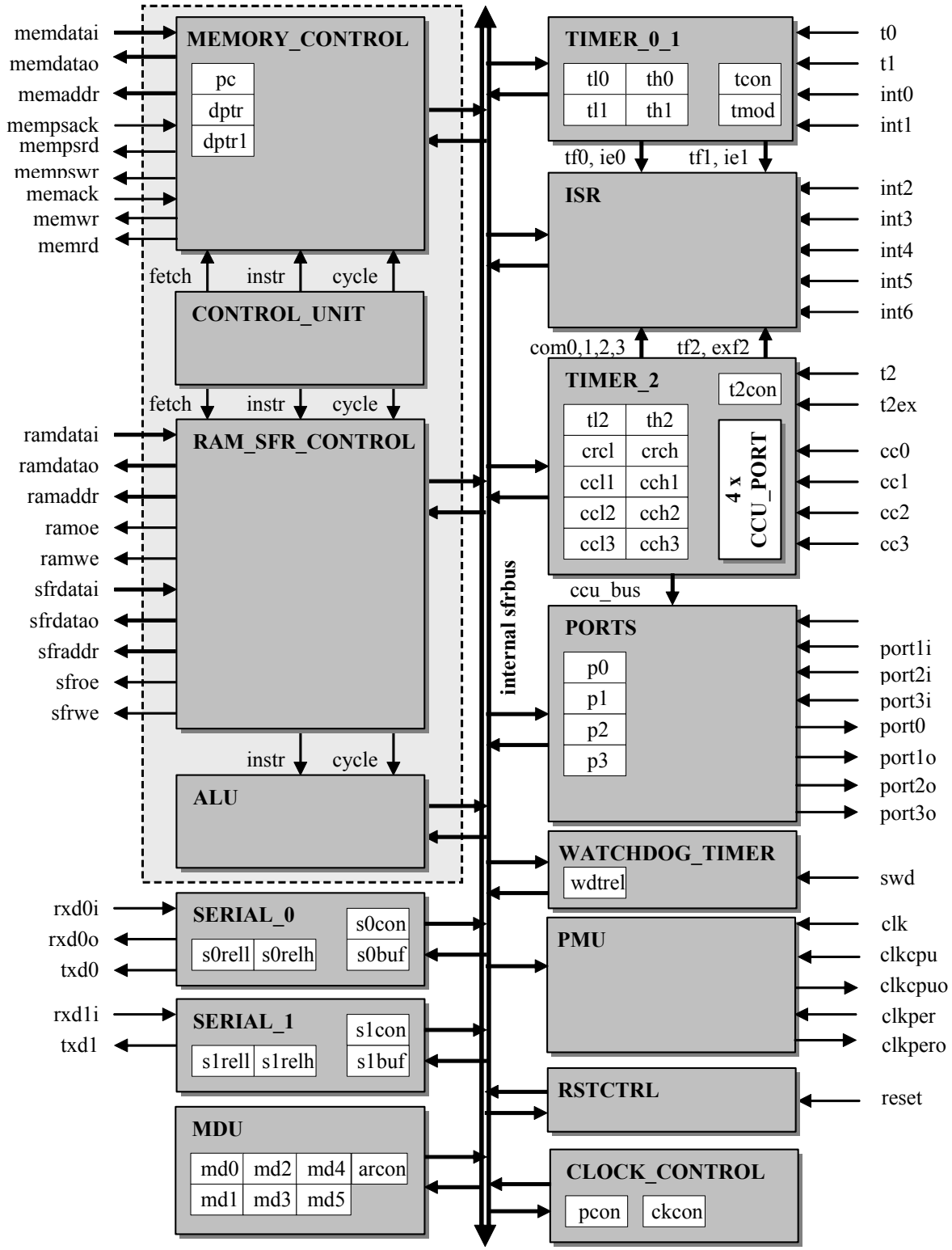
Pin Description

Name	Type	Polarity/ Bus Size	Description
port0i port0o	In Out	8 8	**Port 0** 8-bit bi-directional I/O port with separated inputs and outputs
port1i port1o	In Out	8 8	**Port 1** 8-bit bi-directional I/O port with separated inputs and outputs
port2i port2o	In Out	8 8	**Port 2** 8-bit bi-directional I/O port with separated inputs and outputs
port3i port3o	In Out	8 8	**Port 3** 8-bit bi-directional I/O port with separated inputs and outputs
clk	In	Rising	**Clock** A pulse for internal clock counters and all synchronous circuits
reset	In	High	**Hardware reset** Resets the device when this pin is held high for two clock cycles while the oscillator is running
clkcpu	In	Rising	**Engine clock** A pulse for internal circuits that are stopped when the R80515 is in the IDLE or STOP mode
clkcpuo	Out	Rising	**Engine clock output** Is the gated clk clock. clkcpuo stays low when the R80515 enters into IDLE or STOP mode. The clkcpuo is dedicated to off-core connection to the clkcpu input
clkper	In	Rising	**Peripheral clock** A pulse for internal circuits that are stopped when the R80515 is in STOP mode
clkpero	Out	Rising	**Peripheral clock output** is the gated clk clock. clkpero stays low when the R80515 enters into STOP mode. The clkpero is dedicated to off-core connection to the clkper input

Name	Type	Polarity/ Bus Size	Description
swd	In	High	**Start Watchdog Timer** A high on this pin during reset starts the watchdog timer immediately after reset is released
			External Interrupts
into	In	Low/Falling	External interrupt 0
int1	In	Low/Falling	External interrupt 1
int2	In	Fall./Rising	External interrupt 2
int3	In	Fall./Rising	External interrupt 3
int4	In	Rising	External interrupt 4
int5	In	Rising	External interrupt 5
int6	In	Rising	External interrupt 6
			Compare/Capture
cco	In	High	Compare/Capture 0
cc1	In	High	Compare/Capture 1
cc2	In	High	Compare/Capture 2
cc3	In	High	Compare/Capture 3
			Serial 0 interface
rxd0i	In	-	Serial 0 receive data
rxd0o	Out	-	Serial 0 transmit data
txd0	Out	-	Serial 0 transmit data or receive clock in mode 0
			Serial 1 interface
rxd1i	In	-	Serial 1 receive data
rxd1o	Out	-	Serial 1 transmit data
			Timer inputs
t0	In	Falling	Timer 0 external input
t1	In	Falling	Timer 1 external input
t2	In	Falling	Timer 2 external input
t2ex	In	Falling	Timer 2 capture trigger
			External Memory interface
memdatai	In	8	Memory data input
memdatao	Out	8	Memory data output
memaddr	Out	16	Memory address
mempswr	Out	High	Program store write enable
mempsrd	Out	High	Program store read enable
memwr	Out	High	Data Memory write enable
memrd	Out	High	Data Memory read enable
			Internal Data Memory interface
ramdatai	In	8	Data bus input
ramdatao	Out	8	Data bus output
ramaddr	Out	8	Data file address
ramwe	Out	High	Data file write enable
ramoe	Out	High	Data file output enable

Name	Type	Polarity/ Bus Size	Description
			External Special Function Registers interface
sfrdatai	I	8	SFR data bus input
sfrdatao	O	8	SFR data bus output
sfraddr	O	7	SFR address
sfrwe	O	High	SFR write enable
sfroe	O	High	SFR output enable

Block Diagram



Verification Methods

The R80515 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 and Siemens SAB80C537 chips, and the results were compared with the core's simulation outputs.

Device Utilization & Performance

Supported Family	Device Tested	Utilization			Performance
		LEs	Memory	Memory bits	F_{max}
Cyclone	EP1C4-6	3696	3 M4K	10,240	38 MHz
Stratix	EP1S10-5	3726	3 M4K	10,752	39 MHz
Stratix-II	EP2S5-3	3115	3 M4K	10,752	51 MHz

Notes:

1. Optimized for speed
2. Implemented with 256 bytes of RAM and 1KB of ROM

Deliverables

- VHDL or Verilog HDL source code
- Post-synthesis EDIF netlist (netlist license)
- Testbench (self-checking)
- Vectors for testing the core
- Place & route scripts (netlist license)
- Simulation script
- Synthesis script
- Documentation

Contact Information

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This megafunction developed by the processor experts at Evatronix SA