PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843256

FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER W/INTEGRATED FANOUT BUFFER

GENERAL DESCRIPTION

The ICS843256 is a Crystal-to-3.3V LVPECL Clock Synthesizer/Fanout Buffer designed for Fibre Channel and Gigabit Ethernet applications and is a member of the HiperClockS™ family of High Performance Clock Solutions from ICS. The output frequency can be set using the frequency select pins and a 25MHz crystal for Ethernet frequencies, or a 19.44MHz crystal for SONET. The low phase noise characteristics of the ICS843256 make it an ideal clock for these demanding applications.

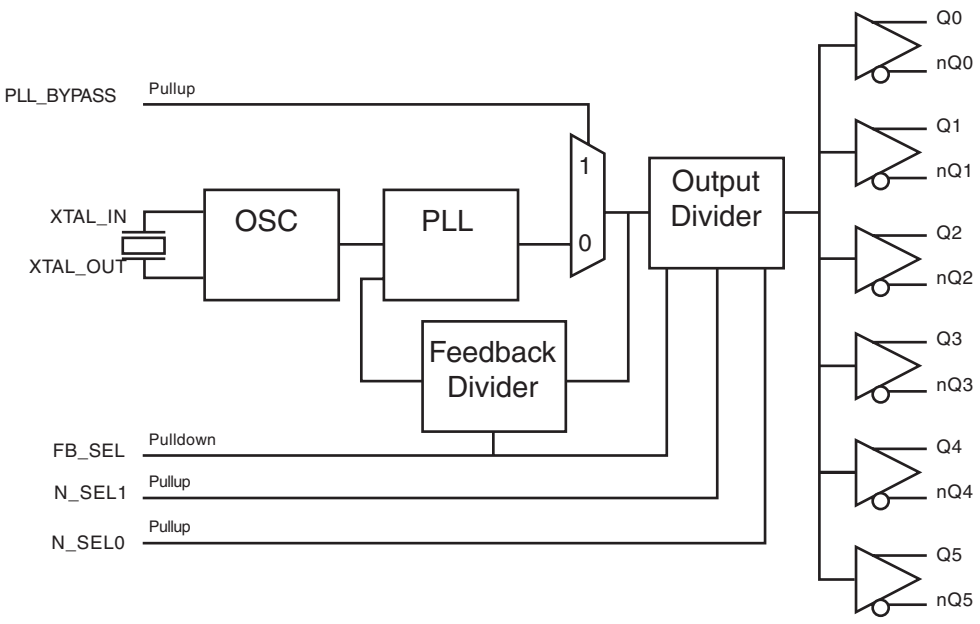
FEATURES

- Six LVPECL outputs
- Crystal oscillator interface
- Output frequency range: 53.125MHz to 333.3333MHz
- Crystal input frequency range: 25MHz to 33.333MHz
- RMS phase jitter at 125MHz, using a 25MHz crystal (1.875MHz to 20MHz): 0.33ps (typical)
- Full 3.3V or 3.3V core, 2.5V output supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

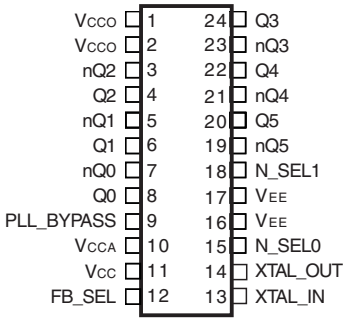
SELECT FUNCTION TABLE

Inputs			Function		
FB_SEL	N_SEL1	N_SEL0	M Divide	N Divide	M/N
0	0	0	25	1	25
0	0	1	25	2	12.5
0	1	0	25	4	6.25
0	1	1	25	5	5
1	0	0	32	1	32
1	0	1	32	2	16
1	1	0	32	4	8
1	1	1	32	8	4

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS843256

24-Lead, 300-MIL SOIC
7.5mm x 15.33mm x 2.3mm body package
M Package
Top View

24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm body package
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	V_{CCO}	Power		Output supply pins.
3, 4	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
5, 6	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
7, 8	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
9	PLL_BYPASS	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When LOW, selects PLL. When HIGH, selects XTAL_IN, XTAL_OUT. LVCMOS / LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
12	FB_SEL	Input	Pulldown	Feedback frequency select pin. LVCMOS/LVTTL interface levels.
13, 14	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
15, 18	N_SEL0 N_SEL1	Input	Pullup	Output frequency select pin. LVCMOS/LVTTL interface levels.
16, 17	V_{EE}			Negative supply pin.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. CRYSTAL FUNCTION TABLE

Inputs				Function			
XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	M	VCO (MHz)	N	Output (MHz)
20	0	0	0	25	500	1	500
20	0	0	1	25	500	2	250
20	0	1	0	25	500	4	125
20	0	1	1	25	500	5	100
21.25	0	1	1	25	531.25	5	106.25
24	0	0	0	25	600	1	600
24	0	0	1	25	600	2	300
24	0	1	0	25	600	4	150
24	0	1	1	25	600	5	120
25	0	0	0	25	625	1	625
25	0	0	1	25	625	2	312.5
25	0	1	0	25	625	4	156.25
25	0	1	1	25	625	5	125
25.5	0	1	0	25	637.5	4	159.375
15.625	1	1	1	32	500	8	62.5
18.5625	1	1	1	32	594	8	74.25
18.75	1	0	0	32	600	1	600
18.75	1	0	1	32	600	2	300
18.75	1	1	0	32	600	4	150
18.75	1	1	1	32	600	8	75
19.44	1	0	0	32	622.08	1	622.08
19.44	1	0	1	32	622.08	2	311.04
19.44	1	1	0	32	622.08	4	155.52
19.44	1	1	1	32	622.08	8	77.76
19.53125	1	0	0	32	625	1	625
19.53125	1	0	1	32	625	2	312.5
19.53125	1	1	0	32	625	4	156.25
19.53125	1	1	1	32	625	8	78.125
20	1	1	1	32	640	8	80

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
24 Lead SOIC	50°C/W (0 lfpm)
24 Lead TSSOP	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			TBD		mA
I_{CCA}	Analog Supply Current			TBD		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			TBD		mA
I_{CCA}	Analog Supply Current			TBD		mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $V_{CCO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL	$V_{CC} = V_{IN} = 3.465V$			150	µA
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	FB_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		15.625		25.5	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		333.33	MHz
*t*jit(Ø)	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.33		ps
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

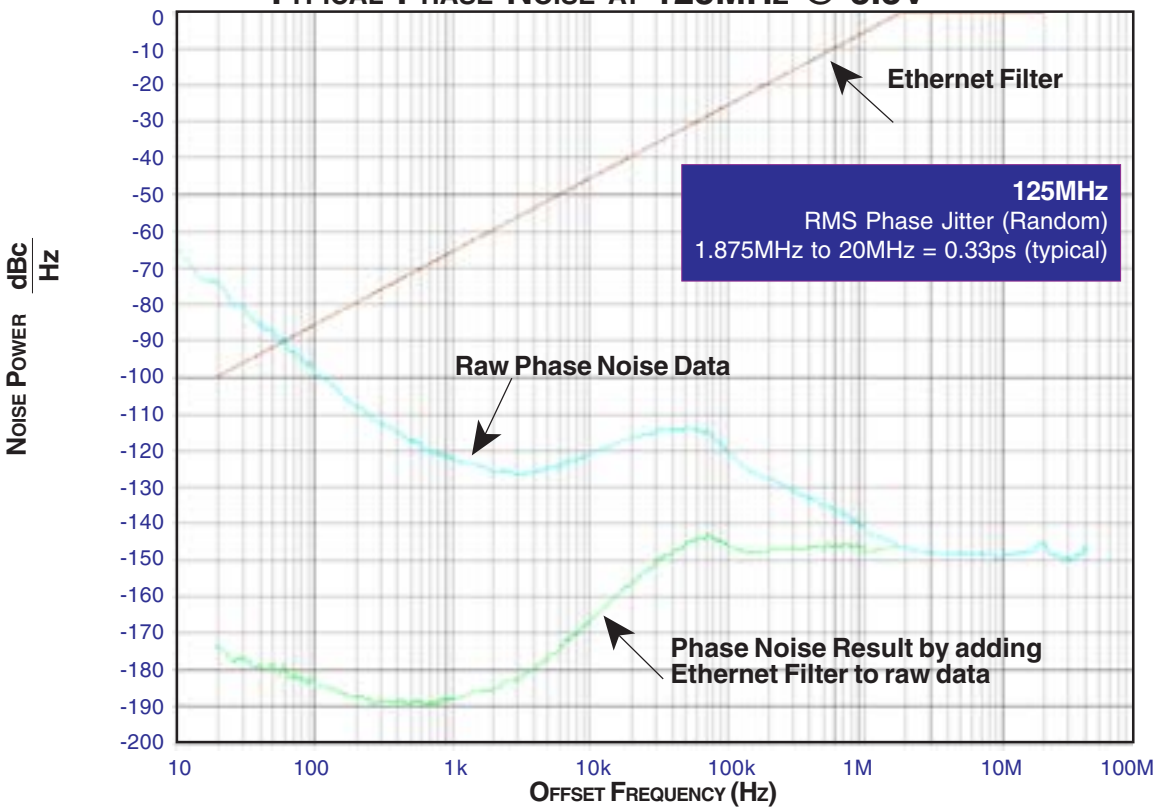
See Parameter Measurement Information section.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

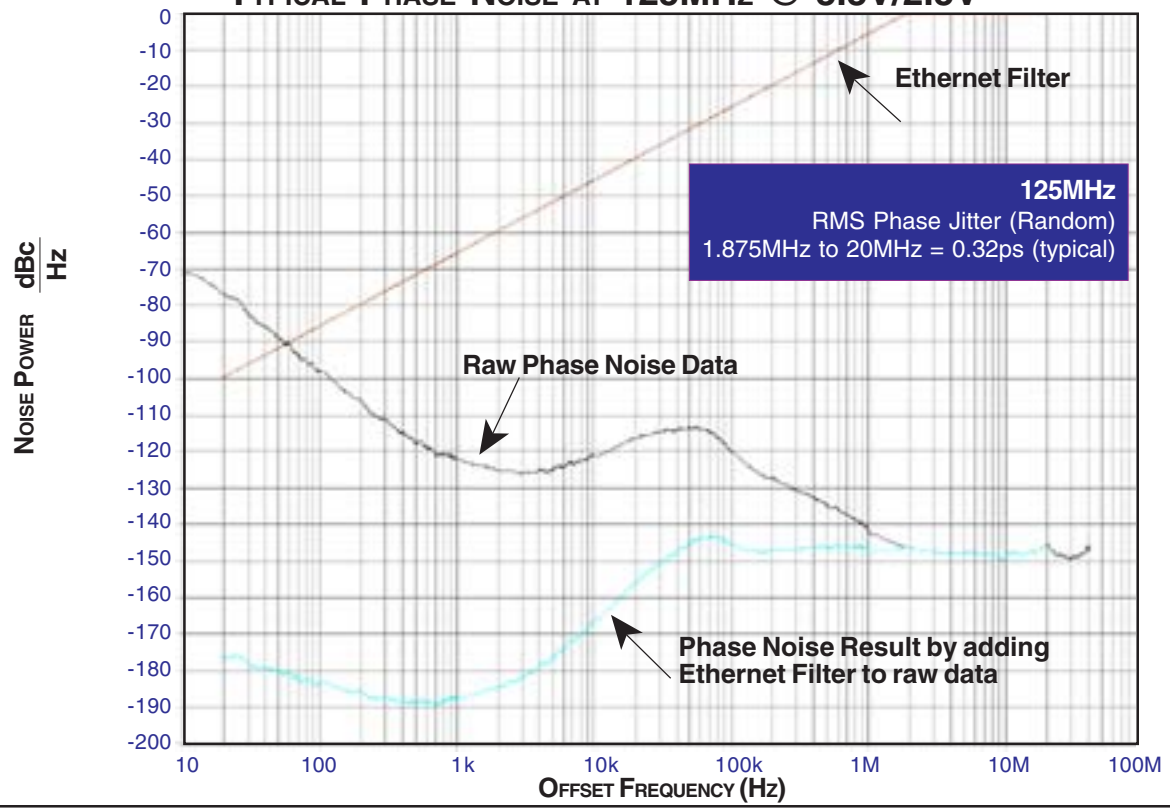
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		53.125		333.33	MHz
*t*jit(Ø)	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.32		ps
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

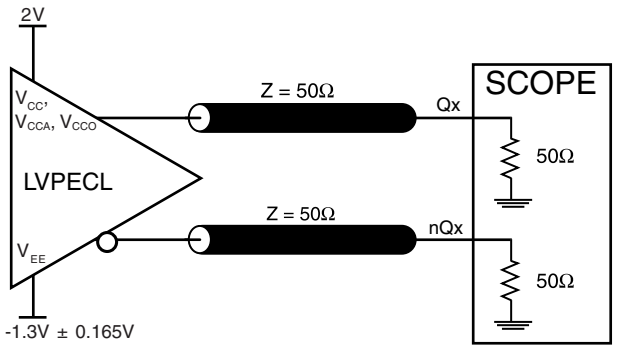
TYPICAL PHASE NOISE AT 125MHZ @ 3.3V



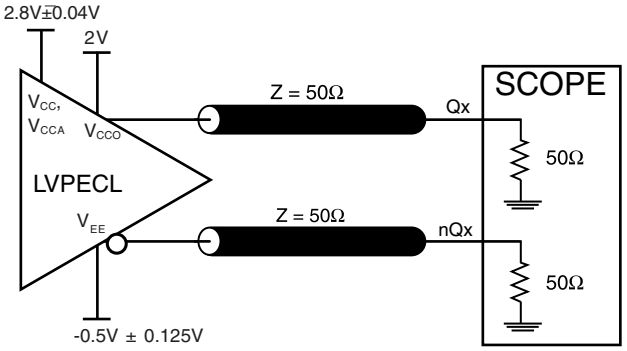
TYPICAL PHASE NOISE AT 125MHZ @ 3.3V/2.5V



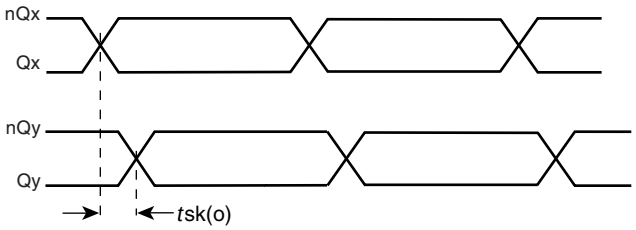
PARAMETER MEASUREMENT INFORMATION



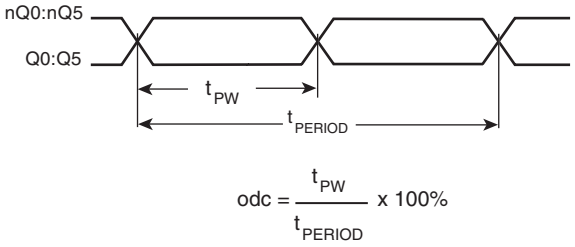
3.3V OUTPUT LOAD AC TEST CIRCUIT



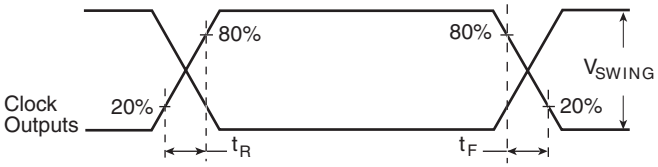
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843256 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

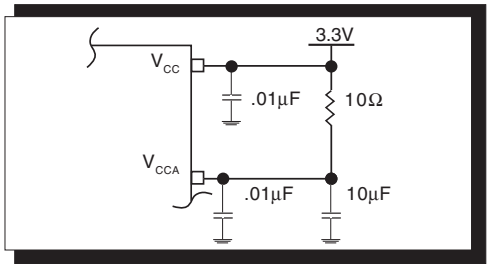


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843256 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

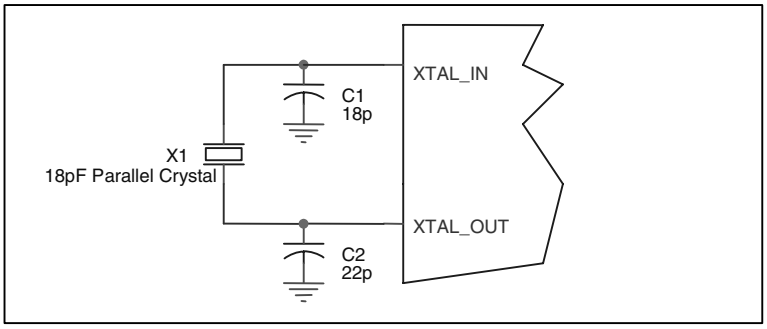


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

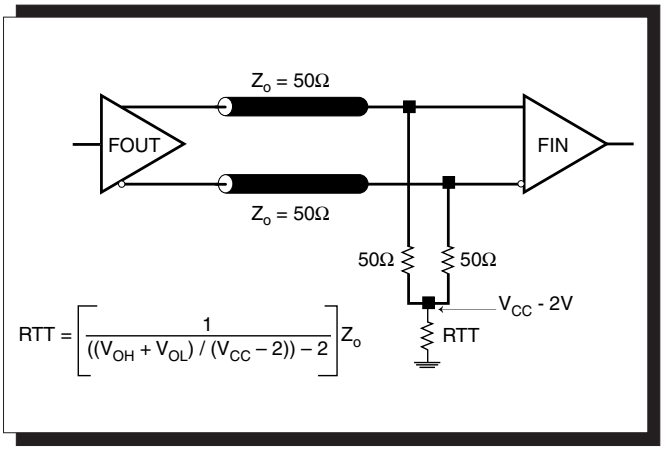


FIGURE 3A. LVPECL OUTPUT TERMINATION

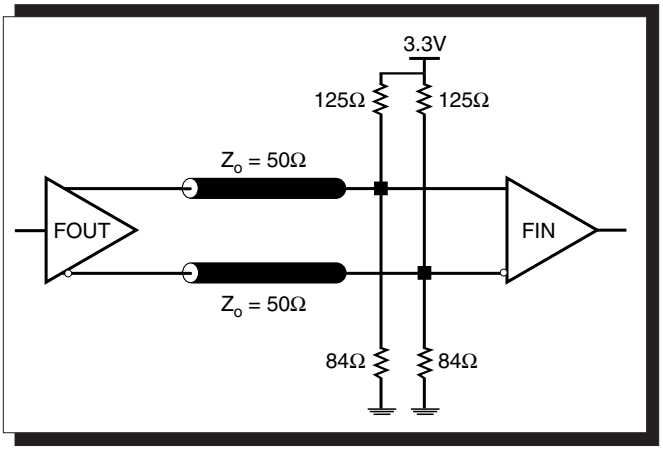


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

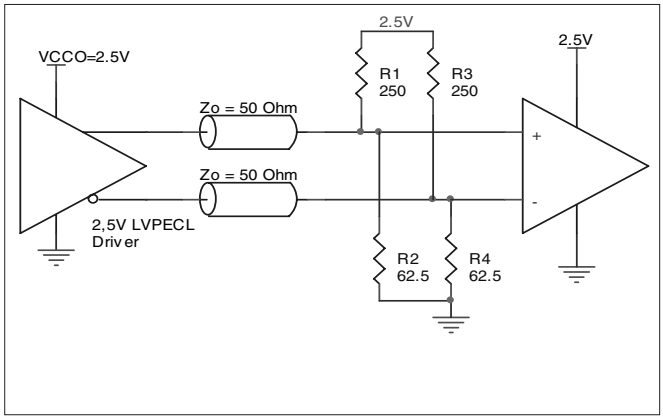


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

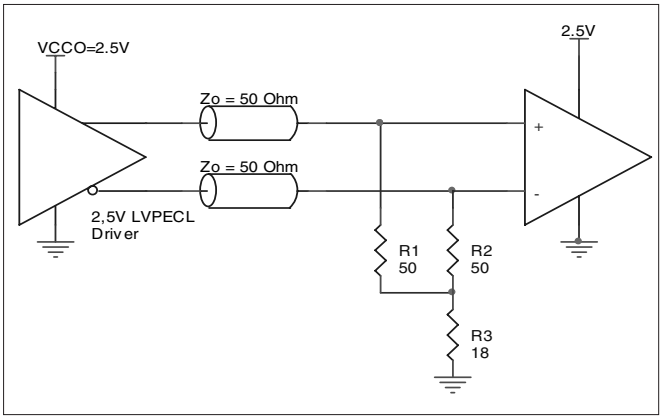


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

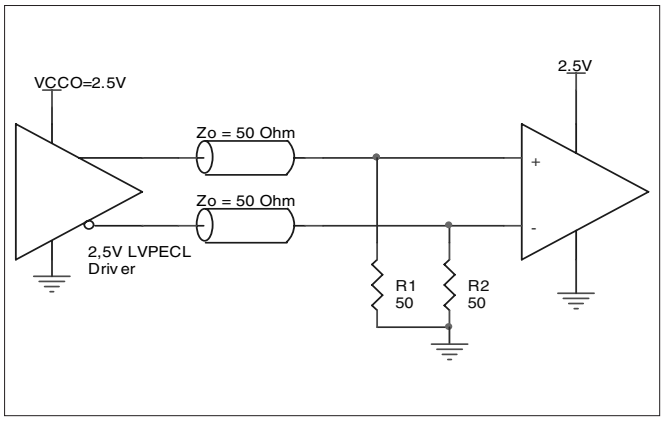


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

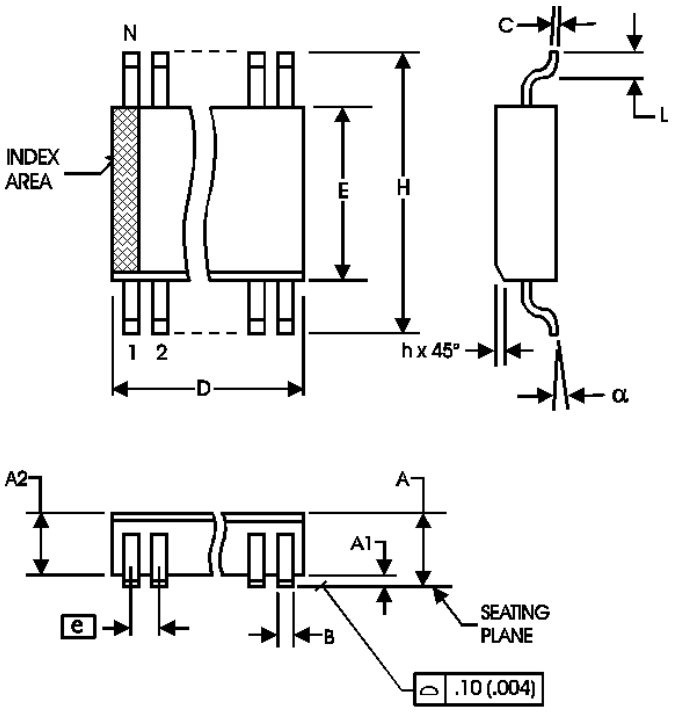
TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843256 is: 3863

PACKAGE OUTLINE - M SUFFIX FOR 24 LEAD SOIC



PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

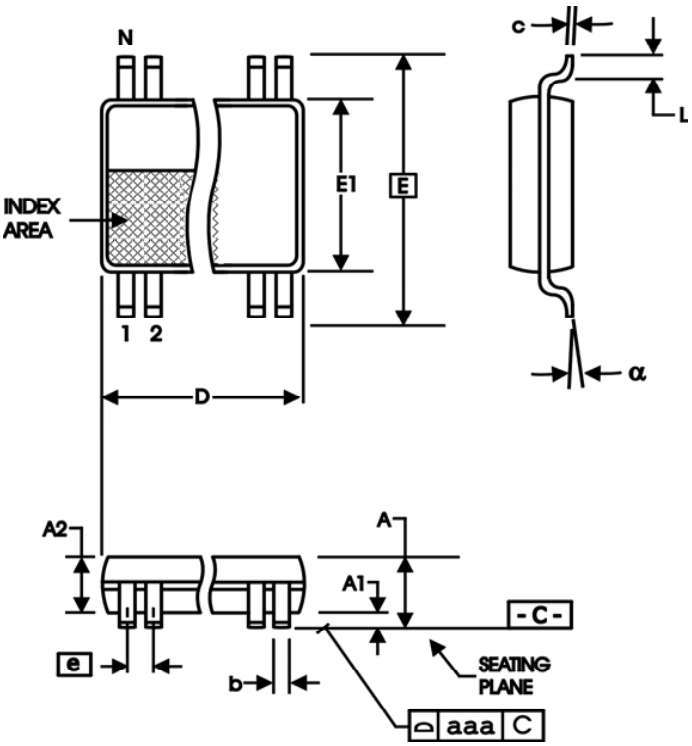


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843256AM	TBD	24 Lead SOIC	tube	0°C to 70°C
ICS843256AMT	TBD	24 Lead SOIC	1000 tape & reel	0°C to 70°C
ICS843256AMLF	TBD	24 Lead "Lead-Free" SOIC	tube	0°C to 70°C
ICS843256AMLFT	TBD	24 Lead "Lead-Free" SOIC	1000 tape & reel	0°C to 70°C
ICS843256AG	ICS843256AG	24 Lead TSSOP	tube	0°C to 70°C
ICS843256AGT	ICS843256AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843256AGLF	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843256AGLFT	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.