EM78P157N

8-Bit Microcontroller with OTP ROM

Product Specification

Doc. Version 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	09/22/2005

1 General Description

EM78P157N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is equipped with 1K*13-bits Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides three PROTECTION bits to prevent user's code in the OTP memory from being intruded. Eight OPTION bits are also provided to meet user's additional requirements.

With its OTP-ROM feature, the EM78P157N is able to offer a convenient way of developing and verifying user's programs. Moreover, user can take advantage of ELAN DWriter to easily program his development code.

2 Features

- Operating voltage range**:** 2.5V~5.5V
- Operating temperature range**:** -40°C~85°C
- Operating frequency range (base on 2 clocks)**:**
  - Crystal mode: DC~20MHz at 5V, DC~8MHz at 3V, DC~4MHz at 2.5V.
  - ERC mode: DC~4MHz at 5V, DC~4MHz at 3V, DC~4MHz at 2.5V.
- Low power consumption**:**
  - Less then 2 mA at 5V/4MHz
  - Typically 20 μA at 3V/32KHz
  - Typically 1 μA during sleep mode
- 1K × 13 bits on chip ROM
- One security register to prevent intrusion of OTP memory codes
- One configuration register to accommodate user's requirements
- 48× 8 bits on chip registers (SRAM, general purpose register)
- 2 bi-directional I/O ports
- 5 level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- Two clocks per instruction cycle
- Power down (SLEEP) mode
- Three available interruptions
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - External interrupt

- Programmable free running watchdog timer
- 8 programmable pull-high pins
- 7 programmable pull-down pins
- 8 programmable open-drain pins
- 2 programmable R-option pins
- Package types:
  - 14 pin DIP 300mil : EM78P157NBP
  - 14 pin SOP 150mil : EM78P157NBM
  - 18 pin DIP 300mil : EM78P157NAP
  - 18 pin SOP 300mil : EM78P157NAM
  - 20 pin SSOP 209mil : EM78P157NAAS
  - 20 pin SSOP 209mil : EM78P157NAKM
- 99.9% single instruction cycle commands
- The transient point of system frequency between HXT and LXT is around 400KHz

3 Pin Assignments and Descriptions

3.1 Pin Assignments

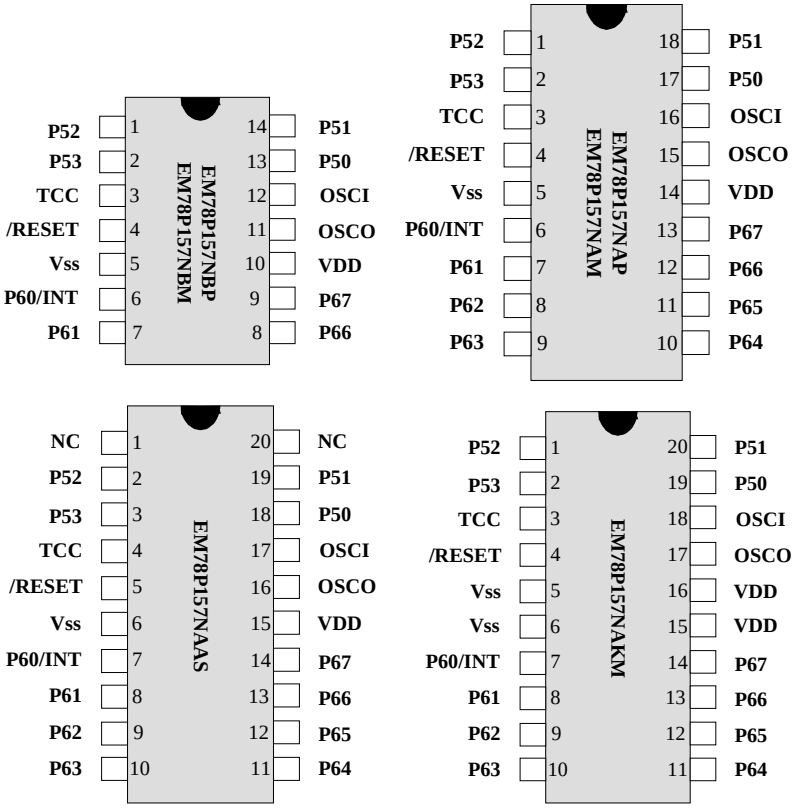


Fig. 1-1 Pin Assignments

3.2 Pin Descriptions

3.2.1 EM78P157NBP and EM78P157NBM Pin Descriptions

Symbol	Pin No.	Type	Function
VDD	10	–	• Power supply
OSCI	12	I	• XTAL type: Crystal input terminal or external clock input pin • ERC type: RC oscillator input pin
OSCO	11	I/O	• XTAL type: Output terminal for crystal oscillator or external clock input pin • RC type: Instruction clock output • External clock signal input
TCC	3	I	• The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use
/RESET	4	I	• Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain at reset condition.
P50~P53	13, 14, 1, 2	I/O	• P50~P53 are bi-directional I/O pins • P50 and P51 can also be defined as the R-option pins • P50~P52 can be set as pull-down by software
P60~P61	6~7	I/O	• P60~P61 are bi-directional I/O pins • These pins can be set as pull-high, pull-down, or open-drain through software programming
P66~P67	8~9	I/O	• P66~P67 are bi-directional I/O pins • These pins can be set as pull-high or open-drain through software programming
/INT	6	I	• External interrupt pin triggered by falling edge
VSS	5	–	• Ground

3.2.2 EM78P157NAP and EM78P157NAM Pin Descriptions

Symbol	Pin No.	Type	Function
VDD	14	–	• Power supply
OSCI	16	I	• XTAL type: Crystal input terminal or external clock input pin • ERC type: RC oscillator input pin
OSCO	15	I/O	• XTAL type: Output terminal for crystal oscillator or external clock input pin • RC type: Instruction clock output • External clock signal input
TCC	3	I	• The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use
/RESET	4	I	• Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain at reset condition.
P50~P53	17,18, 1, 2	I/O	• P50~P53 are bi-directional I/O pins • P50 and P51 can also be defined as the R-option pins • P50~P52 can be set as pull-down by software
P60~P67	6~13	I/O	• P60~P67 are bi-directional I/O pins • These pins can be set as pull-high or open-drain through software programming • P60~P63 can also be set as pull-down by software
/INT	6	I	• External interrupt pin triggered by falling edge
VSS	5	–	• Ground

3.2.3 EM78P157NAAS Pin Descriptions

Symbol	Pin No.	Type	Function
VDD	15	–	• Power supply
OSCI	17	I	• XTAL type: Crystal input terminal or external clock input pin • ERC type: RC oscillator input pin
OSCO	16	I/O	• XTAL type: Output terminal for crystal oscillator or external clock input pin • RC type: Instruction clock output • External clock signal input
TCC	4	I	• The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use
/RESET	5	I	• Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain at reset condition.
P50~P53	18, 19, 2, 3	I/O	• P50~P53 are bi-directional I/O pins • P50 and P51 can also be defined as the R-option pins • P50~P52 can be set as pull-down by software
P60~P67	7~14	I/O	• P60~P67 are bi-directional I/O pins • These pins can be set as pull-high or open-drain through software programming • P60~P63 can also be set as pull-down by software
/INT	7	I	• External interrupt pin triggered by falling edge
VSS	6	–	• Ground

3.2.4 EM78P157NAKM Pin Descriptions

Symbol	Pin No.	Type	Function
VDD	15,16	–	• Power supply
OSCI	18	I	• XTAL type: Crystal input terminal or external clock input pin • ERC type: RC oscillator input pin
OSCO	17	I/O	• XTAL type: Output terminal for crystal oscillator or external clock input pin • RC type: Instruction clock output • External clock signal input
TCC	3	I	• The real time clock/counter (with Schmitt trigger input pin), must be tied to VDD or VSS if not in use
/RESET	4	I	• Input pin with Schmitt trigger. If this pin remains at logic low, the controller will also remain at reset condition.
P50~P53	19, 20, 1, 2	I/O	• P50~P53 are bi-directional I/O pins • P50 and P51 can also be defined as the R-option pins • P50~P52 can be set as pull-down by software
P60~P67	7~14	I/O	• P60~P67 are bi-directional I/O pins • These pins can be set as pull-high or open-drain through software programming • P60~P63 can also be set as pull-down by software
/INT	7	I	• External interrupt pin triggered by falling edge
VSS	5, 6	–	• Ground

4 Function Description

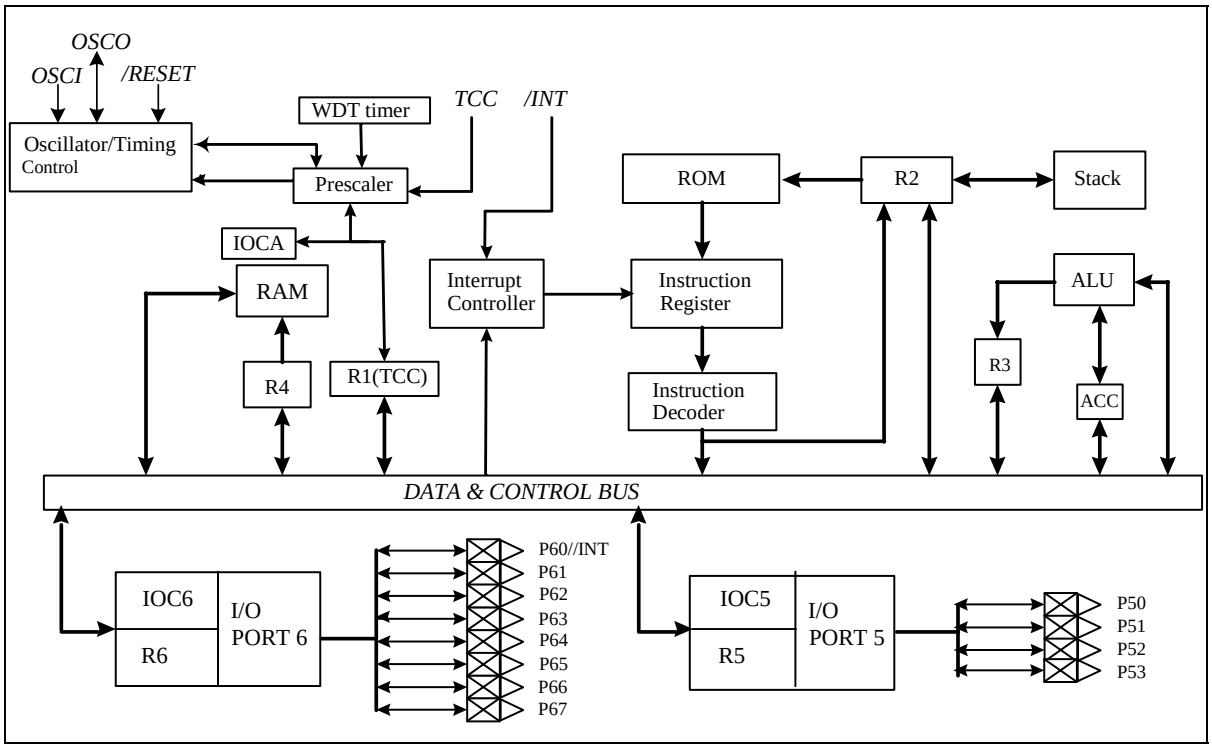


Fig. 4-1 Function Block Diagram

4.1 Operational Registers

The following is the operational registers' data memory configuration.

Address	R PAGE Registers	IOC PAGE Registers
00	R0 (IAR)	Reserve
01	R1 (TCC)	CONT (Control Register)
02	R2 (PC)	Reserve
03	R3 (Status)	Reserve
04	R4 (RSR)	Reserve
05	R5 (Port5)	IOC5 (I/O Port Control Register)
06	R6 (Port6)	IOC6 (I/O Port Control Register)
07	Reserve	Reserve
08	Reserve	Reserve
09	Reserve	Reserve
0A	Reserve	IOCA (Prescaler Control Register)
0B	Reserve	IOCB (Pull-down Register)
0C	Reserve	IOCC (Open-drain Control)
0D	Reserve	IOCD (Pull-high Control Register)
0E	Reserve	IOCE (WDT Control Register)
0F	RF (Interrupt Status)	IOCF (Interrupt Mask Register)
10 : 3F	General Registers	

4.1.1 Indirect Addressing (R0) Register

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

4.1.2 Time Clock / Counter (R1) Register

- Increased by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when TCC register is written with a value.

4.1.3 Program Counter and Stack (R2) Register

- Depending on the device type, R2 and hardware stack are 10-bits wide. The R2 structure is depicted in Fig. 4-2 below.
- Generates 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all “0” when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k," "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows the contents of ‘A’ to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that writes to R2 (e.g., "ADD R2,A," "MOV R2,A," "BC R2,6",·etc.) will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

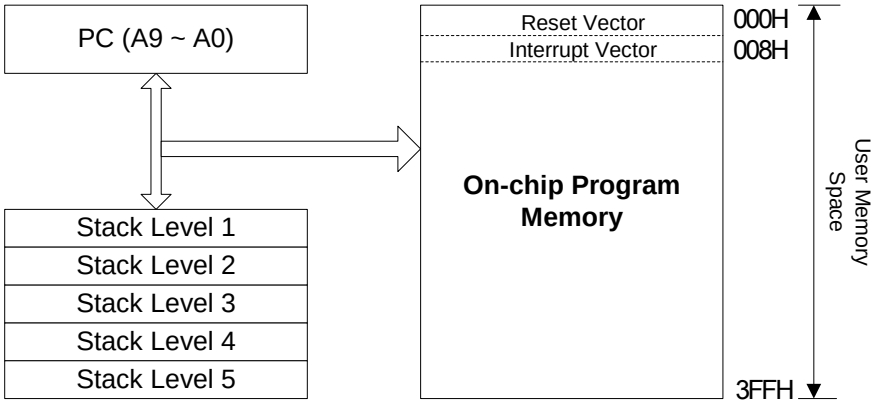


Fig. 4-2 R2 (Program Counter) & Stack Organization

4.1.4 Status (R3) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP2	GP1	GP0	T	P	Z	DC	C

Bit 0 (C): Carry flag

Bit 1 (DC): Auxiliary carry flag

Bit 2 (Z): Zero flag
Set to "**1**" if the result of an arithmetic or logic operation is zero

Bit 3 (P): Power down bit
Set to "**1**" during power on or by a "WDTC" command
Reset to "**0**" by a "SLEP" command

Bit 4 (T): Time-out bit
Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up
Reset to "**0**" by WDT time-out

Bit 5~7 (GP0 ~ 2): General-purpose read/write bits

4.1.5 RAM Select (R4) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not used (read only)		Select Registers					

Z flag of R3 will set to "**1**" when R4 content is equal to "3F." When R4=R4+1, R4 content will function as R0. See the data memory configuration shown in Section 4.1.

Bits 0~5: are used to select registers (Address**:** 00~06, 0F~3F) in indirect address mode

Bits 6~7: are not used (read only)
Bits 6~7 are set to "**1**" all the time

4.1.6 Port 5 ~ Port 6 (R5 ~ R6) Registers

R5 and R6 are I/O registers. Only the lower 4 bits of R5 are available.

4.1.7 Interrupt Status (RF) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

RF can be cleared by instruction but cannot be set

IOCF is the interrupt mask register (see Section 4.2.9)

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

0: disable interrupt request
1: enable interrupt request

Bit 0 (TCIF): TCC overflow interrupt flag
Set when TCC overflows. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag
Set when Port 6 input changes. Reset by software.

Bit 2 (EXIF): External interrupt flag
Set by falling edge on /INT pin. Reset by software.

Bits 3 ~ 7: Not used

4.1.8 General Purpose (R10 ~ R3F) Registers

R10 ~ R3F are all 8-bit general-purpose registers

4.2 Special Purpose Registers

4.2.1 Accumulator (A) Register

- Internal data transfer, or instruction operand holding
- It cannot be addressed

4.2.2 Control (CONT) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

CONT register is both readable and writable

Bit 0 ~ Bit 2 (PSR0 ~ PSR2): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB): Prescaler assignment bit
0: TCC
1: WDT

Bit 4 (TE): TCC signal edge
0: increment if the transition from **low** to high takes place on TCC pin
1: increment if the transition from **high** to low takes place on TCC pin

Bit 5 (TS): TCC signal source
0: internal instruction cycle clock
1: transition on TCC pin

Bit 6 (/INT): Interrupt enable flag
0: masked by DISI or hardware interrupt
1: enabled by ENI/RETI instructions

Bit 7: Not used

4.2.3 I/O Port Control (IOC5 ~ IOC6) Registers

- **0:** defines the relative I/O pin as output
  1: put the relative I/O pin into high impedance
- Only the lower 4 bits of IOC5 can be defined.
- IOC5 and IOC6 registers are both readable and writable

4.2.4 Prescaler Counter (IOCA) Register

- IOCA register is readable
- The value of IOCA is equal to the contents of Prescaler counter
- Down counter

4.2.5 Pull-Down Control (IOCB) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	-	/PD2	/PD1	/PD0

IOCB Register is both readable and writable.

Bit 0 (/PD0): Control bit is used to enable the P50 pin pull-down
0: Enable internal pull-down
1: Disable internal pull-down

Bit 1 (/PD1): Control bit is used to enable the P51 pin pull-down

Bit 2 (/PD2): Control bit is used to enable the P52 pin pull-down

Bit 3: Not used

Bit 4 (/PD4): Control bit is used to enable the P60 pin pull-down

Bit 5 (/PD5): Control bit is used to enable the P61 pin pull-down

Bit 6 (/PD6): Control bit is used to enable the P62 pin pull-down

Bit 7 (/PD7): Control bit is used to enable the P63 pin pull-down

4.2.6 Open-Drain Control (IOCC) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

IOCC Register is both readable and writable.

Bit 0 (OD0): Control bit is used to enable the P60 pin open-drain
0: Disable open-drain output
1: Enable open-drain output

Bit 1 (OD1): Control bit is used to enable the P61 pin open-drain

Bit 2 (OD2): Control bit is used to enable the P62 pin open-drain

Bit 3 (OD3): Control bit is used to enable the P63 pin open-drain

Bit 4 (OD4): Control bit is used to enable the P64 pin open-drain

Bit 5 (OD5): Control bit is used to enable the P65 pin open-drain

Bit 6 (OD6): Control bit is used to enable the P66 pin open-drain

Bit 7 (OD7): Control bit is used to enable the P67 pin open-drain

4.2.7 Pull-High Control (IOCD) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

IOCD Register is both readable and writable

Bit 0 (/PH0): Control bit is used to enable the P60 pin pull-high
0: Enable internal pull-high
1: Disable internal pull-high

Bit 1 (/PH1): Control bit is used to enable the P61 pin pull-high

Bit 2 (/PH2): Control bit is used to enable the P62 pin pull-high

Bit 3 (/PH3): Control bit is used to enable the P63 pin pull-high

Bit 4 (/PH4): Control bit is used to enable the P64 pin pull-high

Bit 5 (/PH5): Control bit is used to enable the P65 pin pull-high

Bit 6 (/PH6): Control bit is used to enable the P66 pin pull-high

Bit 7 (/PH7): Control bit is used to enable the P67 pin pull-high

4.2.8 WDT Control (IOCE) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	ROC	-	-	-	-

Bits 0~3, 5: Not used

Bit 4 (ROC): ROC is used for the R-option
Setting the ROC to "**1**" will enable the status of R-option pins (P50~P51) that are read by the controller. Clearing the ROC will disable the R-option function. If the R-option function is selected, you must connect the P51 pin or/and P50 pin to VSS with a 430KΩ external resistor (Rex). If the Rex is connected or disconnected, the status of P50 (P51) is read as "**0**" or "**1**" respectively Refer to Fig. 4-6 under Section 4.4.

Bit 6 (EIS): Control bit is used to define the P60 (/INT) pin function
0: P60, bi-directional I/O pin
1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (bit 0 of IOC6) must be set to "**1**"

EIS is both readable and writable.

When EIS is "**0**," the path of /INT is masked. When EIS is "**1**," the status of /INT pin can also be read by way of reading Port 6 (R6). Refer to Fig. 4-5(a) under Section 4.4.

Bit 7 (WDTE): Control bit is used to enable Watchdog timer
0: Disable WDT
1: Enable WDT
WDTE is both readable and writable

4.2.9 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIE	ICIE	TCIE

Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**."

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 4-8 under Section 4.6.

IOCF register is both readable and writable.

Bit 0 (TCIE): TCIF interrupt enable bit
0: disable TCIF interrupt
1: enable TCIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit
0: disable ICIF interrupt
1: enable ICIF interrupt

Bit 2 (EXIE): EXIF interrupt enable bit
0: disable EXIF interrupt
1: enable EXIF interrupt

Bits 3~7: Not used.

4.3 TCC/WDT & Prescaler

An 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT only at any given time, and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. Fig. 4-3 below, depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). Referring to Fig. 4-3 below, CLK=Fosc/2 or CLK=Fosc/4 application is determined by the CODE Option bit CLK status. CLK=Fosc/2 is used when CLK bit is "**0**," and CLK=Fosc/4 is used when CLK bit is "**1**." If TCC signal source comes from external clock input, TCC is increased by 1 at every falling edge or rising edge of TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

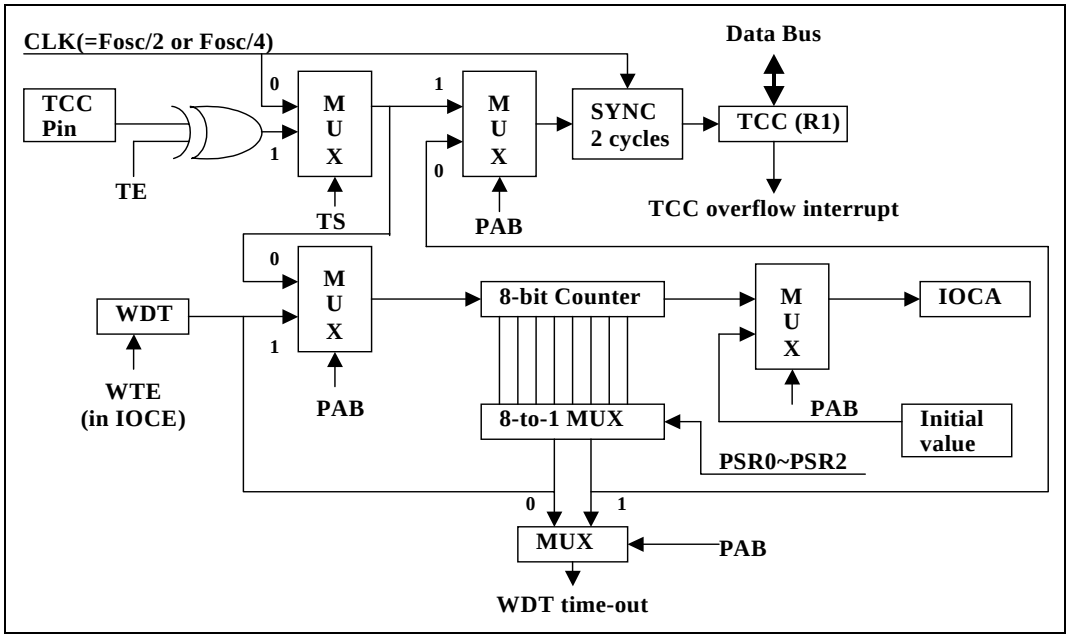


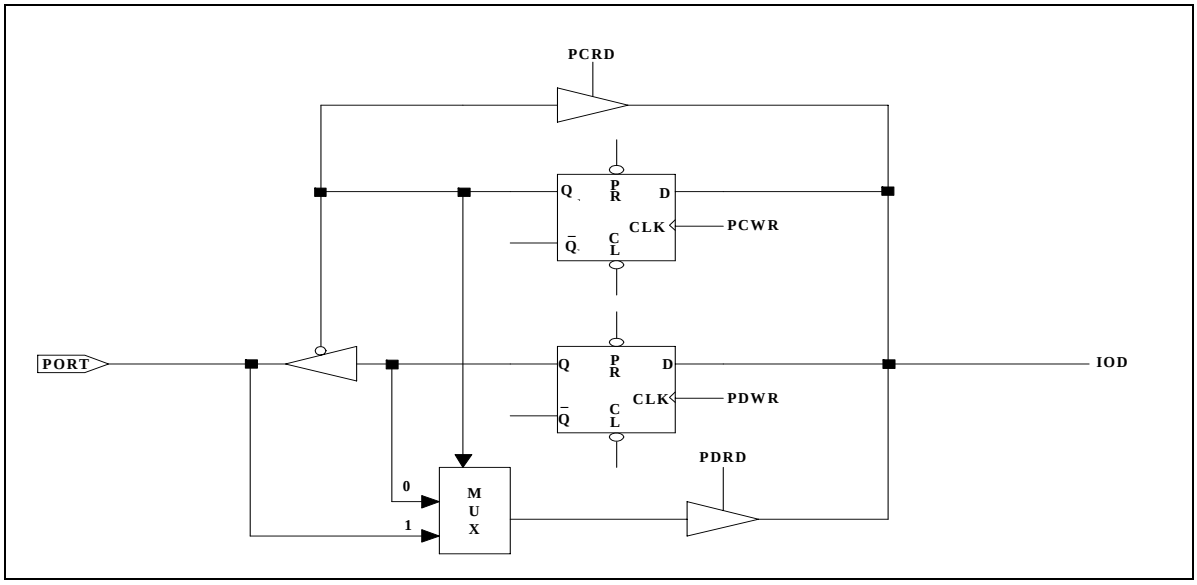
Fig. 4-3 TCC and WDT Block Diagram

4.4 I/O Ports

The I/O registers, both Port 5 and Port 6, are bi-directional tri-state I/O ports. Port 6 can be set as pull-high internally by software. Furthermore, Port 6 can also be set as open-drain output by software and supports input status change interrupt (or wake-up) function. P50 ~ P52 and P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6). P50 ~ P51 are the R-option pins which are enabled by setting the ROC bit in the IOCE register to "**1**." When the R-option function is used, it is recommended that P50 ~ P51 are used as output pins. When R-option is in enabled state, P50 ~ P51 must be programmed as input pins. Under R-option mode, the current/power consumption by Rex should be taken into the consideration to promote energy conservation.

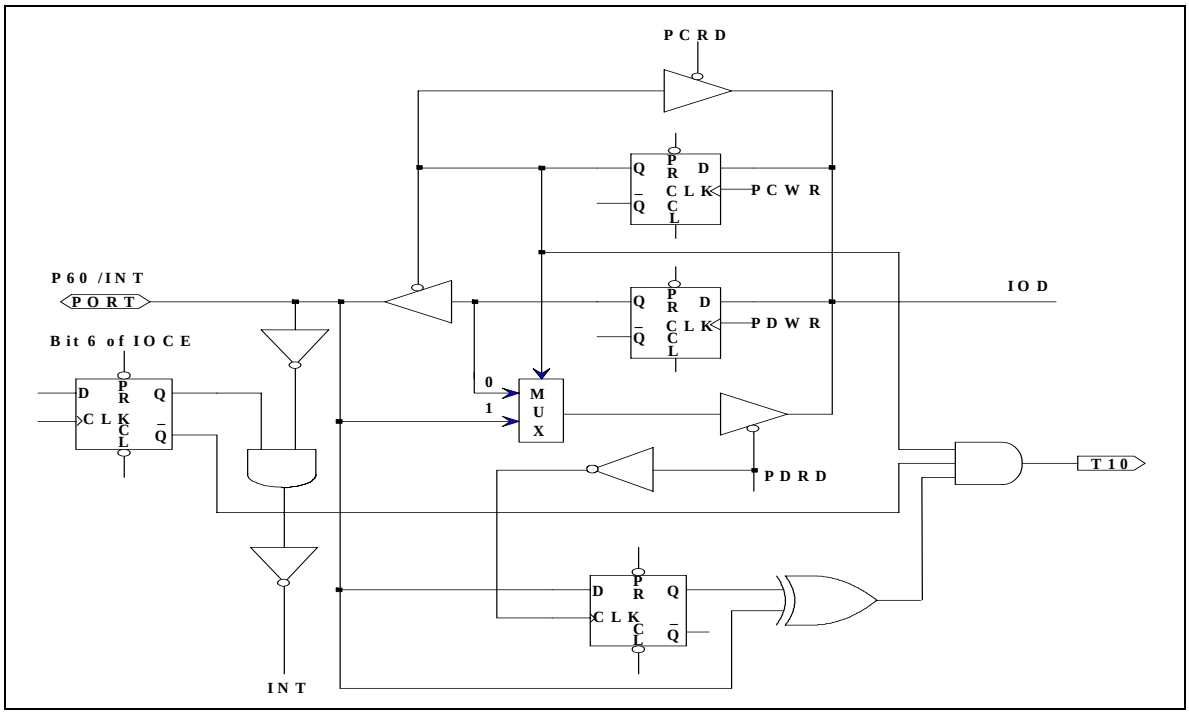
The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are depicted in Figures 4-4, 4-5(a), 4-5(b), and 4-6 shown below.

[1] *Vdd = 5V, set up time period = 16.8ms ± 30%*
Vdd = 3V, set up time period = 18ms ± 30%



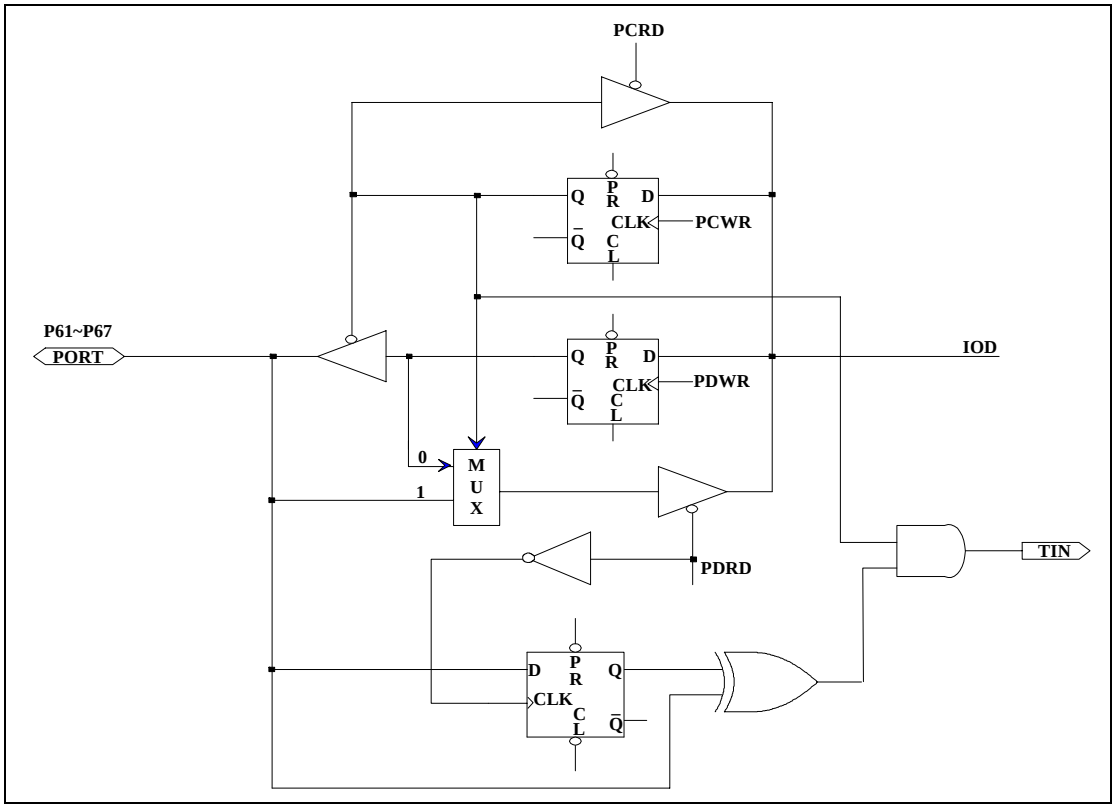
NOTE: *Pull-down is not shown in the figure*

Fig. 4-4(a) I/O Port and I/O Control Register Port 5 Circuit Diagram



NOTE: *Pull-high/down and open-drain are not shown in the figure*

Fig. 4-5(b) I/O Port and I/O Control Register P60 (/INT) Circuit Diagram



NOTE: *Pull-high/down and open-drain are not shown in the figure*

Fig. 4-5(c) I/O Port and I/O Control Register for P61~P67 Circuit Diagram

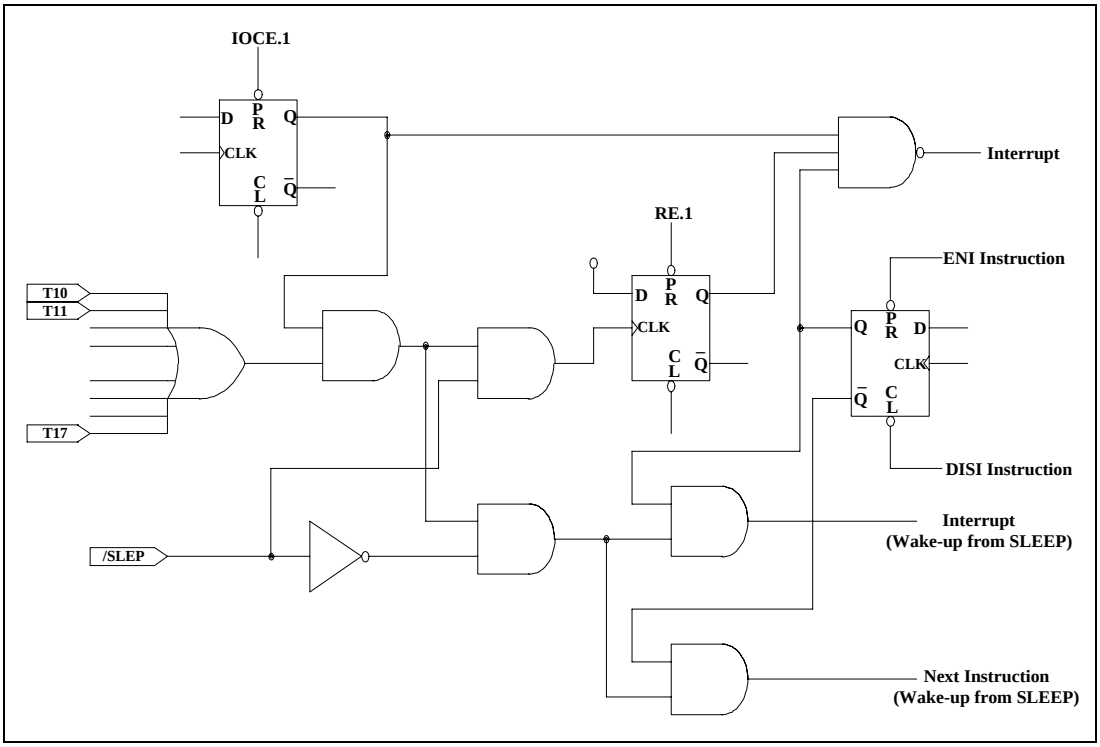


Fig. 4-5(d) Block Diagram on I/O Port 6 with Input Change Interrupt/Wake-up

4.4.1 Port 6 Input Change Wake-up/Interrupt Function Usage

(I) Wake-up from Port 6 Input Status Change	(II) Port 6 Input Status Change Interrupt
(a) Before SLEEP	1. Read I/O Port 6 (MOV R6,R6)
1. Disable WDT* (using very carefully)	2. Execute "ENI"
2. Read I/O Port 6 (MOV R6,R6)	3. Enable interrupt (Set IOCF.1)
3. Execute "ENI" or "DISI"	4. IF Port 6 change (interrupt)
4. Enable interrupt (Set IOCF.1)	→ Interrupt vector (008H)
5. Execute "SLEP" instruction	
(b) After Wake-up	
1. IF "ENI" → Interrupt vector (008H)	
2. IF "DISI" → Next instruction	

* Software disables WDT (watchdog timer) but hardware must be enabled before applying the Port 6 Change Wake-Up function (CODE Option Register and Bit 11 (ENWDTB-) set to "**1**").

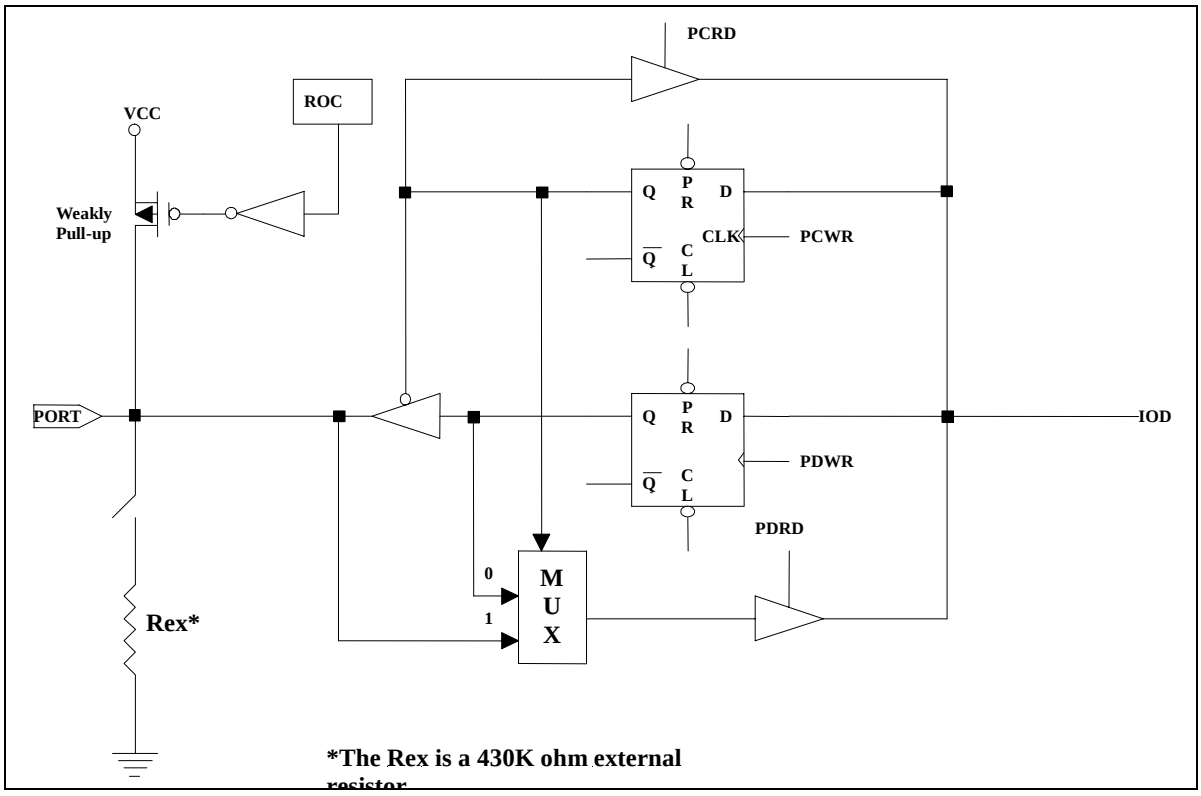


Fig. 4-6 I/O Port with R-option (P50,P51) Circuit Diagram

4.5 RESET and Wake-up

A RESET is initiated by one of the following events**:**

1. Power on reset
2. /RESET pin input "low," or
3. WDT time-out (if enabled)

The device is kept in a RESET condition for a period of approximately 18ms[2] (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed (see Fig. 4-7 under Section 4.5.2.1)

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "**0**."
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- All the CONT register bits are set to "**1**" except for the Bit 6 (INT flag).
- All the IOCA register bits are set to "**1**."
- All the IOCB register bits are set to "**1**."
- The IOCC register is cleared.
- All the IOCD register bits are set to "**1**."
- Bit 7 of the IOCE register is set to "**1**," and Bits 4 and 6 are cleared.
- Bits 0 ~2 of RF and bits 0 ~2 of IOCF registers are cleared.

The sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be awakened by**:**

1. External reset input on /RESET pin,
2. WDT time-out (if enabled), or
3. Port 6 input status changes (if enabled).

The first two cases will cause the EM78P157N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). The last case is considered the continuation of the program execution. The global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 008H after wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after wake-up.

[2] *Vdd = 5V, set up time period = 16.8ms ± 30%*
Vdd = 3V, set up time period = 18ms ± 30%

Only one of Cases 2 and 3 can be enabled before entering into sleep mode, i.e.,

[a] if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P157N can be awakened only by either Case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P157N can only be awakened by either Case 1 or 2. Refer to the section (Section 4.6) on Interrupt.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P157N (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xx000110b       ; Select internal TCC clock
CONTW
CLR R1                  ; Clear TCC and prescaler
MOV A, @xxxx1110b       ; Select WDT prescaler
CONTW
WDTC                    ; Clear WDT and prescaler
MOV A, @0xxxxxxxb       ; Disable WDT
IOW RE
MOV R6, R6              ; Read Port 6
MOV A, @00000x1xb       ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)           ; Enable (or disable) global interrupt
SLEP                    ; Sleep

NOP
```

One problem you should be aware of is that after waking up from the sleep mode, WDT is enabled automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from the sleep mode.

4.5.1 Summary of Initialized Values for Registers

Legend:
U = Unknown or don't care **P** = Previous value before reset **t** = Check with Section 4.5.2.1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	X	X	X	X	C53	C52	C51	C50
		Power-On	U	U	U	U	1	1	1	1
		/RESET and WDT	U	U	U	U	1	1	1	1
		Wake-Up from Pin Change	U	U	U	U	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	X	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	*0/P	*0/P	*0/P	*0/P	*1/P	*0/P	*0/P	*0/P
0x03	R3(SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-On	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-Up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	U	U	U	U	U	U
		/RESET and WDT	1	1	P	P	P	P	P	P
		Wake-Up from Pin Change	1	1	P	P	P	P	P	P
0x05	P5	Bit Name	X	X	X	X	P53	P52	P51	P50
		Power-On	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	P	P	P	P
		Wake-Up from Pin Change	0	0	0	0	P	P	P	P

* Jump to address 0x08, or execute the instruction following the "SLEP" instruction.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0F	RF(ISR)	Bit Name	X	X	X	X	X	EXIF	ICIF	TCIF
		Power-On	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-Up from Pin Change	U	U	U	U	U	P	P	P
0x0A	IOCA	Bit Name	-	-	-	-	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	X	/PD2	/PD1	/PD0
		Power-On	1	1	1	1	U	1	1	1
		/RESET and WDT	1	1	1	1	U	1	1	1
		Wake-Up from Pin Change	P	P	P	P	U	P	P	P
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	X	ROC	X	X	X	X
		Power-On	1	0	U	0	U	U	U	U
		/RESET and WDT	1	0	U	0	U	U	U	U
		Wake-Up from Pin Change	1	P	U	P	U	U	U	U
0x0F	IOCF	Bit Name	X	X	X	X	X	EXIE	ICIE	TCIE
		Power-On	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-Up from Pin Change	U	U	U	U	U	P	P	P
0x10~0x2F	R10~R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

4.5.2 The Status of RST, T, and P of STATUS Register

A RESET condition is initiated by the following events:

1. A power-on condition
2. A high-low-high pulse on /RESET pin
3. Watchdog timer time-out

4.5.2.1 RST, T and P after RESET Values

The values of T (Time-out) and P (Power-down) as listed below are used to verify how the processor wakes up.

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during SLEEP mode	0	0
Wake-Up on pin change during SLEEP mode	1	0

*P = Previous status before reset

4.5.2.2 Event Affecting T and P Status

The table below shows the events that may affect the status of T (Time-out) and P (Power-down).

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

*P = Previous status before reset

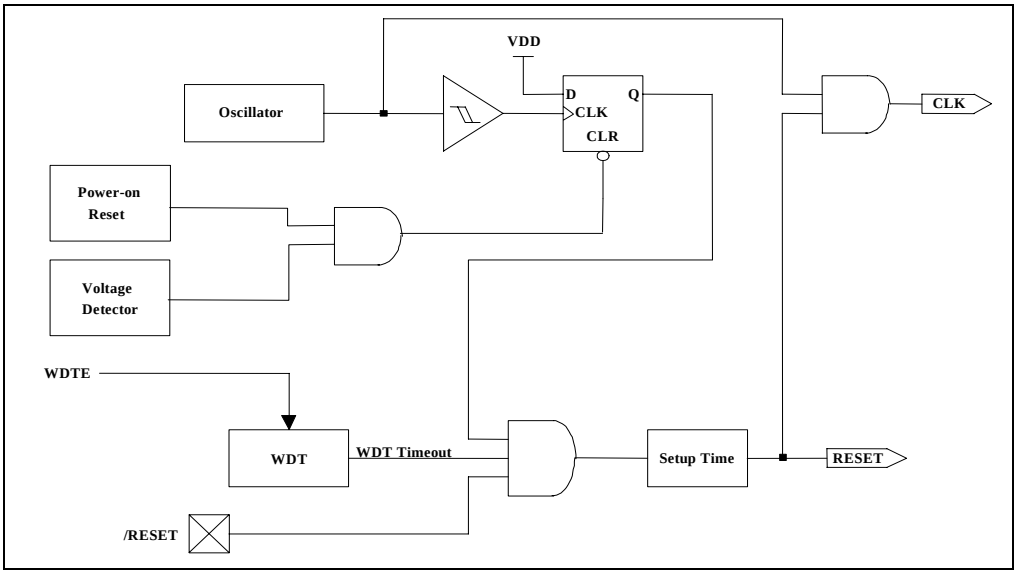


Fig. 4-7 Controller Reset Block Diagram

4.6 Interrupt

The EM78P157N has three falling-edge interrupts as listed below**:**

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External interrupt [(P60, /INT) pin].

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6,R6") is necessary. Each Port 6 pin of will have this feature when its status changes. Any pin configured as output or P60 pin configured as “/INT,” is excluded from this function. The Port 6 Input Status Change Interrupt can wake up the EM78P157N from the sleep mode if Port 6 is enabled prior to going into the sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the succeeding address if the global interrupt is disabled or branches to the interrupt vector 008H if the global interrupt is enabled.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or ENI execution. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Fig. 4-7 above). The RETI instruction ends the interrupt routine and enables the global interrupt (execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from address 001H.

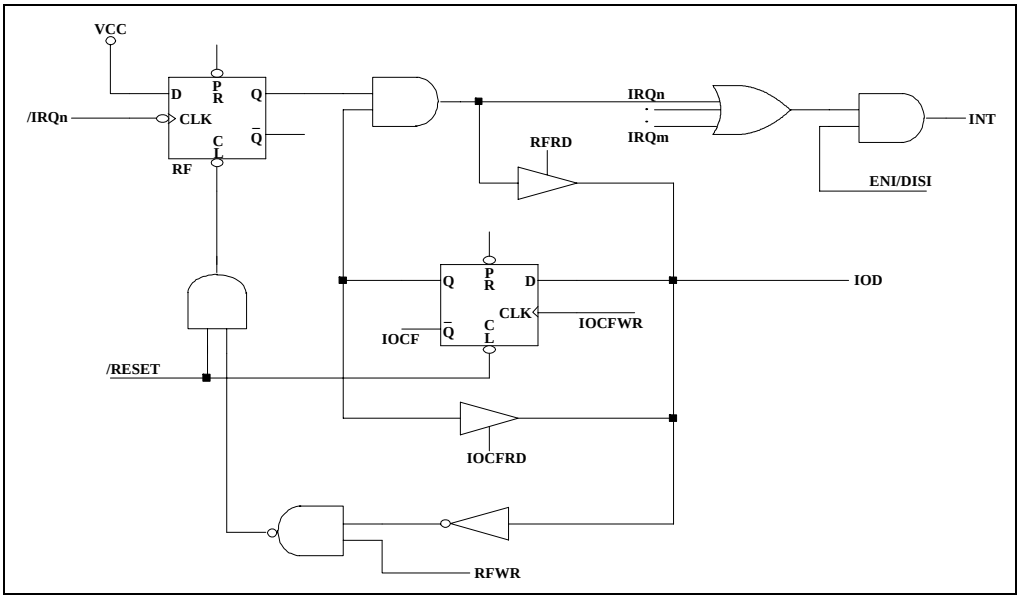


Fig. 4-8 Interrupt Input Circuit

4.7 Oscillator

4.7.1 Oscillator Modes

The EM78P157N can be operated in three different oscillator modes, namely, External RC oscillator mode (ERC), High XTAL oscillator mode (HXT), and Low XTAL oscillator mode (LXT). User can select one of them by programming OSC, HLF, and HLP in the CODE option register. The following table depicts how these three modes are defined.

4.7.1.1 Oscillator Modes Defined by OSC, HLF, and HLP

Mode	OSC	HLF	HLP
ERC (External RC oscillator mode)	0	X[2]	X[2]
HXT (High XTAL oscillator mode)[1]	1	1	X[2]
LXT (Low XTAL oscillator mode)[1]	1	0	0

[1] *The transient point of system frequency between HXT and LXY is around 400 kHz*

[2] *X = Don't care*

4.7.1.2 The Summary of Maximum Operating Speeds

The maximum operational frequency of crystal/resonator under different VDDs is as listed below.

Condition	VDD	Fxt Max Freq.
Two cycles with two clocks	3.0	8.0 MHz
	5.0	20.0 MHz

4.7.2 Crystal Oscillator/Ceramic Resonators (XTAL)

EM78P157N can be driven by an external clock signal through the OSCI pin as illustrated in the following figure.

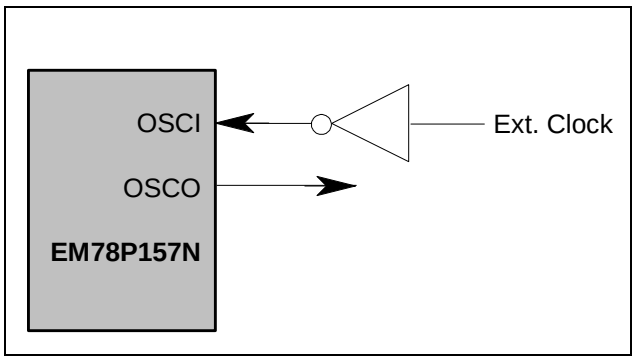


Fig. 4-9 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can connected with a crystal or ceramic resonator to generate oscillation. The figure below depicts such circuit. The same thing is applicable whether it is in the HXT mode or LXT mode. Table below provides the recommended values of C1 and C2. Since each resonator has its own attribute, you should refer to its specification for the appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

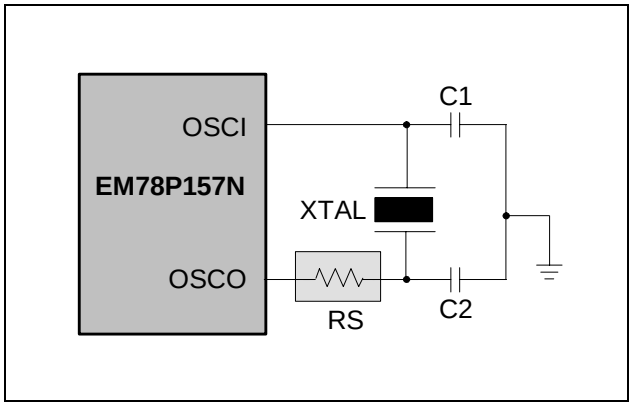


Fig. 4-10 Crystal/Resonator Circuit

4.7.2.1 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

The table below provides the recommended values of C1 and C2. Since each resonator has its own attribute, you should refer to its specification for the appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

Oscillator Type	Frequency Mode	Frequency	C1(pF)*	C2(pF)*
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100KHz	25	25
		200KHz	25	25
	HXT	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

* *The values shown for capacitors C1 & C2 are for reference only.*

4.7.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig. 4-11 below) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot accurately discharge the current of the capacitance.

Based on the above factors, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is laid out, will affect the system frequency.

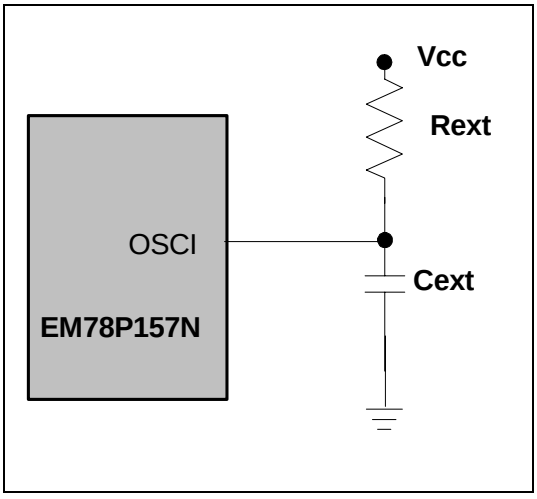


Fig. 4-11 External RC Oscillator Mode Circuit

4.7.3.1 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.92 MHz	3.65 MHz
	5.1k	2.67 MHz	2.60 MHz
	10k	1.39MHz	1.40 MHz
	100k	149 KHz	156 KHz
100 pF	3.3k	1.39 MHz	1.33 MHz
	5.1k	940 KHz	920 KHz
	10k	480 KHz	475 KHz
	100k	52 KHz	50 KHz
300 pF	3.3k	595 KHz	560 KHz
	5.1k	400 KHz	390 KHz
	10k	200 KHz	200 KHz
	100k	21 KHz	20 KHz

NOTE: *1. Values derived and measured from DIP packages*
2. Values are for design references only
3. The frequency drift is about ±30%

4.8 CODE Option Register

The EM78P157N has a CODE option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

The following is the Code Option Register and Customer ID Register arrangement distribution**:**

Word 0	Word 1
Bit12~Bit0	Bit12~Bit0

4.8.1 Code Option Register (Word 0)

WORD 0												
Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	CLKS	ENWDTB	-	HLF	OSC	HLP	PR2	PR1	PR0

Bit 9~Bit 12: Not used (reserved)
This bit is set to "**1**" all the time

Bit 8 (CLKS): Instruction period option bit
0: two oscillator periods
1: four oscillator periods
(Refer to Section 4-12, *Instruction Set*)

Bit 7 (ENWDTB): Watchdog timer enable bit
0: Enable
1: Disable

Bit 6: Not used (reserved)
This bit is set to "**1**" all the time

Bit 5 (HLF): XTAL frequency selection

0: XTAL2 type (low frequency, 32.768KHz)

1: XTAL1 type (high frequency)

This bit will affect system oscillation only when Bit 4 (OSC) is "1." When OSC is"0," HLF must be "0".

NOTE

The transient point of system frequency between HXT and LXY is around 400 KHz.

Bit 4 (OSC): Oscillator type selection

0: RC type

1: XTAL type (XTAL1 and XTAL2)

Bit 3 (HLP): Power selection

0: Low power

1: High power

Bit 2 ~ Bit 0 (PR2 ~ PR0): Protect bits

PR2 ~ PR0 are protect bits that can be set as follows**:**

PR2	PR1	PR0	Protect
0	0	0	Enable
0	0	1	Enable
0	1	0	Enable
0	1	1	Enable
1	0	0	Enable
1	0	1	Enable
1	1	0	Enable
1	1	1	Disable

4.8.2 Customer ID Register (Word 1)

Bit 12 ~ Bit 0
XXXXXXXXXXXX

Bit 12 ~ Bit 0: Customer's ID code

4.9 Power-On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays at its steady state.

EM78P157N POR voltage range is 1.2V~1.8V. Under customer application, when power is OFF, Vdd must drop to below 1.2V and remains OFF for 10μs before power can be switched ON again. This way, the EM78P157N will reset and works normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

4.10 External Power-On Reset Circuit

The circuit shown below implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach the minimum operation voltage. This circuit is used when the power supply has a slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing into /RESET pin.

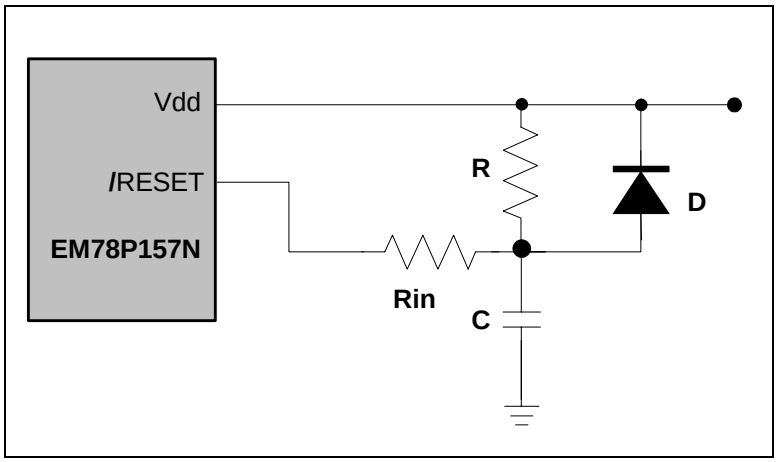


Fig. 4-12 External Power-Up Reset Circuit

4.11 Residual-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residual-voltage remains. The residual-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figures 4-13 and 4-14 illustrate how to build a residual-voltage protection circuit.

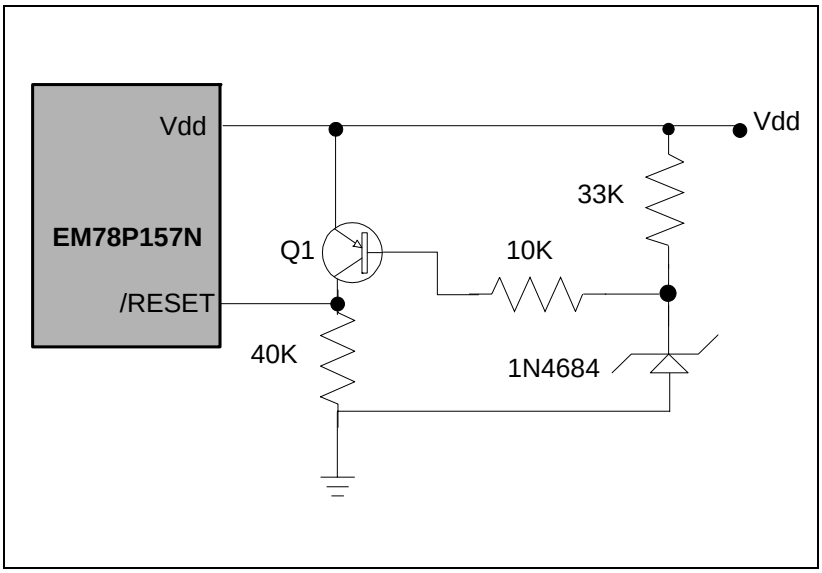


Fig. 4-13 Circuit 1 for the Residue Voltage Protection

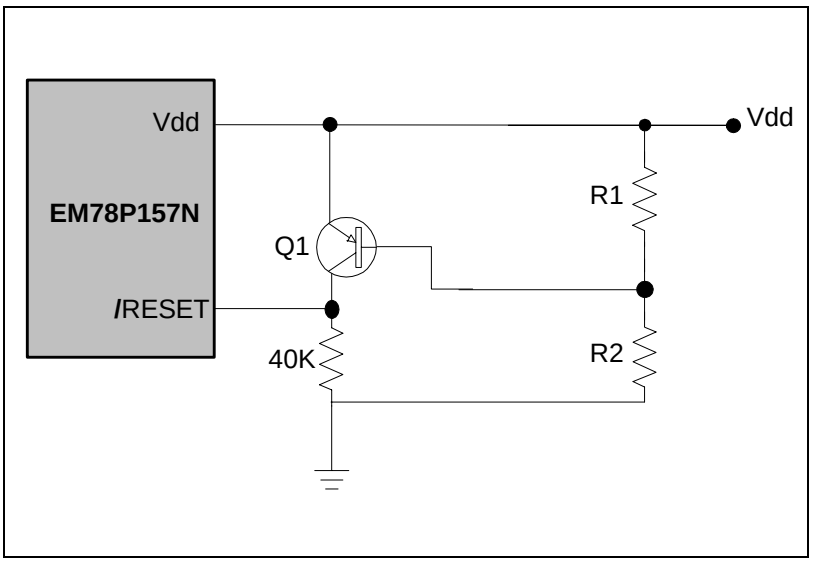


Fig. 4-14 Circuit 2 for the Residue Voltage Protection

4.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

1. Change one instruction cycle to consist of 4 oscillator periods.
2. "JMP," "CALL," "RET," "RETL," and "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," and "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (1) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/2 as indicated in Fig. 4-3 (TCC and WDT Block Diagram) in Section 4.3.

Furthermore, the instruction set has the following features**:**

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

LEGEND: "**R**" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.

"**b**" represents a bit field designator that selects the value for the bit which is located in the register "**R**" and affects operation.

"**k**" represents an 8 or 10-bit constant or literal value.

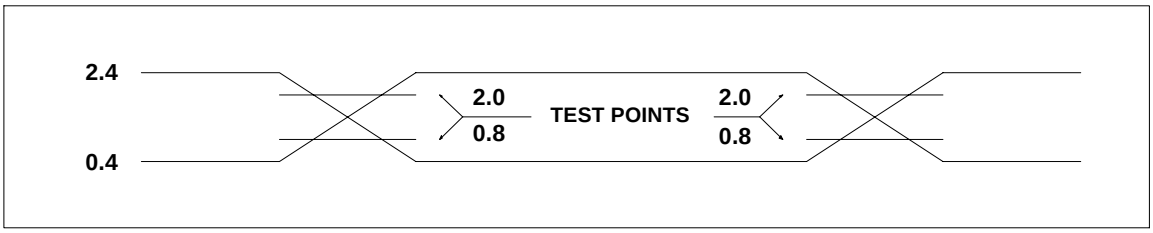
Instruction Binary	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z

Instruction Binary	Hex	Mnemonic	Operation	Status Affected
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

[1]This instruction is applicable to IOC5 ~ IOC6 and IOCB ~ IOCF only
[2]This instruction is not recommended for RF operation
[3]This instruction cannot operate under RF

4.13 Timing Diagrams

4.13.1 AC Test Input/Output Waveform



AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

Fig. 4-15 AC Test Input/Output Waveform Timing Diagram

4.13.2 RESET Timing (CLK = ”0”)

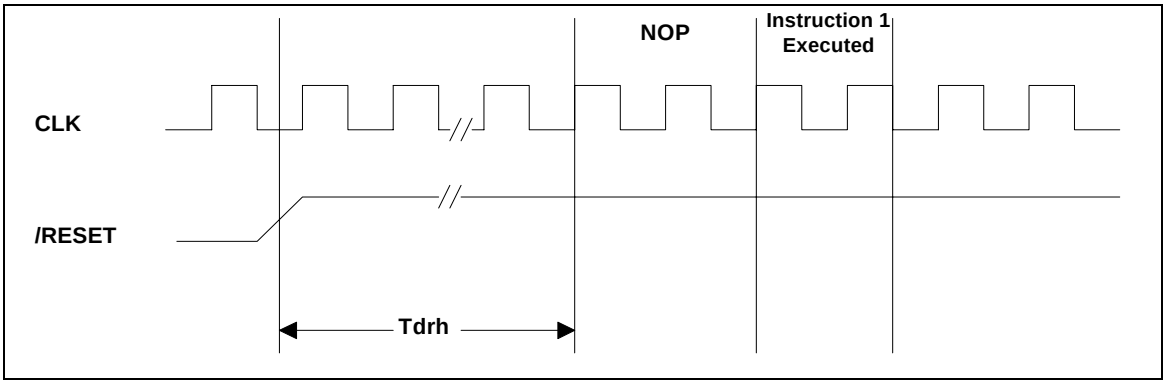


Fig. 4-16 RESET Timing (CLK = ”0”)Timing Diagram

4.13.3 TCC Input Timing (CLKS = ”0”)

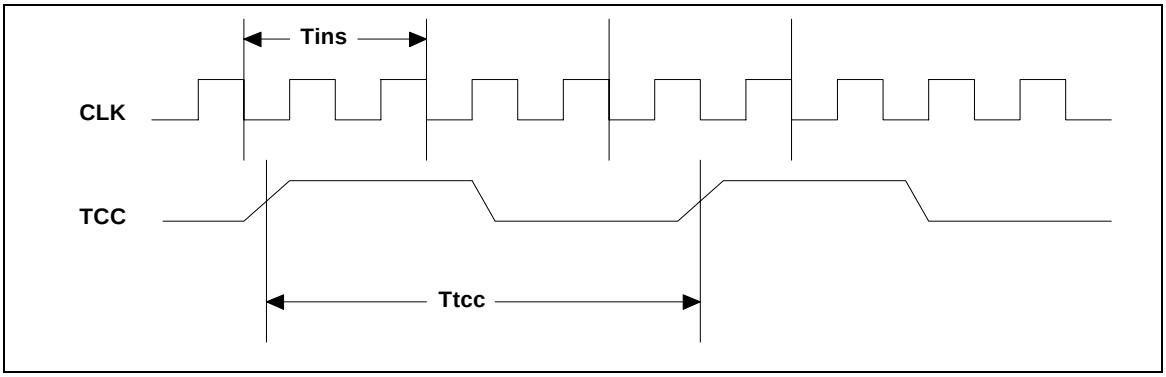


Fig. 4-17 TCC Input Timing (CLKS = ”0”) Timing Diagram

5 Absolute Maximum Ratings

■ **EM78P157N**

Items	Rating
Temperature under bias	–40°C to 85°C
Storage temperature	–65°C to 150°C
Working voltage	2.5 to 5.5V
Working frequency	DC to 20MHz
Input voltage	Vss-0.3V to Vdd+0.5V
Output voltage	Vss-0.3V to Vdd+0.5V

6 Electrical Characteristics

6.1 DC Electrical Characteristic

(Ta=25 °C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FXT	XTAL: VDD to 3V	Two cycle with two clocks	DC		8.0	MHz
	XTAL: VDD to 5V	Two cycle with two clocks	DC		20.0	MHz
ERC	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	940	F±30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS			±1	μA
VIH1	Input High Voltage (VDD=5V)	Ports 5, 6	2.0			V
VIL1	Input Low Voltage (VDD=5V)	Ports 5, 6			0.8	V
VIHT1	Input High Threshold Voltage (VDD=5V)	/RESET, TCC(Schmitt trigger)	2.0			V
VILT1	Input Low Threshold Voltage (VDD=5V)	/RESET, TCC(Schmitt trigger)			0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	3.5			V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI			1.5	V
VIH2	Input High Voltage (VDD=3V)	Ports 5, 6	1.5			V
VIL2	Input Low Voltage (VDD=3V)	Ports 5, 6			0.4	V
VIHT2	Input High Threshold Voltage (VDD=3V)	/RESET, TCC(Schmitt trigger)	1.5			V
VILT2	Input Low Threshold Voltage (VDD=3V)	/RESET, TCC(Schmitt trigger)			0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	2.1			V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI			0.9	V
VOH1	Output High Voltage (Ports 5)	IOH = -12.0 mA	2.4			V
VOH1	Output High Voltage (Ports 6) (Schmitt trigger)	IOH = -12.0 mA	2.4			V
VOL1	Output Low Voltage(Port5)	IOL = 12.0 mA			0.4	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOL1	Output Low Voltage (Ports 6) (Schmitt trigger)	IOL = 12.0 mA			0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–50	–70	–240	μA
IPD	Pull-down current	Pull-down active, input pin at VDD	25	50	120	μA
ISB_1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled		1	2	μA
ISB_2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled			15	μA
ICC1	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled	15	20	30	μA
ICC2	Operating supply current (VDD=3V) at two cycles/four clocks	/RESET= 'High', Fosc=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled		25	35	μA
ICC3	Operating supply current (VDD=5.0V) at two cycles/two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled			2.0	mA
ICC4	Operating supply current (VDD=5.0V) at two cycles/four clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled			4.0	mA

6.2 AC Electrical Characteristics

(Ta=25 °C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time		11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

*N = selected prescaler ratio

6.3 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown herein for reference purposes only and are not guaranteed for its accuracy. In some graphs, the data may be out of the specified warranted operating range.

6.3.1 Port 6 Vih/Vil vs. VDD (Input Pin with Schmitt Inverter)

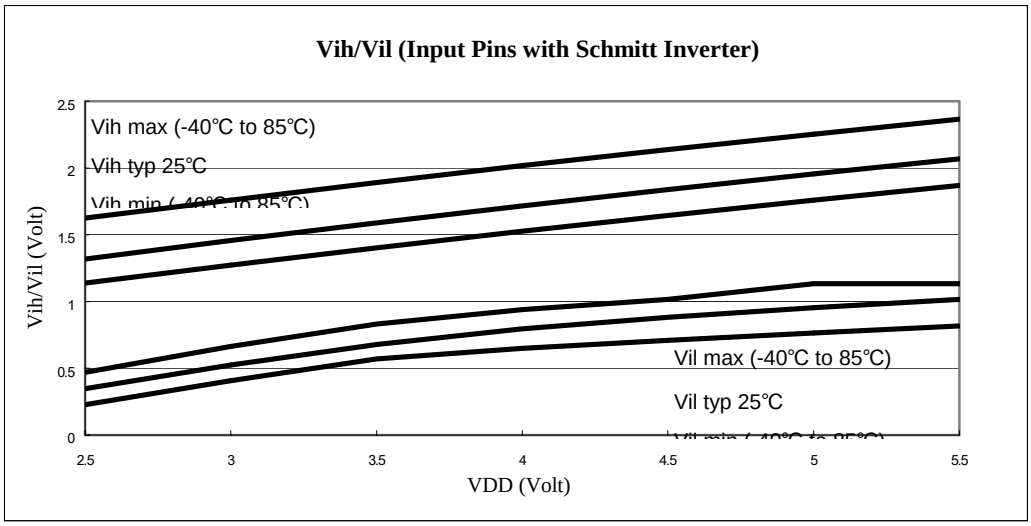


Fig. 6-1 Graph on Port 6 Vih/Vil vs. VDD

6.3.2 Port 5 Input Threshold Voltage (Vth) vs. VDD

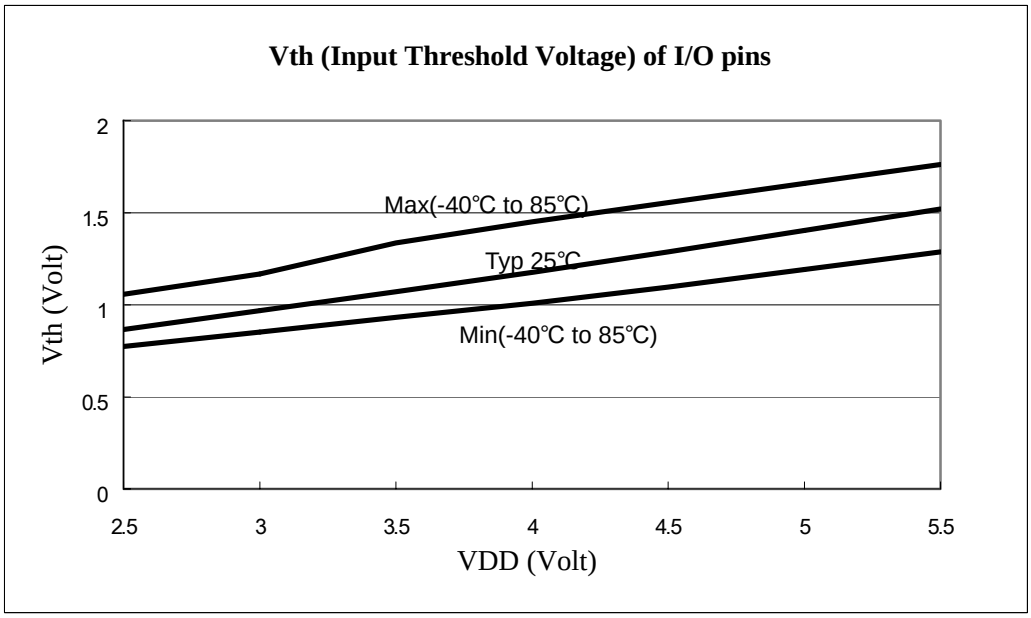


Fig. 6-2 Graph on Port 5 Input Threshold Voltage (Vth) vs. VDD

6.3.3 Ports 5 & Port 6 Voh vs. Ioh, VDD=5V and 3V

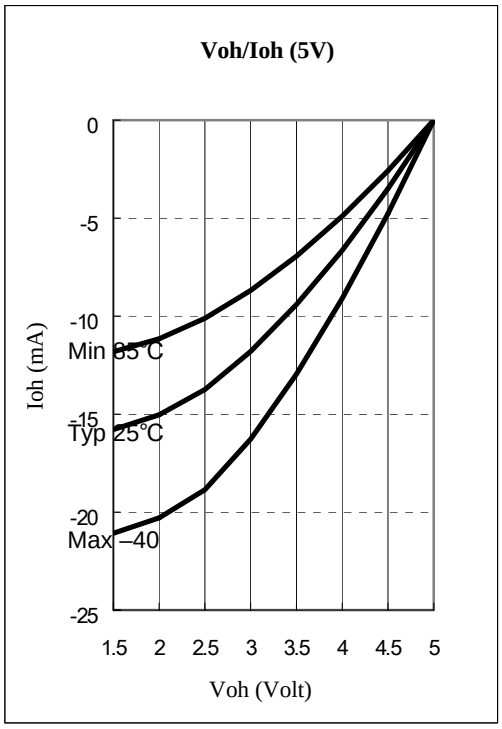


Fig. 6-3 Graph on Ports 5 & 6 Voh vs. Ioh, VDD=5V

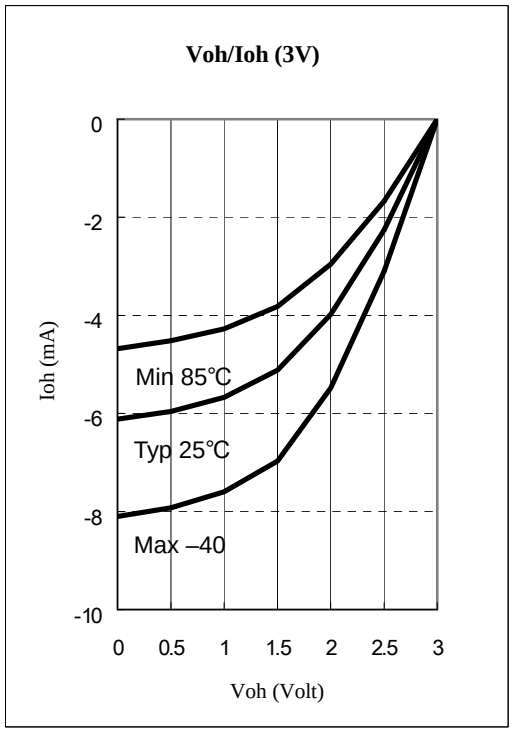


Fig. 6-4 Graph on Ports 5 & 6 Voh vs. Ioh, VDD=3V

6.3.4 Ports 5 & Port 6 Vol vs. Iol, VDD=5V and 3V

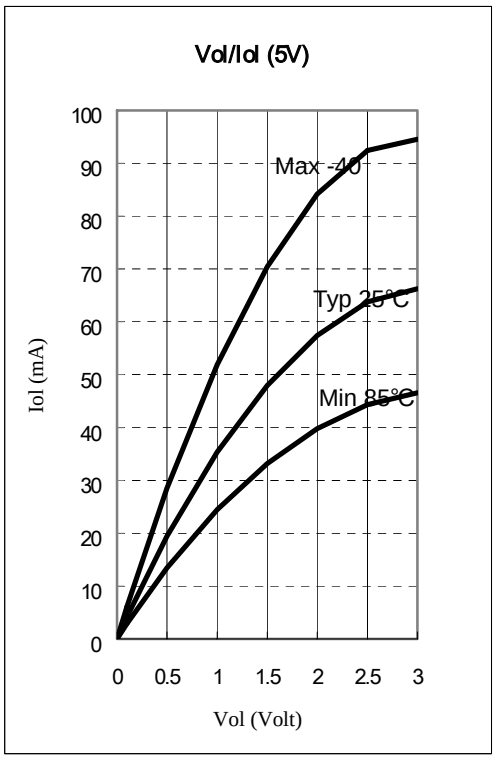


Fig. 6-5 Graph on Ports 5 & 6 Vol vs. Ioh, VDD=5V

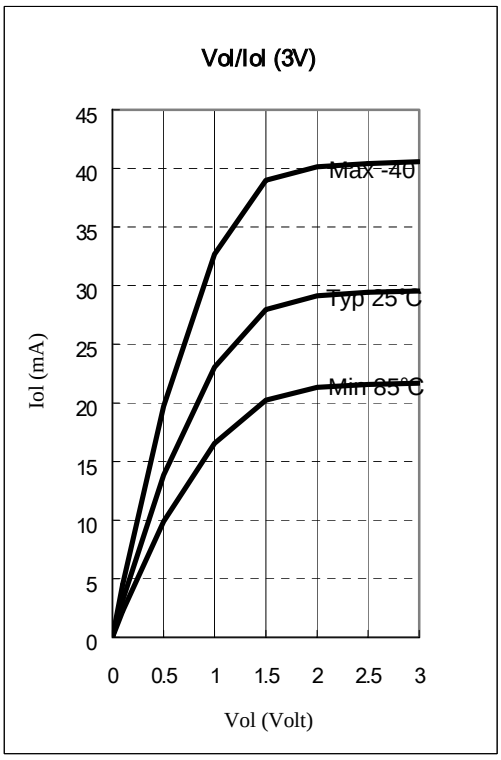


Fig. 6-6 Graph on Ports 5 & 6 Voh vs. Iol, VDD=3V

6.3.5 WDT Time Out Period vs. VDD (Prescaler Set to 1:1)

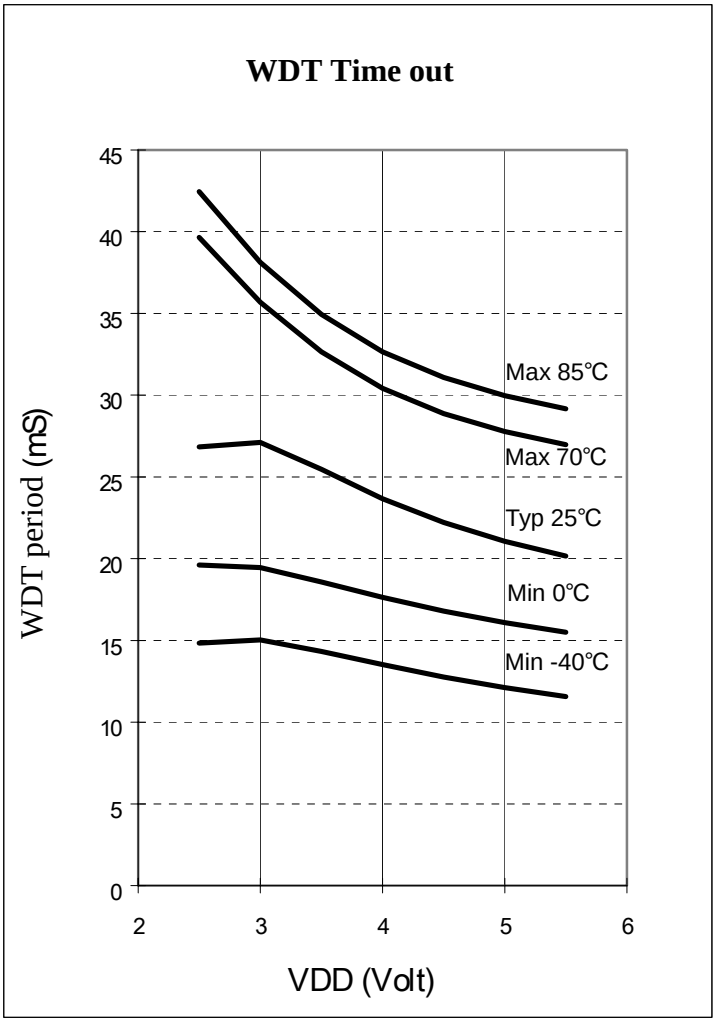


Fig. 6-7 Graph on WDT Time Out Period vs. VDD (Perscaler Set to 1:1)

6.3.6 Typical RC OSC Frequency vs. VDD (Cext = 100pF, Temp. = 25°C)

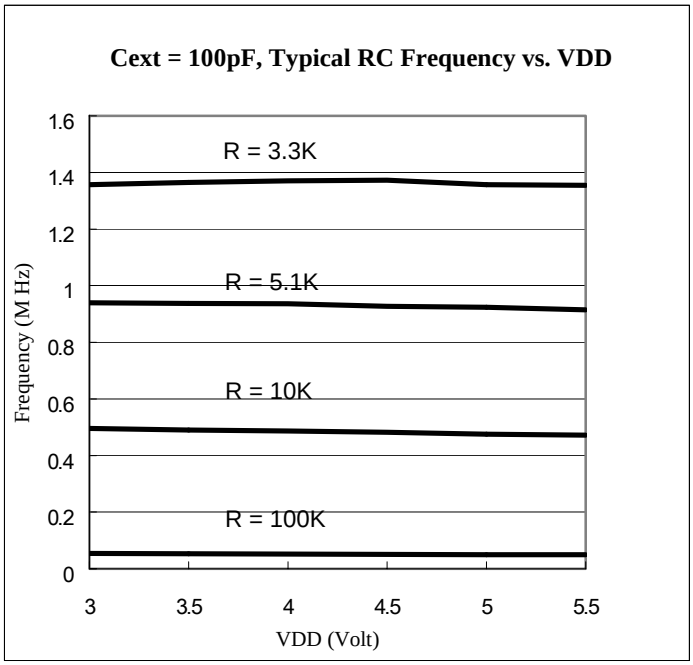


Fig. 6-8 Graph on Typical RC OSC Frequency vs. VDD (Cext = 100pF, Temperature at 25°C)

6.3.7 Typical RC OSC Frequency vs. VDD (with R and C under Ideal Conditions)

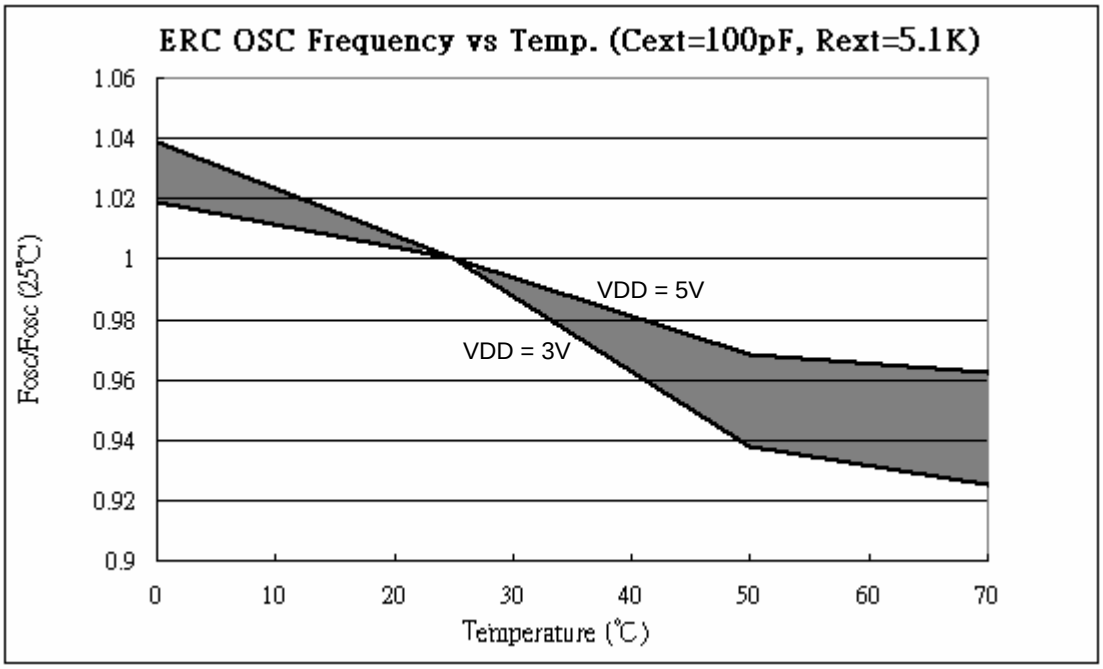


Fig. 6-9 Graph on Typical RC OSC Frequency vs. VDD (with R & C under Ideal Conditions)

6.3.8 Typical and Maximum Operating Current (ICC1/2/3/4) vs. Temperature

The following four conditions exist with the Operating Current ICC1 to ICC4:

- ICC1: VDD=3V, Fosc=32K Hz, 2 clocks, WDT disabled
- ICC2: VDD=3V, Fosc=32K Hz, 2 clocks, WDT enabled
- ICC3: VDD=5V, Fosc=4M Hz, 2 clocks, WDT enabled
- ICC4: VDD=5V, Fosc=10M Hz, 2 clocks, WDT enabled

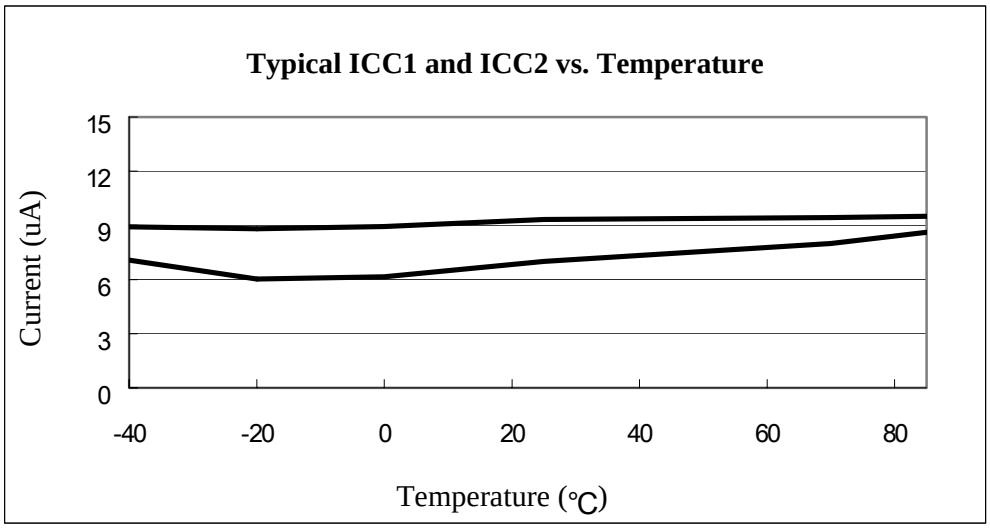


Fig. 6-10 Graph on Typical Operating Current (ICC1 and ICC2) vs. Temperature

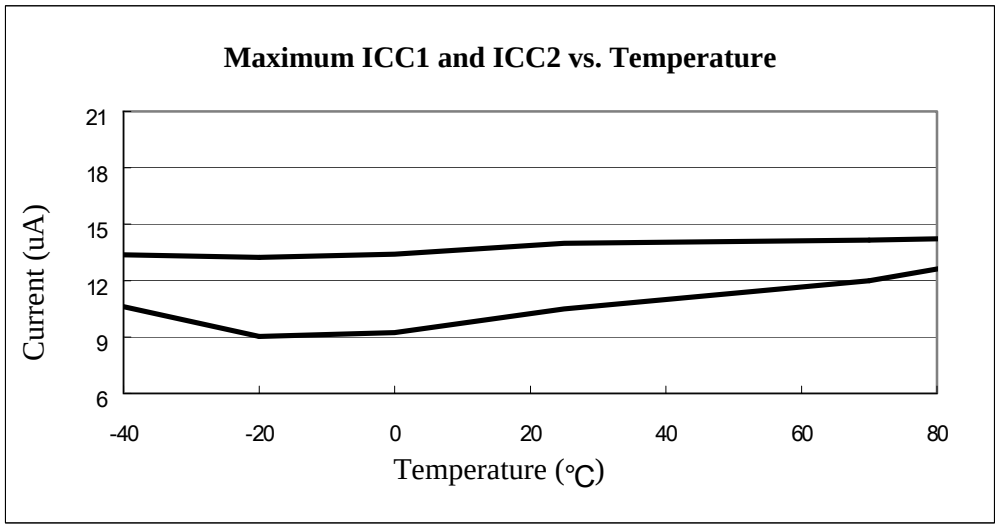


Fig. 6-11 Graph on Maximum Operating Current (ICC1 and ICC2) vs. Temperature

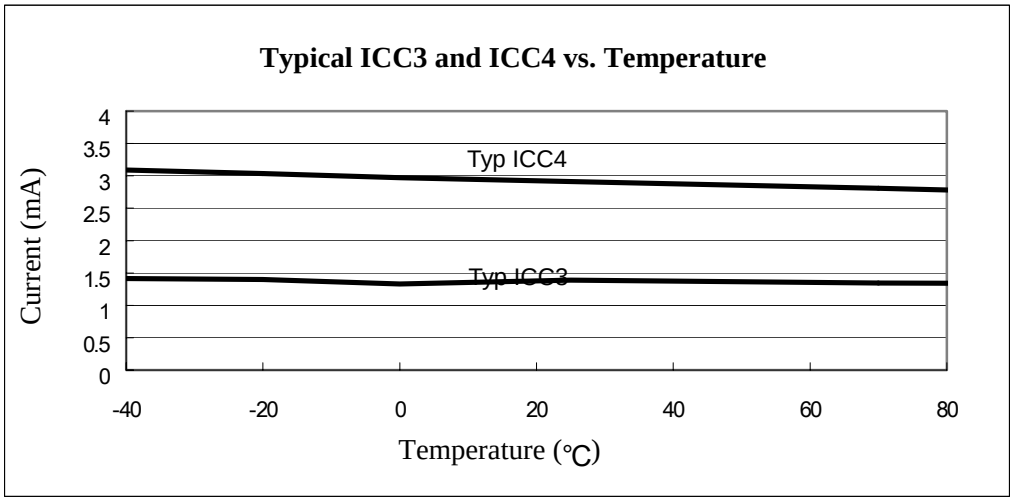


Fig. 6-12 Graph on Typical Operating Current (ICC3 and ICC4) vs. Temperature

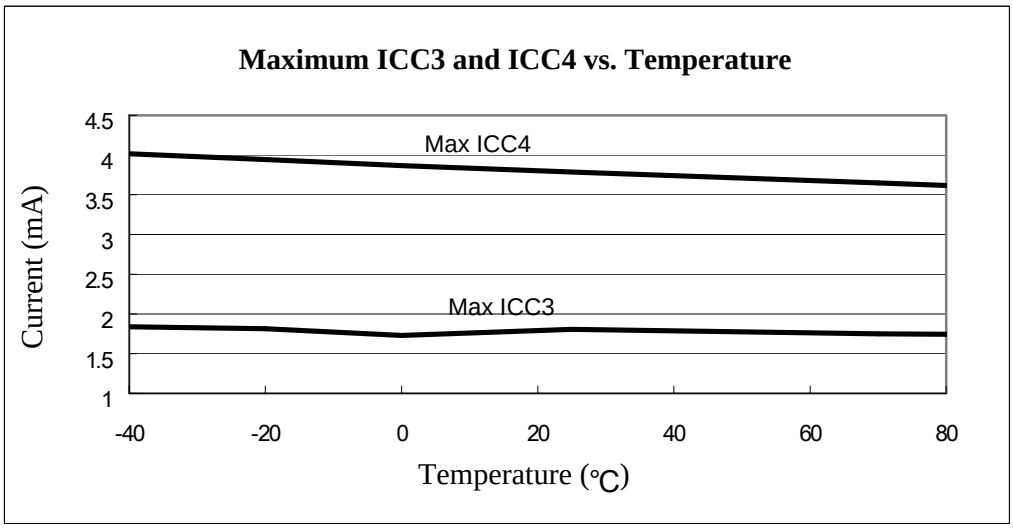


Fig. 6-13 Graph on Maximum Operating Current (ICC3 and ICC4) vs. Temperature

6.3.9 Typical and Maximum Standby Current (ISB1 and ISB2) vs. Temperature

The following two conditions exist with the Standby Current ISB1 and ISB2:

- ISB1: VDD=5V, WDT disabled
- ISB2: VDD=5V, WDT enabled

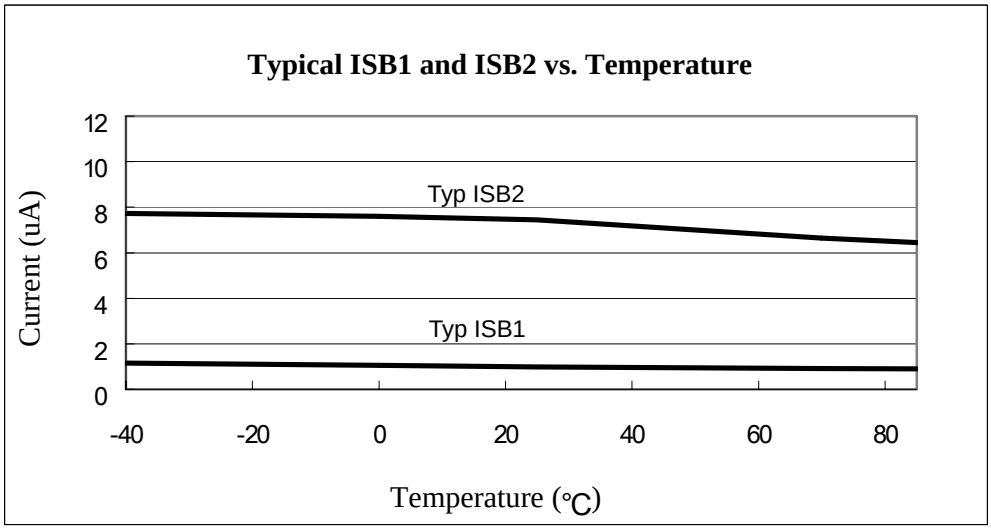


Fig. 6-14 Graph on Typical Standby Current (ISB1 and ISB2) vs. Temperature

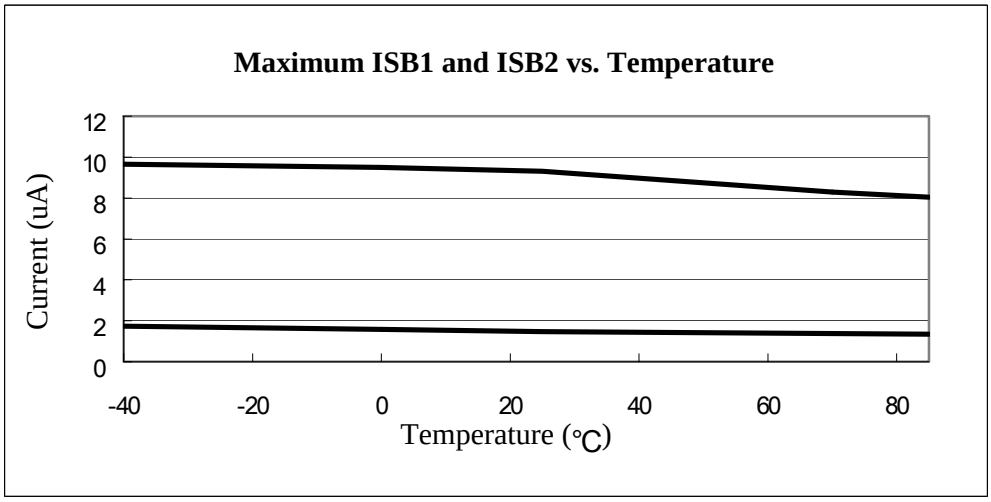


Fig. 6-15 Graph on Maximum Standby Current (ISB1 and ISB2) vs. Temperature

6.3.10 Operating Voltage under Temperature Range of 0℃ to 70℃ and –40℃ to 85℃

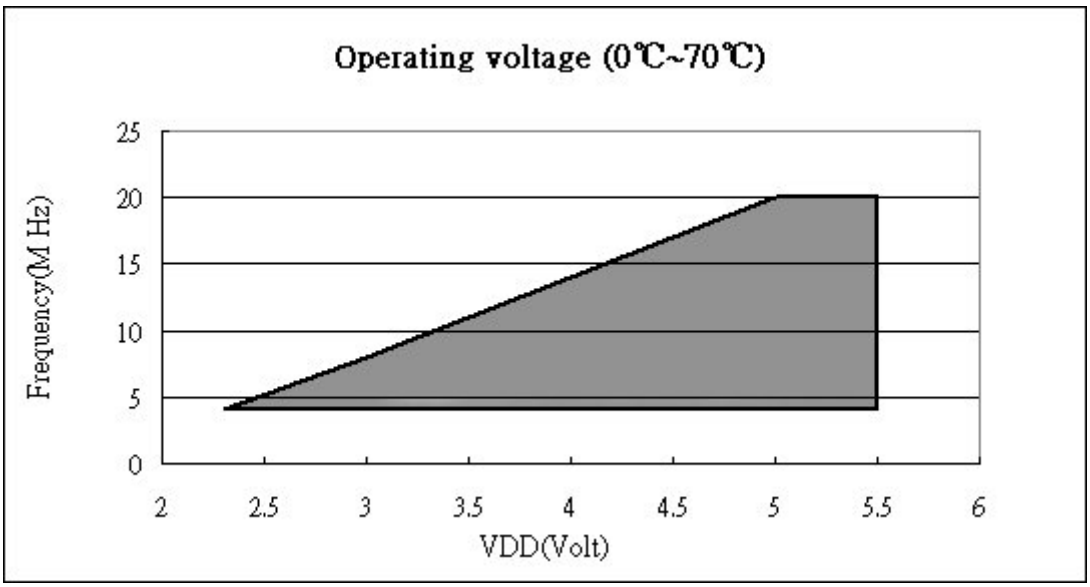


Fig. 6-16 Graph on Operating Voltage under Temperature Range of 0℃ to 70℃

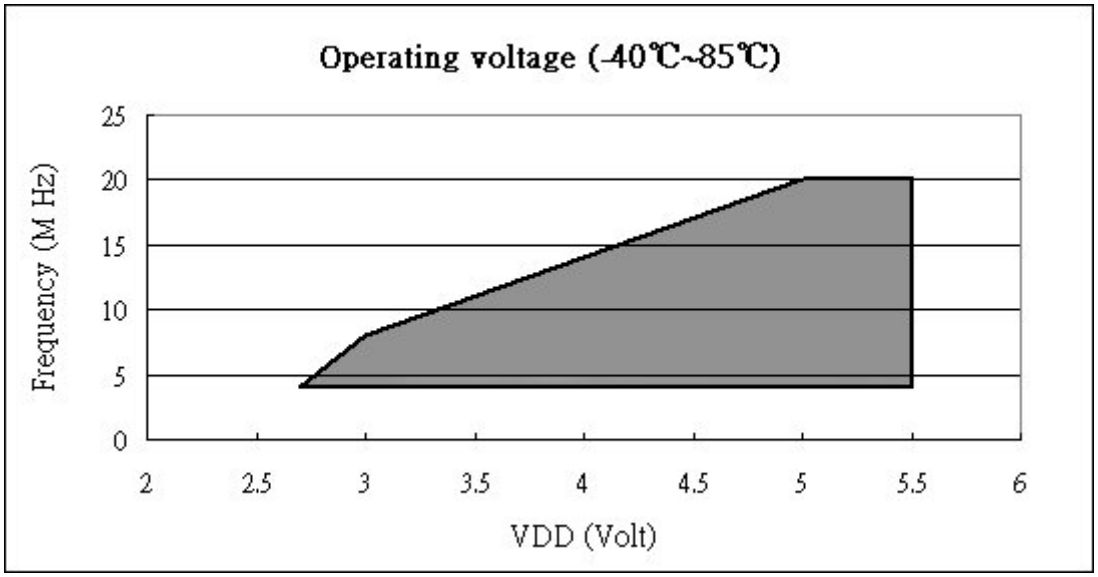


Fig. 6-17 Graph on Operating Voltage under Temperature Range of –40℃ to 85℃

6.3.11 Operating Current Range (Based on High and Low Freq. @ =25℃) vs. Voltage

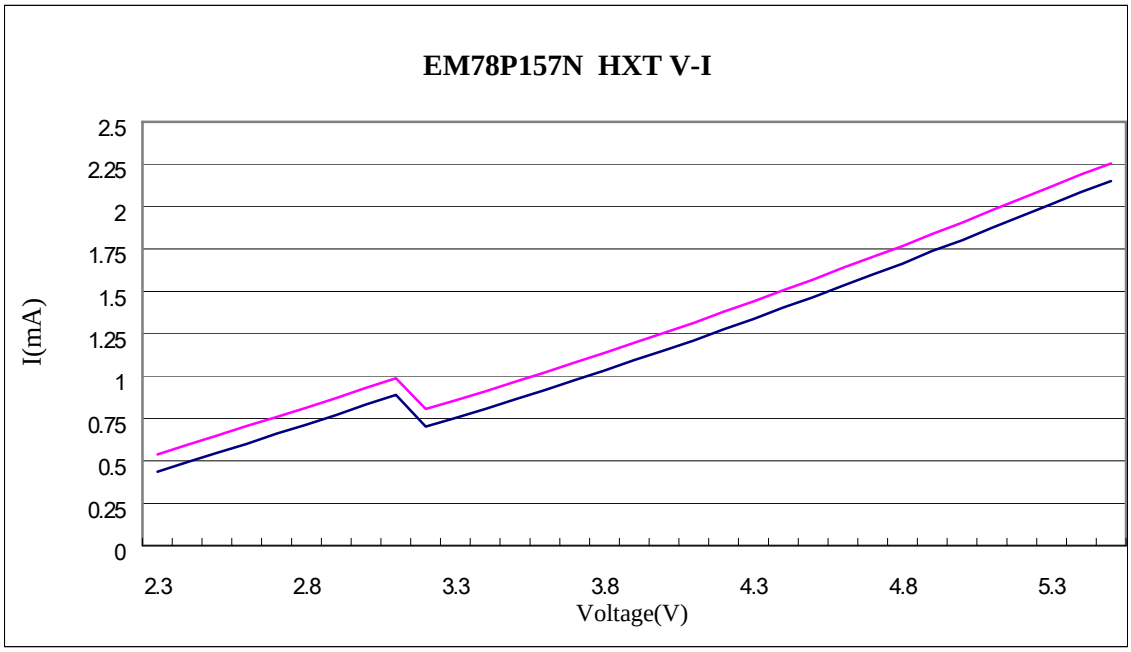


Fig. 34 Operating Current Range (Based on High Freq. @ =25℃) vs. Voltage

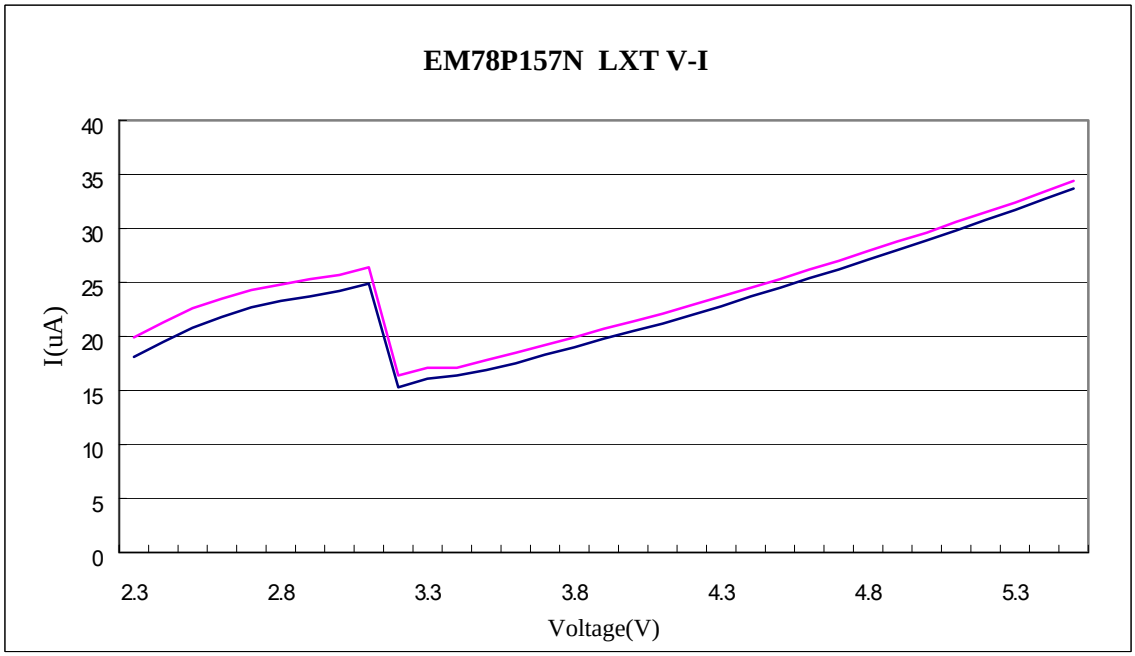


Fig. 35 Operating Current Range (Based on Low Freq. @ =25℃) vs. Voltage

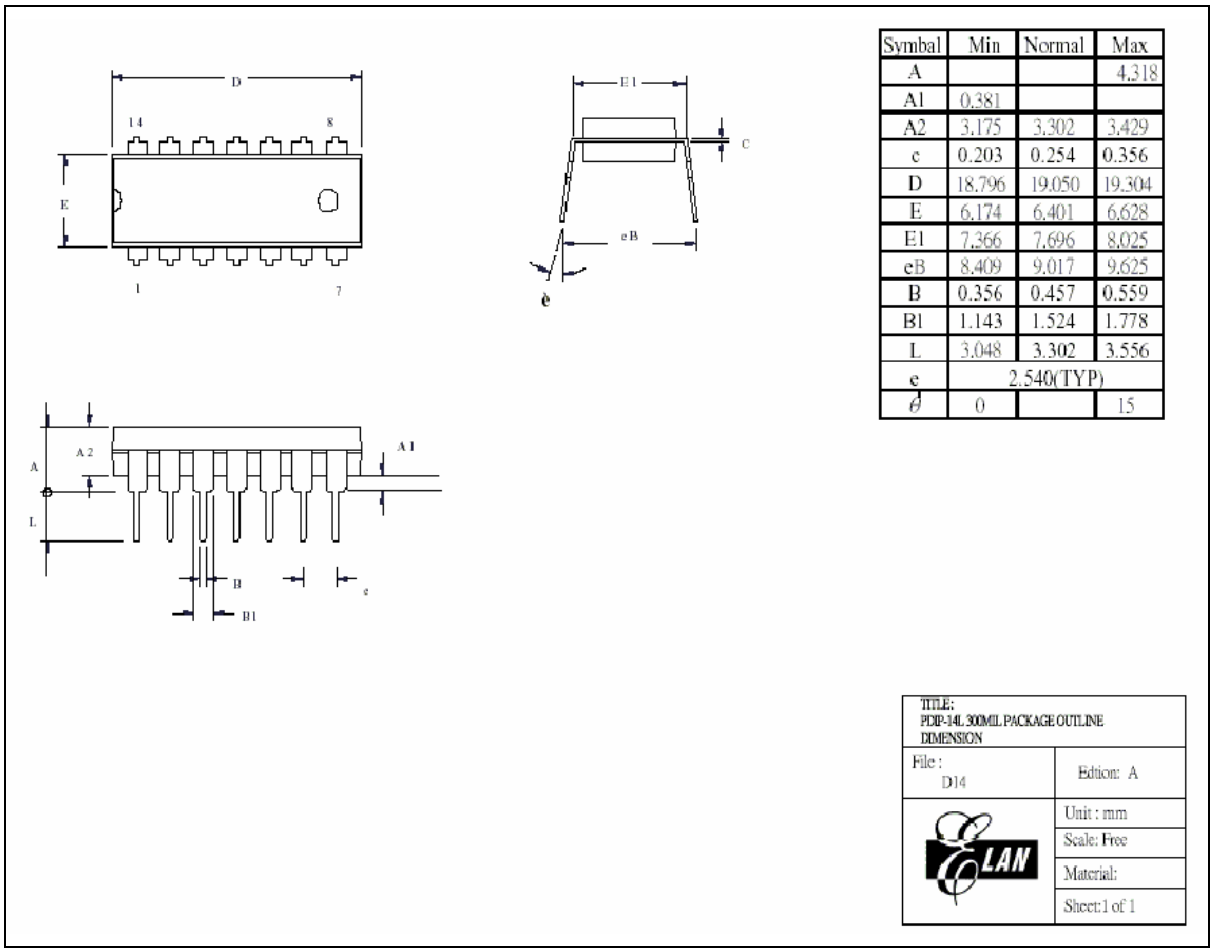
APPENDIX

A Package Types

OTP MCU	Package Type	Pin Count	Package Size
EM78P157NBP	DIP	14	300 mil
EM78P157NBM	SOP	14	150 mil
EM78P157NAP	DIP	18	300 mil
EM78P157NAM	SOP	18	300 mil
EM78P157NAAS	SSOP	20	209 mil
EM78P157NAKM	SSOP	20	209 mil

A.1 Package Detailed Information

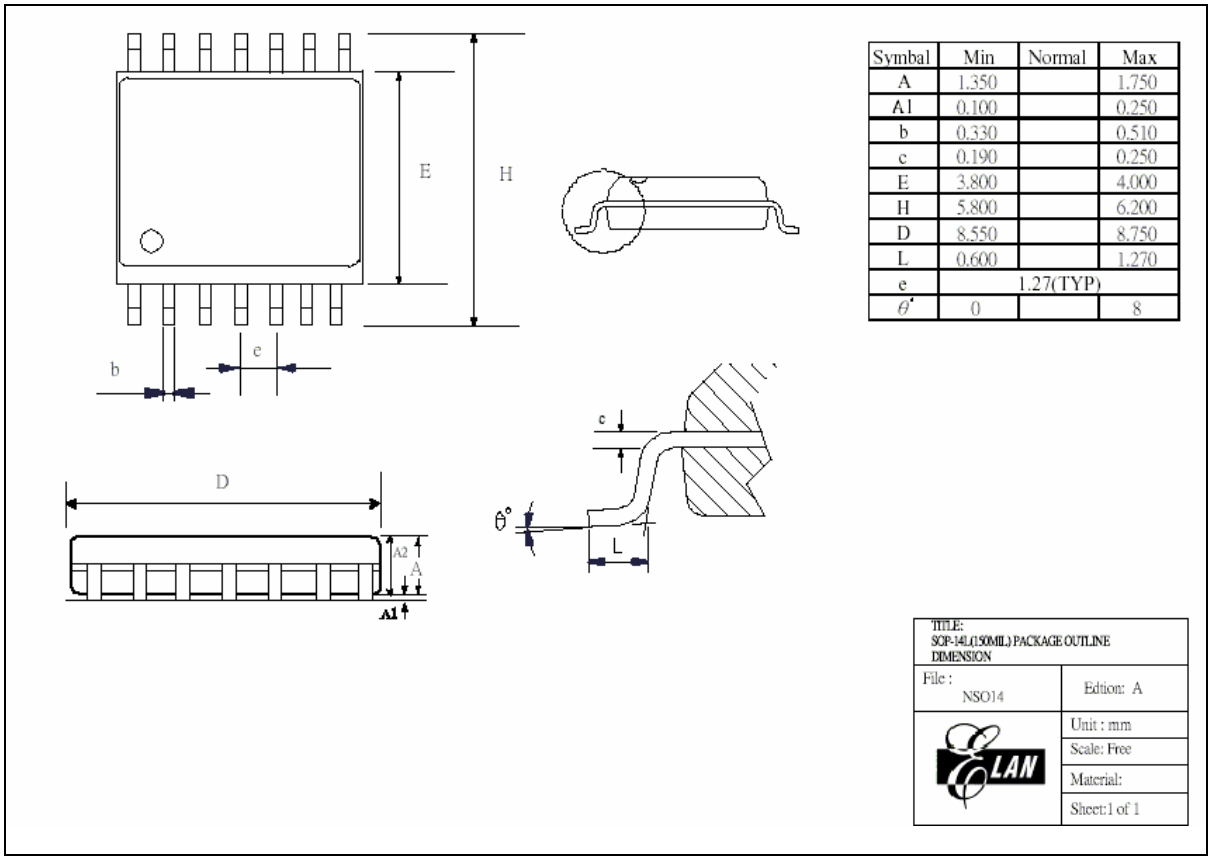
A.1.1 14-Lead Plastic Dual in line (PDIP) — 300 Mil



Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-14L 300MIL PACKAGE OUTLINE DIMENSION	
File : D14	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet 1 of 1

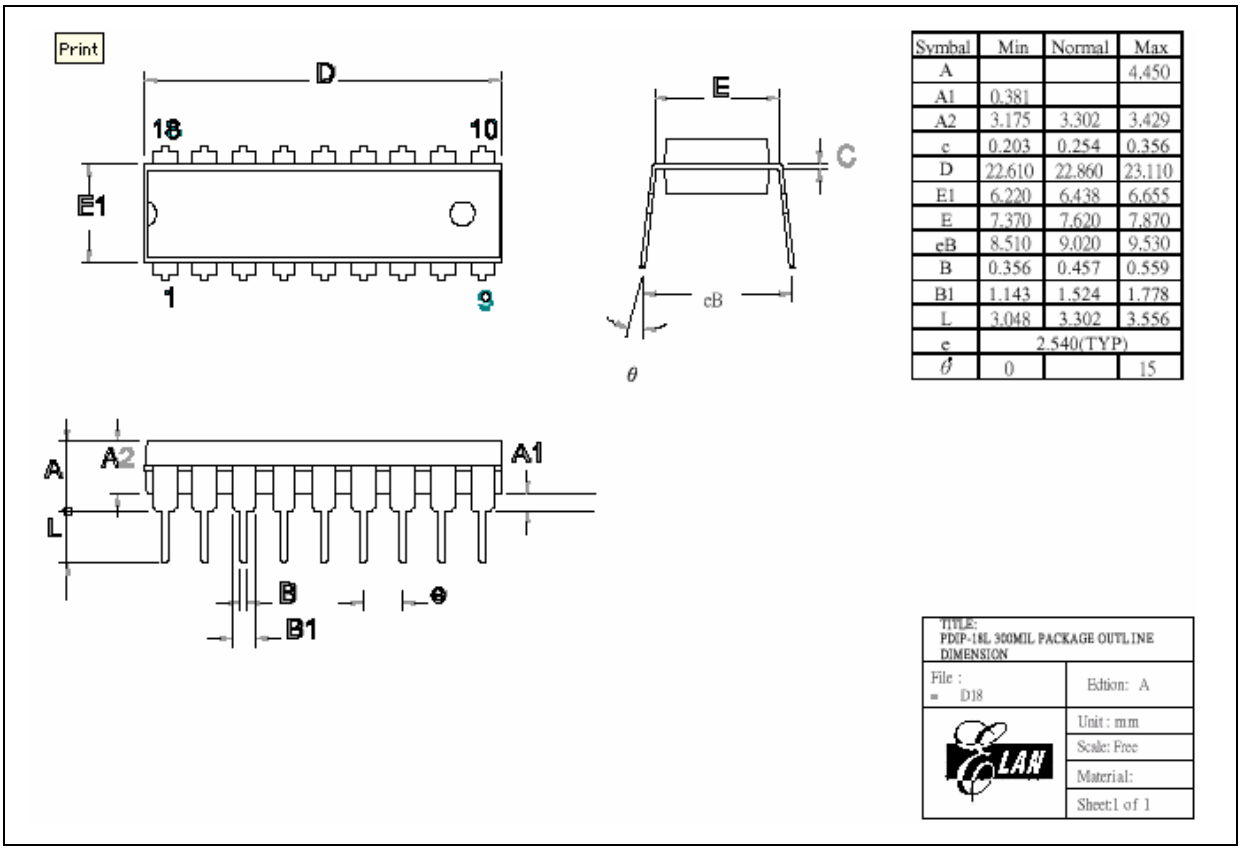
A.1.2 14-Lead Plastic Small Outline (SOP) — 150 Mil



Symbal	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION	
File : NSO14	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

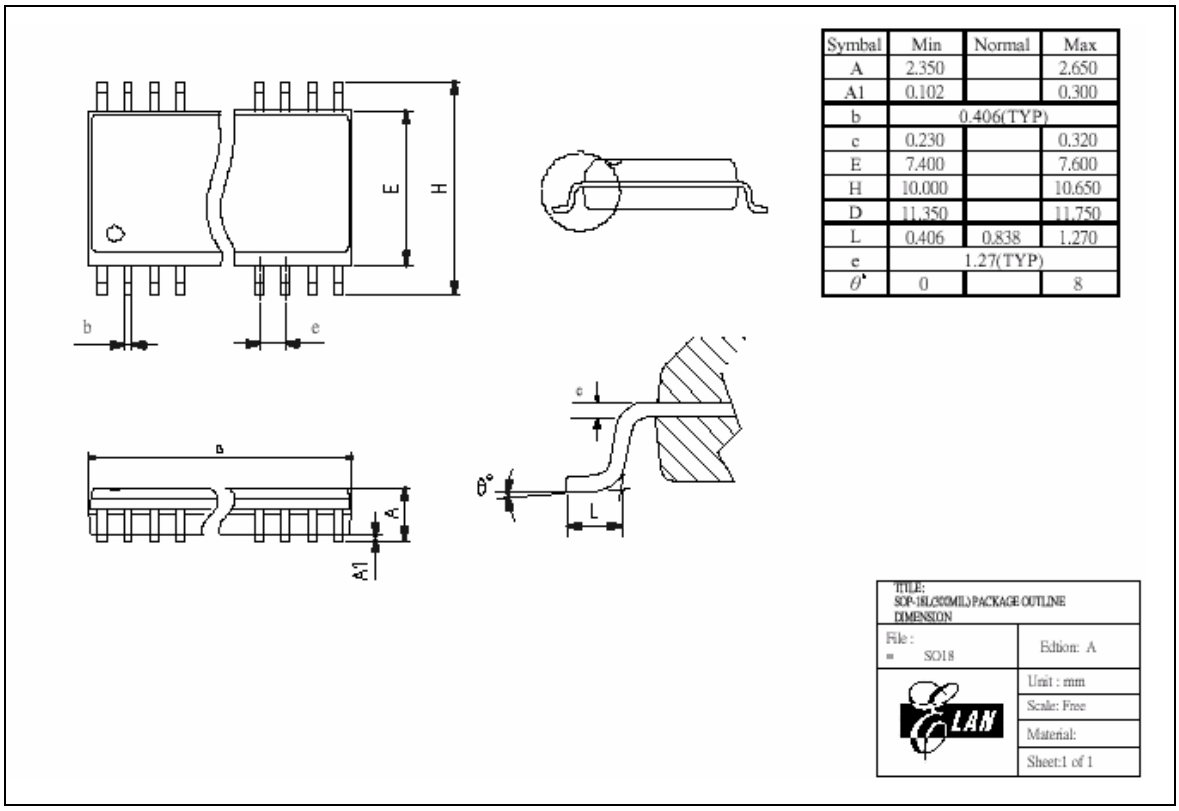
A.1.3 18-Lead Plastic Dual in Line (PDIP) — 300 Mil



Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-18L 300MIL PACKAGE OUTLINE DIMENSION	
File : D18	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

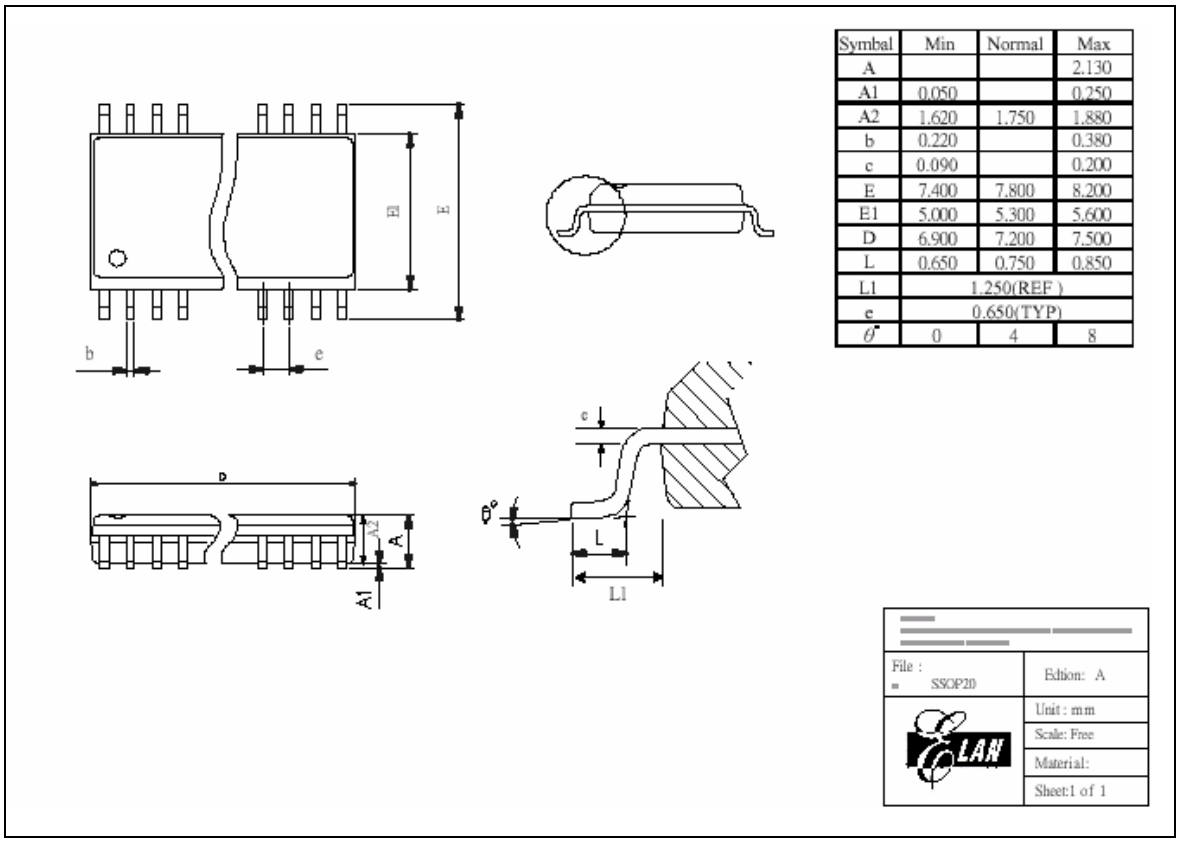
A.1.4 18-Lead Plastic Small Outline (SOP) — 300 Mil



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27(TYP)		
θ°	0		8

TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION	
File : = SO18	Edition: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

A.1.5 20-Lead Plastic Small Outline (SSOP) — 209 Mil



Symbal	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ°	0	4	8

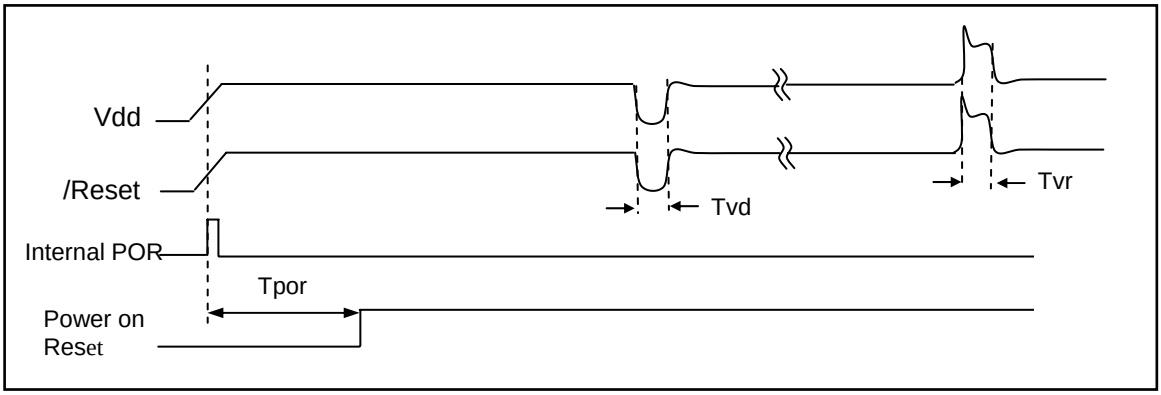
File : SSOP20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

B Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5℃，for 5 seconds up to the stopper using a rosin-type flux	
Pre-condition	Step1: TCT ，65℃(15mins)~150℃(15mins)，10 cycles	For SMD IC(such as SOP, QFP, SOJ, etc.)
	Step2: bake 125℃，TD(durance)=24 hrs	
	Step3:soak 30°C /60%，TD(durance)=192hrs	
	Step4:IR flow 3cycles (Pkg thickness≧2.5mm or Pkg volume≧350mm3 ----225±5℃) (Pkg thickness≦2.5mm or Pkg volume≦350mm3 ----240±5℃)	
Temperature cycle test	–65℃(15mins)~150℃(15mins) , 200 cycles	
Pressure cooker test	TA =121℃,RH=100%,pressure=2atm, TD(durance)= 96 Hrs	
High temperature /high humidity test	TA=85℃ , RH=85% , TD(durance)=168 ,500 Hrs	
High-temperature storage life	TA=150℃, TD(durance)=500,1000Hrs	
High-temperature operating life	TA=125 ℃ , VCC=Max. operating voltage, TD(durance) =168,500,1000Hrs	
Latch-up	TA=25℃, VCC=Max. operating voltage, 150mA/20V	
ESD(HBM)	TA=25℃, ≧|±3KV|	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-)mode
ESD(MM)	TA=25℃, ≧|±300V|	

C Address Trap Detect

An address trap detect is one of the fail-safe function that detects CPU malfunction caused by noise or the like. If the CPU attempts to fetch an instruction from a part of RAM, an internal recovery circuit will auto started. Until CPU got the correct function, it will execute the next program that follows.



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tpor	Power on reset time	Vdd = 5V, -40℃ to 85℃	**10.5**	**16.8**	**22**	ms
Tvd	Vdd Voltage drop time	Vdd = 5V, -40℃ to 85℃	-	-	1*	us
Tvr	Vdd Voltage rise time	Vdd = 5V, -40℃ to 85℃	-	-	1**	us

* Tvd is the period of Vdd voltage less than POR voltage 1.9 volts.
** Tvr is the period of Vdd voltage higher than 5.5 volts.