Design Idea DI-37
DPA-Switch™
16.5 W DC-DC Converter

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Telecom	DPA424R	16.5 W	36-75 VDC	3.3 V	Forward Sync. Rec.

Design Highlights

- Low cost
- 400 kHz synchronous rectification design
- Low component count
- Efficiency – 87% at 48 VDC
- No current sense resistor or current transformer required
- Output overload, open loop and thermal protection
- Integrated UV meets ETSI standard

Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. Resistor R1 programs the under/over voltages and linearly reduces the maximum duty cycle with input voltage to prevent core saturation during load transients. Resistor R3 programs the *DPA-Switch* current limit to 60% of nominal to limit fault and overload power. Drain voltage clamping is provided by Zener diode VR1. Transformer core reset is controlled by the gate capacitance of Q1.

Resistor R15 charges the gate of Q2, the forward synchronous rectifier MOSFET. The catch synchronous rectifier MOSFET (Q1) is directly driven by the transformer (T1) reset voltage and operates only when Q2 is off. Diode D2 provides a conduction path for the output inductor (L2) current when the transformer reset is complete.

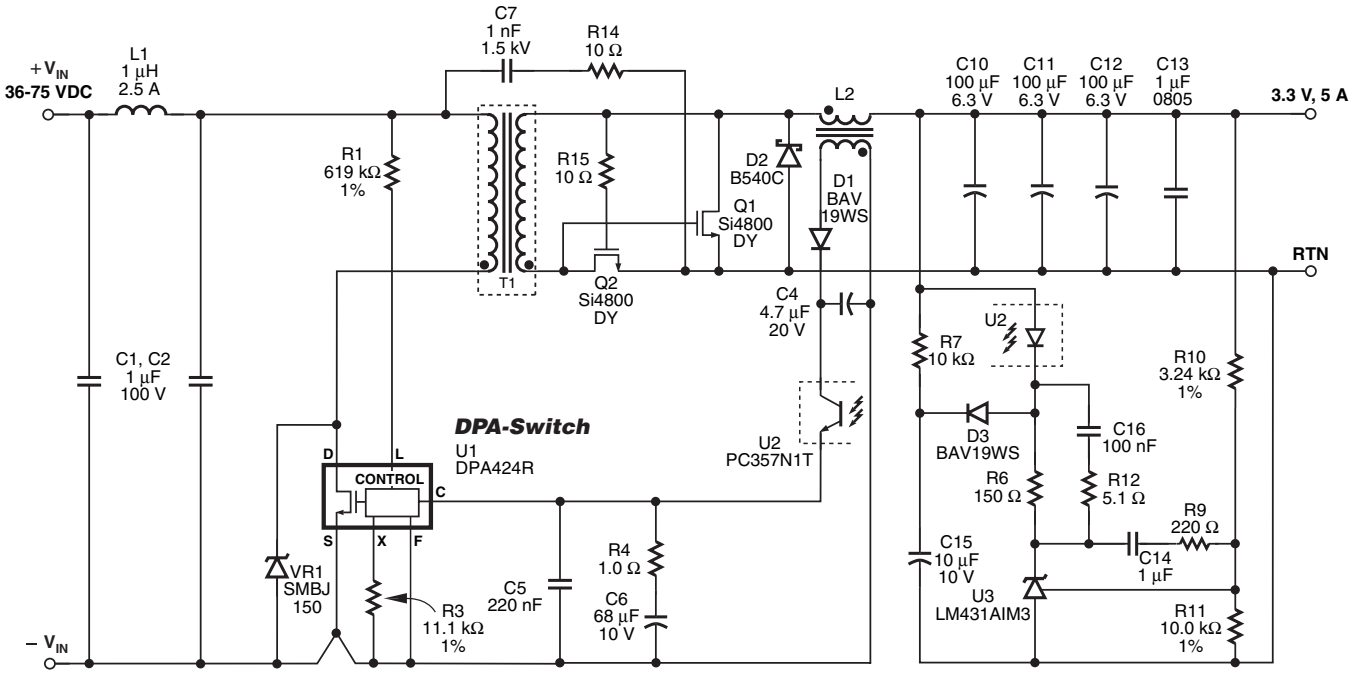

Figure 1. DPA424R–16.5 W, 3.3 V, 5 A DC-DC Converter.

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Key Design Points

- Transformer core reset is critical in this design. MOSFET gate loading will affect the transformer reset waveform. Capacitor C_{Q1gs} will load transformer reset. Choose Q1 MOSFET such that C_{Q1gs} provides sufficient reset at low line and safe maximum drain voltage at high line.
- Choose synchronous rectifier MOSFETs which have both low $R_{DS(ON)}$ and also low Q_g (combination of gate charge Q_{gs} and Miller capacitance Q_{gd}).
- Reduce transformer leakage inductance by filling each winding layer across the entire width of the bobbin.
- Choose a low-drop Schottky diode (such as Vishay SL44 – V_f = 0.42 V), to increase high line efficiency.
- Choose a larger *DPA-Switch* to increase efficiency at low and medium input voltages.

TRANSFORMER PARAMETERS	
Core Material	Epcos P/N: P 14 x 8 N87, ungapped
Bobbin	8-pin P 14 x 8 surface mount bobbin
Winding Details	Primary 10T + 10T, 1 x 26 AWG 3.3 V, 4 x 26 AWG
Winding Order and Pin Numbers	Primary-1 (4-NC), 3.3 V (5-6), Primary-2 (NC-1)
Primary Inductance	600 µH ±25% at 400 kHz
Primary Resonant Frequency	3.8 MHz (minimum)
Leakage Inductance	1 µH (maximum)

Table 1. Transformer Design Parameters.

INDUCTOR PARAMETERS	
Core Material	Epcos P/N: P 14 x 8 N87, gap for inductor
Bobbin	8-pin P 14 x 8 surface mount bobbin
Winding Details	Main 10T, 2 x 24 AWG Bias 30T, 1 x 32 AWG
Winding Order and Pin Numbers	Main (7,8-5,6) Bias (1-2)
Inductance	Pin (7,8-5,6): 16 µH ±10% at 400 kHz

Table 2. Inductor Design Parameters.

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