4,6 & 8 Channel ESD Protection Arrays with Zener Supply Clamp

Features

- Four, six or eight channels of ESD protection for high data rate signals
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- ±15 kV contact, ±15 kV air ESD protection per channel (IEC 61000-4-2 standard)
- Low loading capacitance of 6pF typical
- Low supply current
- Available in miniature MSOP and SOIC packages
- Lead-free versions available

Applications

- ESD protection for a variety of electronic equipment
- Set Top Boxes
- Digital TVs
- I/O & VGA Port protection
- Desktop and Notebook computers
- PDAs
- Cellular Phones

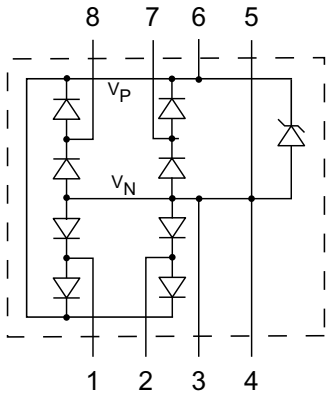
Product Description

The CM1209 family of diode arrays are designed to provide either 4, 6 or 8 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steer the ESD current pulse either to the positive (V_P) or negative (V_N) supply. In addition, there is an integral Zener diode between V_P and V_N to suppress any voltage disturbance due to these ESD current pulses. The CM1209 devices will protect against ESD pulses up to 15kV contact discharge per the International Standard IEC61000-4-2.

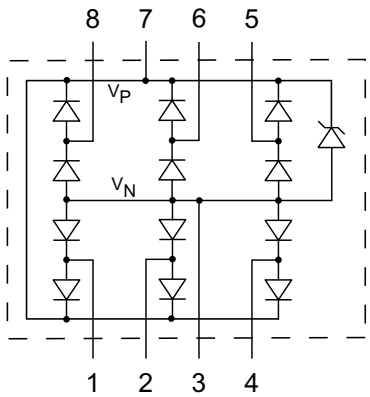
These devices are particularly well-suited for portable electronics (e.g. cellular phones, PDAs, notebook computers) because of its small package footprint, high ESD protection level, and low loading capacitance. They are also suitable for protecting video output lines and I/O ports in computers, set top boxes, digital TVs and peripheral equipment.

The CM1209 family of devices is optionally available with lead-free finishing.

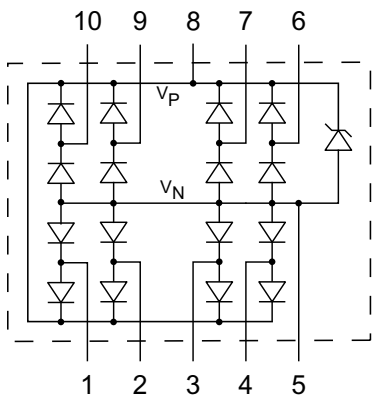
Electrical Schematics



CM1209-04
4-Channel

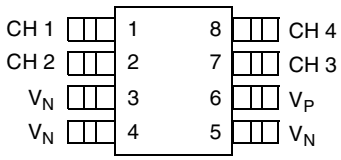


CM1209-06
6-Channel

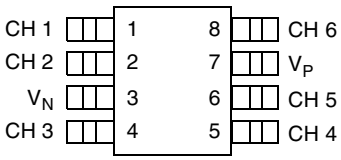


CM1209-08
8-Channel

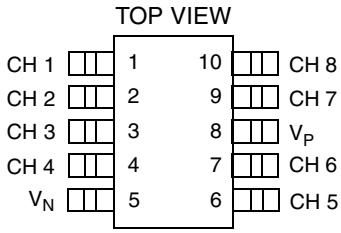
PACKAGE / PINOUT DIAGRAMS



8-pin MSOP
CM1209-04MS/MR



8-pin SOIC/MSOP
CM1209-06SN/SM
CM1209-06MS/MR



10-pin MSOP
CM1209-08MS/MR

Note: These drawings are not to scale.

PIN DESCRIPTIONS

	CM1209-04	CM1209-06	CM1209-08		
NAME	**PIN NO.**	**PIN NO**	**PIN NO**	**TYPE**	**DESCRIPTION**
CH 1	1	1	1	I/O	ESD Channel 1
CH 2	2	2	2	I/O	ESD Channel 2
CH 3	7	4	3	I/O	ESD Channel 3
CH 4	8	5	4	I/O	ESD Channel 4
CH 5		6	6	I/O	ESD Channel 5
CH 6		8	7	I/O	ESD Channel 6
CH 7			9	I/O	ESD Channel 7
CH 8			10	I/O	ESD Channel 8
V_N	3,4,5	3	5	GND	Negative voltage supply rail or ground reference rail.
V_P	6	7	8	Supply	Positive voltage supply rail.

Ordering Information

PART NUMBERING INFORMATION						
			Standard Finish		Lead-free Finish	
# of Channels	Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
4	8	MSOP-8	CM1209-04MS	0904	CM1209-04MR	0914
6	8	SOIC-8	CM1209-06SN	CM1209-06S	CM1209-06SM	CM1209-06SM
6	8	MSOP-8	CM1209-06MS	0906	CM1209-06MR	0916
8	10	MSOP-10	CM1209-08MS	0908	CM1209-08MR	0918

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Supply Voltage (V_P - V_N)	6.0	V
Diode Forward DC Current (Note 1)	20	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	(V_N - 0.5) to (V_P + 0.5)	V
Package Power Rating SOIC Package MSOP Package	 350 200	 mW mW

Note 1: Only one diode conducting at a time.

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	°C
Operating Supply Voltage (V_P - V_N)	0 to 5.5	V

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS(SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_P	Supply Current	(V_P-V_N)=5.5V; T_A=25°C			10	µA
V_F	ESD Diode Forward Voltage	I_F = 20mA; T_A=25°C	0.65		0.95	V
V_{ZBD}	Zener Clamp Reverse Breakdown Voltage	At 1mA; T_A=25°C		7		V
I_{LEAK}	Channel Leakage Current	T_A=25°C		±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P=5V, via 10K; V_N=0V, V_{IN}=2.5V; Notes 2 and 6		6	8	pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input and V_P rail Contact discharge per IEC 61000-4-2 standard Air discharge per IEC 61000-4-2 standard	 Notes 2, 3, 5, and 6 Notes 2, 3, 5, and 6	 ±15 ±15			 kV kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	At 8kV ESD HBM; T_A=25°C; Notes 2, 4 and 6		 +12.5 - 5.1		 V V
Z_{POS}	Dynamic Resistance of Channel Input for Positive Transients	I = 1A; T_A=25°C; See Figure 2; Note 6 applies		0.70		Ω
Z_{NEG}	Dynamic Resistance of Channel Input for Negative Transients	I = 1A; T_A=25°C; See Figure 2; Note 6 applies		0.45		Ω

Note 1: All parameters specified at T_A=-40 to +85°C unless otherwise noted.
Note 2: These parameters guaranteed by design and characterization.
Note 3: From I/O pins to V_P or V_N only.
Note 4: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5KΩ, V_P = 5.0V, V_N grounded.
Note 5: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 5.0V, V_N grounded.
Note 6: These measurements performed with no external capacitor on V_P.

Performance Information

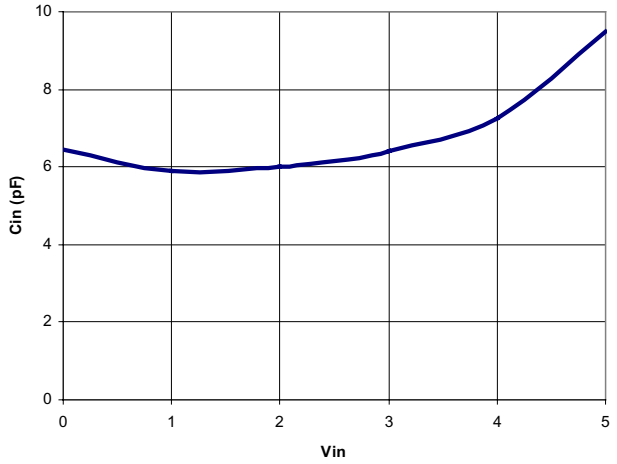


Figure 1. Typical Variation of Channel Input Capacitance (C_{IN}) vs. Channel Input Voltage (V_{IN})
(V_P = 5V via 10K resistor, V_N = 0V)

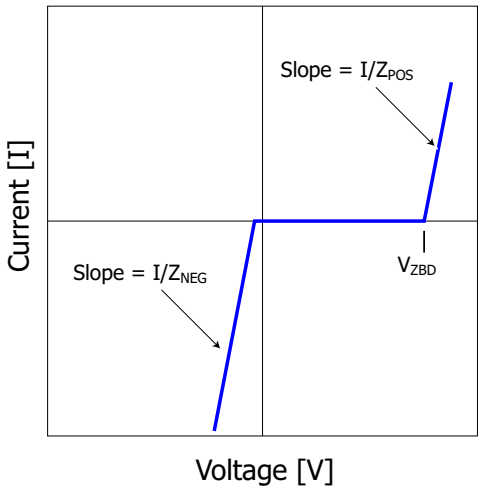
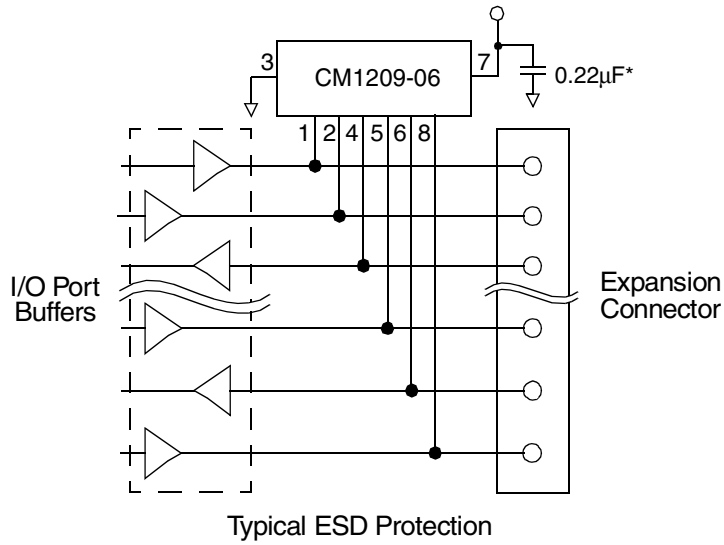


Figure 2. IV Curve for CM1209

Application Information



* Optional capacitor should be placed as close as possible to the V_P pin on all CM1209 devices. Refer to 'Design Considerations' text.

Figure 3. Application Example Using the CM1209-06 for I/O Port Protection

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 4, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1209 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22µF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See California Micro Devices Application Note AP209, “Design Considerations for ESD Protection", under Applications at www.calmicro.com.

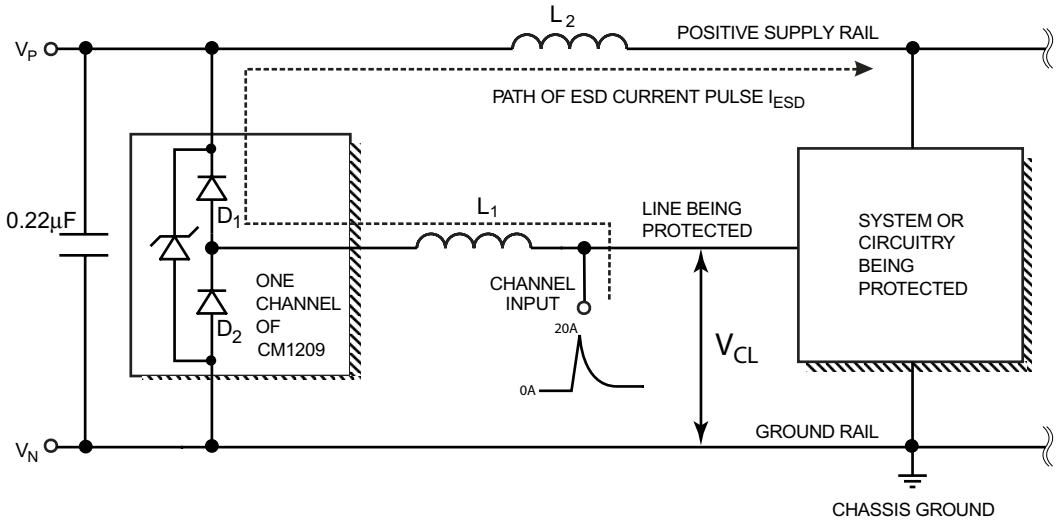


Figure 4. Application of Positive ESD Pulse between Input Channel and Ground

Mechanical Details

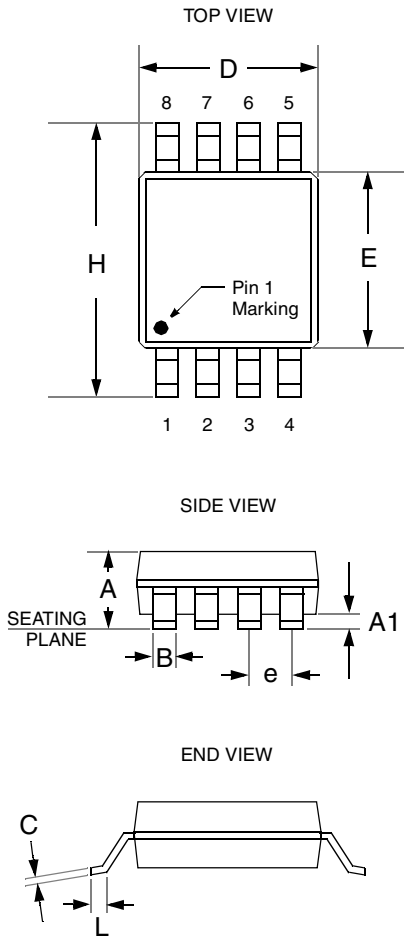
CM1209 devices are packaged in 8-pin and 10-pin MSOP and 8-pin SOIC packages. Dimensions for these packages are presented on the following pages. For complete information on the MSOP-8/-10 or SOIC-8 packages, see the specific California Micro Devices Package Information document.

MSOP-8 Mechanical Specifications

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.87	1.17	0.034	0.046
A1	0.05	0.25	0.002	0.010
B	0.30 (typ)		0.012 (typ)	
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.025 BSC	
H	4.78	4.98	0.188	0.196
L	0.52	0.54	0.017	0.025
# per tube	80 pieces*			
# per tape and reel	4000 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for MSOP-8

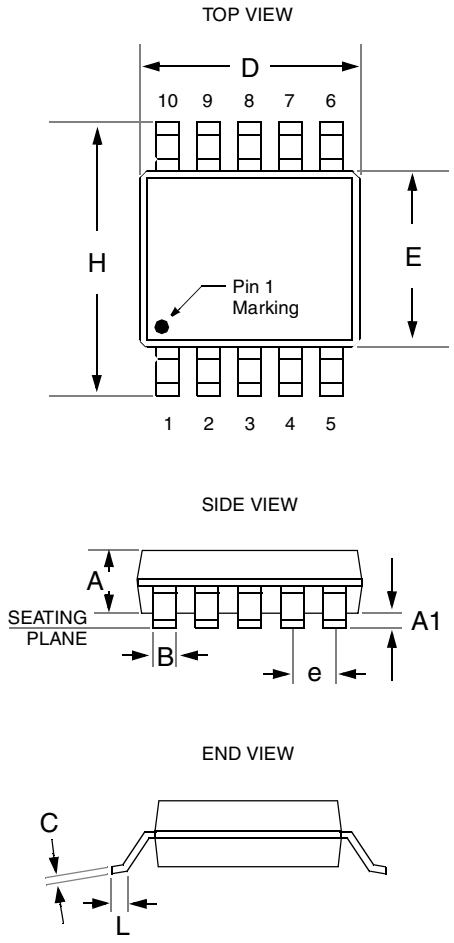
Mechanical Details (cont'd)

MSOP-10 Mechanical Specifications

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.18	0.40	0.006	0.016
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.76	5.00	0.187	0.197
L	0.40	0.70	0.0137	0.029
# per tube	80 pieces*			
# per tape and reel	4000			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for MSOP-10

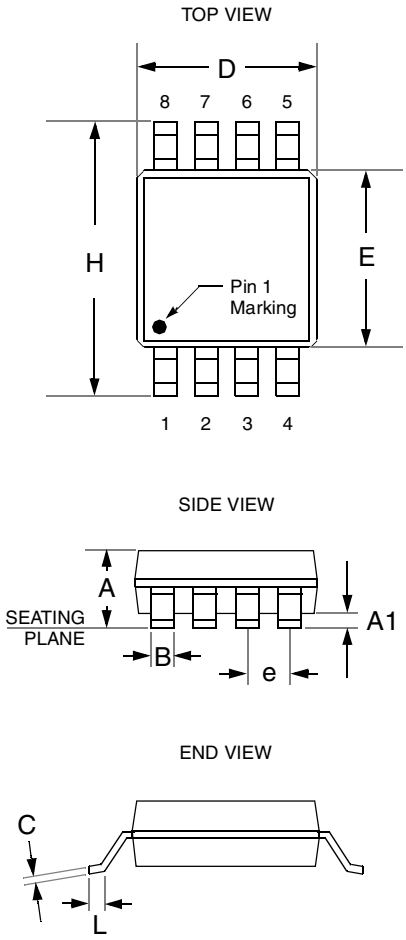
Mechanical Details (cont'd)

SOIC-8 Mechanical Specifications

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pcs*			
# per tape and reel	2500 pcs			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for SOIC-8