

DATA SHEET

74LVC1G66 Bilateral switch

Product specification
Supersedes data of 2002 Nov 15

2004 Apr 13

Bilateral switch

74LVC1G66

FEATURES

- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V.
- Switch handling capability of 32 mA
- High noise immunity
- CMOS low power consumption
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Direct interface TTL-levels
- Multiple package options
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74LVC1G66 is a high-speed Si-gate CMOS device.

The 74LVC1G66 provides an analog switch. The switch has two input/output pins (Y and Z) and an active HIGH enable input pin (E). When pin E is LOW, the analog switch is turned off.

QUICK REFERENCE DATA

Ground = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn-ON time E to V_{OS}	$C_L = 50$ pF; $R_L = 500$ Ω ; $V_{CC} = 3$ V	2.5	ns
		$C_L = 50$ pF; $R_L = 500$ Ω ; $V_{CC} = 5$ V	1.9	ns
t_{PHZ}/t_{PLZ}	turn-OFF time E to V_{OS}	$C_L = 50$ pF; $R_L = 500$ Ω ; $V_{CC} = 3$ V	3.4	ns
		$C_L = 50$ pF; $R_L = 500$ Ω ; $V_{CC} = 5$ V	2.5	ns
C_I	input capacitance		2	pF
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f_i = 10$ MHz; $V_{CC} = 3.3$ V; notes 1 and 2	12.0	pF
C_S	switch capacitance	OFF-state	6.5	pF
		ON-state	11	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

C_S = switch capacitance in pF;

V_{CC} = supply voltage in Volts;

2. The condition is $V_i = \text{GND}$ to V_{CC} .

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FUNCTION TABLE

See note 1.

INPUT E	SWITCH
L	OFF
H	ON

Note

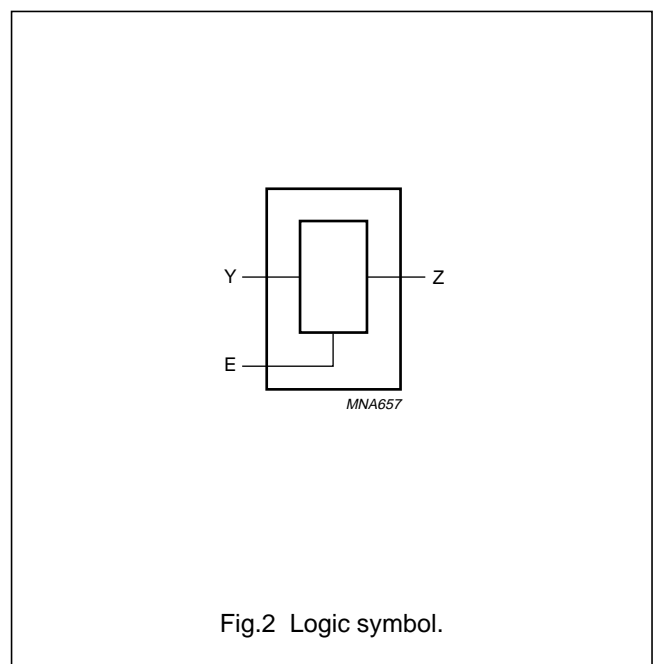
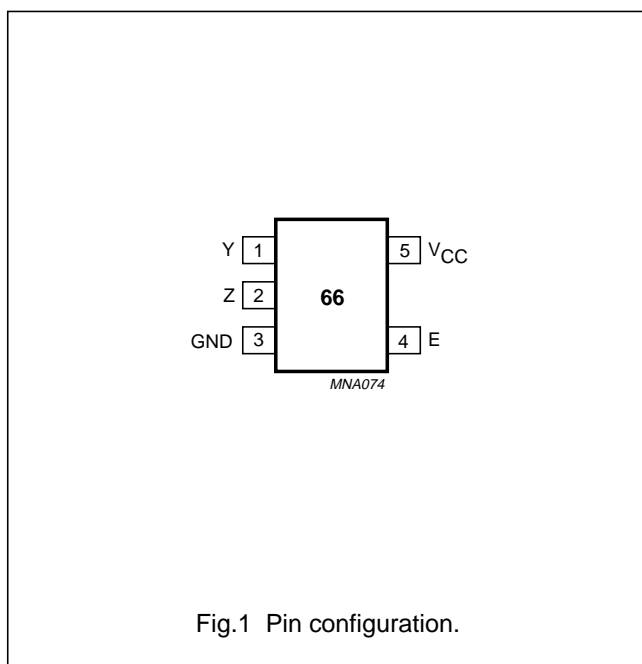
- 1. H = HIGH voltage level;
L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G66GW	-40 to +125 °C	5	SC-88A	plastic	SOT353	VL
74LVC1G66GV	-40 to +125 °C	5	SC-74A	plastic	SOT753	V66

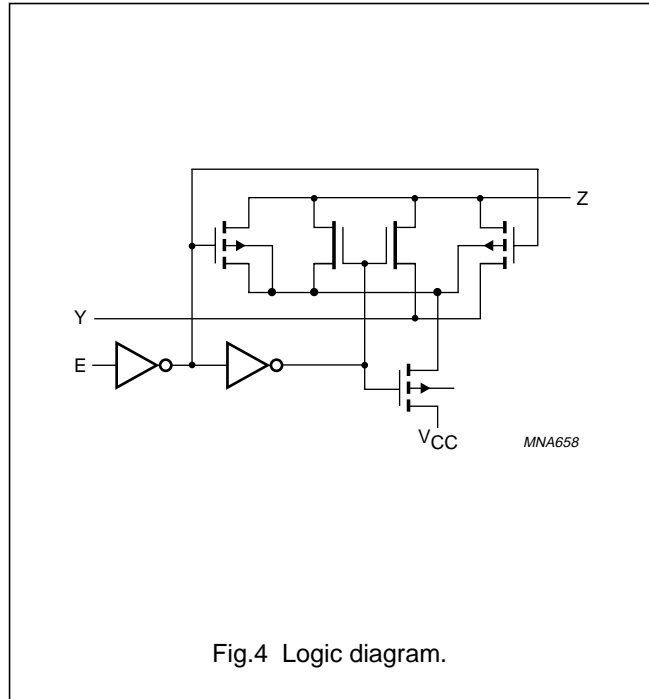
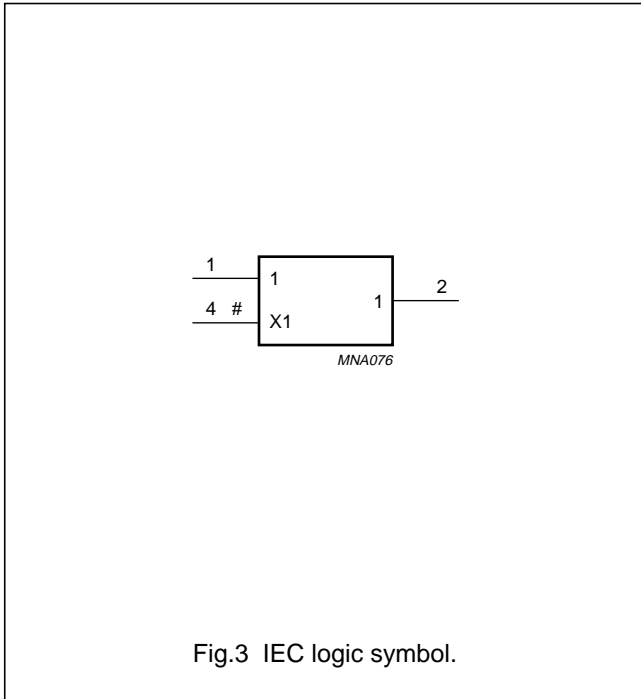
PINNING

PIN	SYMBOL	DESCRIPTION
1	Y	independent input/output
2	Z	independent output/input
3	GND	ground (0 V)
4	E	enable input (active HIGH)
5	V _{CC}	supply voltage



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V
T_{amb}	operating ambient temperature		-40	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.65$ to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ to 5.5 V	0	10	ns/V

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
V_O	output voltage	active mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
I_{OS}	maximum switch current	$V_O = 0$ to V_{CC}	-	± 50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	± 100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	-	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
$T_{amb} = -40$ to $+85$ °C; note 1							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	-	-	V
			2.3 to 2.7	1.7	-	-	V
			2.7 to 3.6	2.0	-	-	V
			4.5 to 5.5	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	-	-	$0.35 \times V_{CC}$	V
			2.3 to 2.7	-	-	0.7	V
			2.7 to 3.6	-	-	0.8	V
			4.5 to 5.5	-	-	$0.3 \times V_{CC}$	V
I_{LI}	input leakage current (control pin)	$V_I = 5.5$ V or GND	5.5	-	± 0.1	± 5	μ A
I_S	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL} ; $ V_S = V_{CC} - GND$; see Fig.5	5.5	-	± 0.1	± 5	μ A
	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL} ; $ V_S = V_{CC} - GND$; see Fig.6	5.5	-	± 0.1	± 5	μ A
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $V_S = GND$ or V_{CC} ; $I_O = 0$	5.5	-	0.1	10	μ A

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC} - 0.6\text{ V}$; $V_S = \text{GND or } V_{CC}$; $I_O = 0$	5.5	–	5	500	μA
$R_{ON(\text{peak})}$	ON-resistance (peak)	$V_S = \text{GND to } V_{CC}$; $V_I = V_{IH}$; see Fig.7 $I_S = 4\text{ mA}$ $I_S = 8\text{ mA}$ $I_S = 12\text{ mA}$ $I_S = 24\text{ mA}$ $I_S = 32\text{ mA}$	1.65 to 1.95 2.3 to 2.7 2.7 3.0 to 3.6 4.5 to 5.5	– – – – –	35 14 11.5 8.5 6.5	100 30 25 20 15	Ω Ω Ω Ω Ω
$R_{ON(\text{rail})}$	ON-resistance (rail)	$V_S = \text{GND}$; $V_I = V_{IH}$; see Fig.7 $I_S = 4\text{ mA}$ $I_S = 8\text{ mA}$ $I_S = 12\text{ mA}$ $I_S = 24\text{ mA}$ $I_S = 32\text{ mA}$	1.65 to 1.95 2.3 to 2.7 2.7 3.0 to 3.6 4.5 to 5.5	– – – – –	10 8.5 7.5 6.5 6	30 20 18 15 10	Ω Ω Ω Ω Ω
		$V_S = V_{CC}$; $V_I = V_{IH}$; see Fig.7 $I_S = 4\text{ mA}$ $I_S = 8\text{ mA}$ $I_S = 12\text{ mA}$ $I_S = 24\text{ mA}$ $I_S = 32\text{ mA}$	1.65 to 1.95 2.3 to 2.7 2.7 3.0 to 3.6 4.5 to 5.5	– – – – –	12 8.5 7.5 6.5 6	30 20 18 15 10	Ω Ω Ω Ω Ω
$R_{ON(\text{flatness})}$	ON-resistance (flatness)	$V_S = \text{GND to } V_{CC}$; $V_I = V_{IH}$; see Figs 9 to 13 $I_S = 4\text{ mA}$ $I_S = 8\text{ mA}$ $I_S = 12\text{ mA}$ $I_S = 24\text{ mA}$ $I_S = 32\text{ mA}$	1.65 to 1.95 2.3 to 2.7 2.7 3.0 to 3.6 4.5 to 5.5	– – – – –	100 ⁽²⁾ 17 ⁽²⁾ 10 ⁽²⁾ 5 ⁽²⁾ 3 ⁽²⁾	– – – – –	Ω Ω Ω Ω Ω

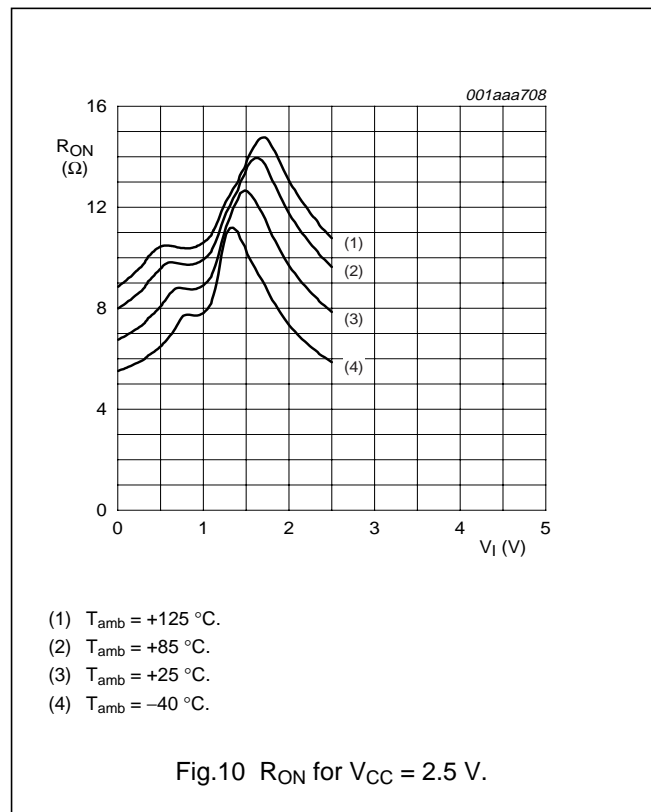
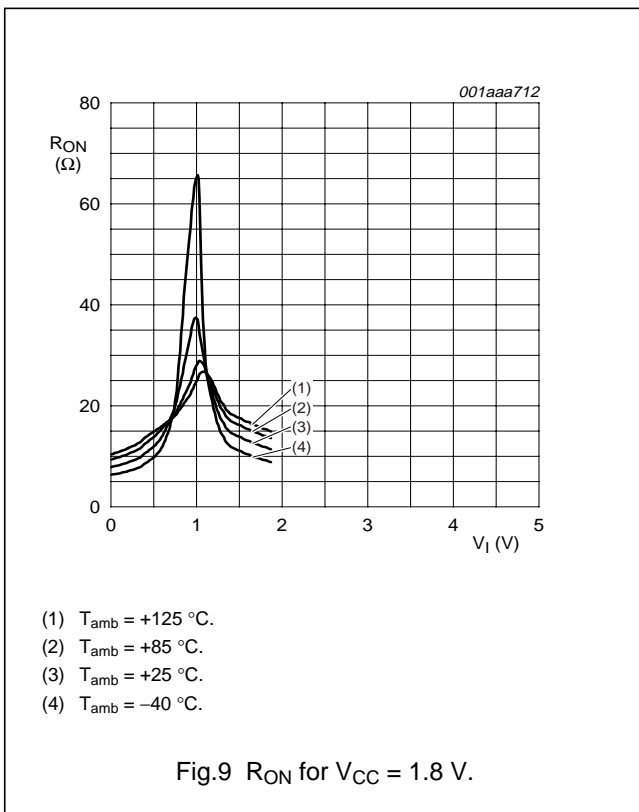
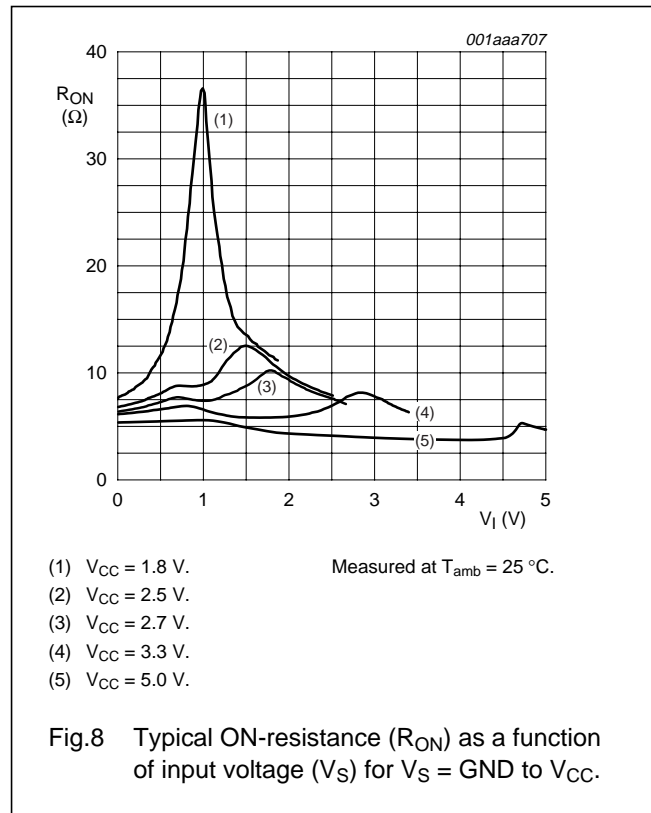
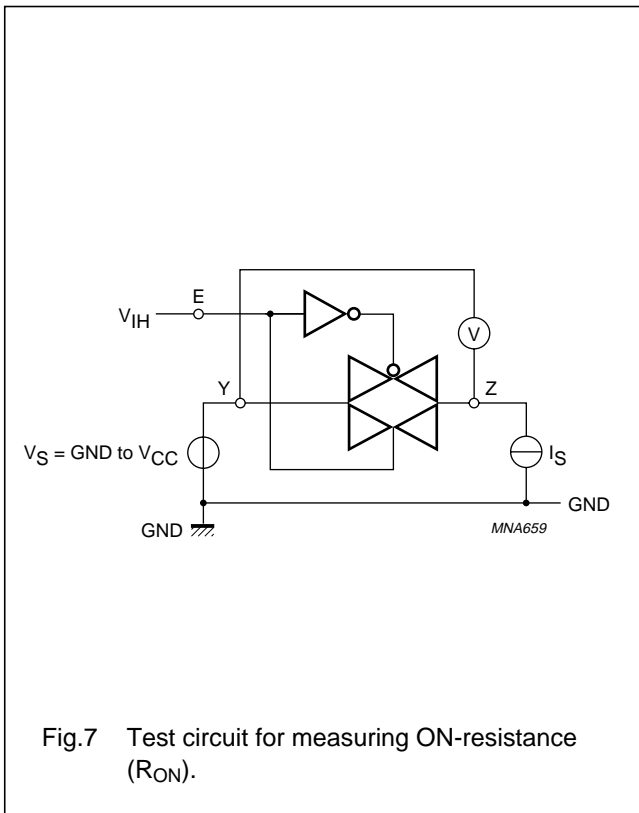
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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.65 to 1.95	0.65 × V _{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V _{CC}	–	–	V
V _{IL}	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V _{CC}	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V _{CC}	V
I _{LI}	input leakage current (control pin)	V _I = 5.5 V or GND	5.5	–	–	100	μA
I _S	analog switch OFF-state current	V _I = V _{IH} or V _{IL} ; V _S = V _{CC} – GND; see Fig.5	5.5	–	–	200	μA
	analog switch ON-state current	V _I = V _{IH} or V _{IL} ; V _S = V _{CC} – GND; see Fig.6	5.5	–	–	200	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; V _S = GND or V _{CC} ; I _O = 0	5.5	–	–	200	μA
ΔI _{CC}	additional quiescent supply current per control pin	V _I = V _{CC} – 0.6 V; V _S = GND or V _{CC} ; I _O = 0	5.5	–	–	5000	μA
R _{ON(peak)}	ON-resistance (peak)	V _S = GND to V _{CC} ; V _I = V _{IH} ; see Fig.7					
		I _S = 4 mA	1.65 to 1.95	–	–	150	Ω
		I _S = 8 mA	2.3 to 2.7	–	–	45	Ω
		I _S = 12 mA	2.7	–	–	38	Ω
		I _S = 24 mA	3.0 to 3.6	–	–	30	Ω
		I _S = 32 mA	4.5 to 5.5	–	–	23	Ω

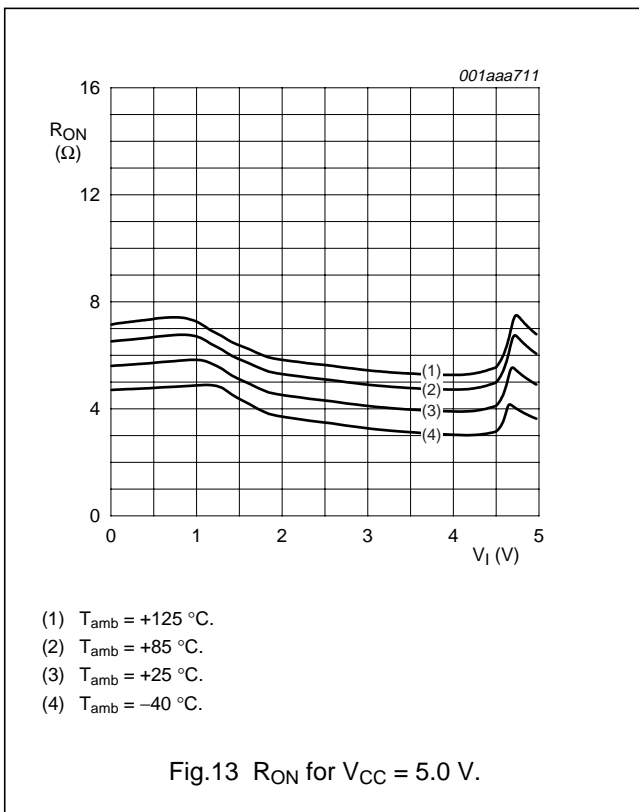
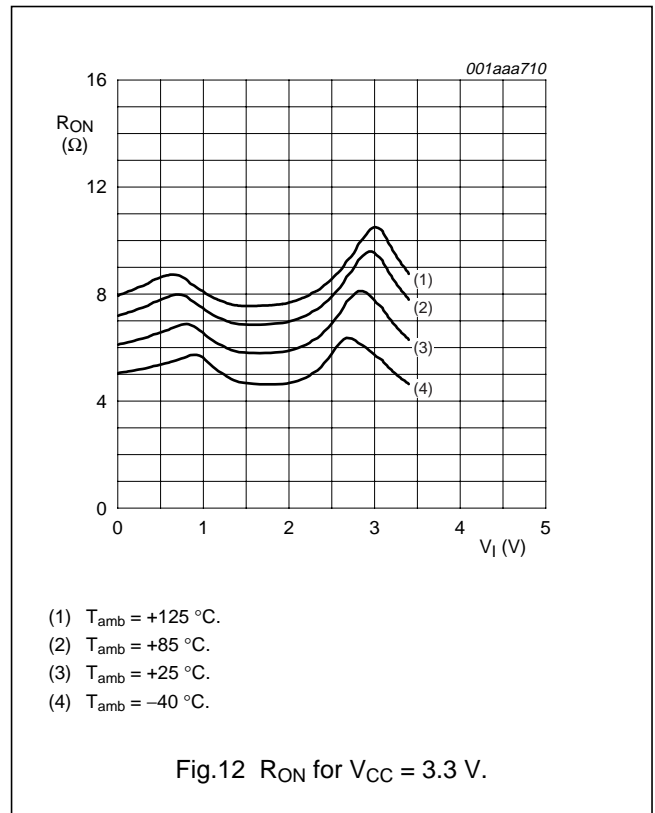
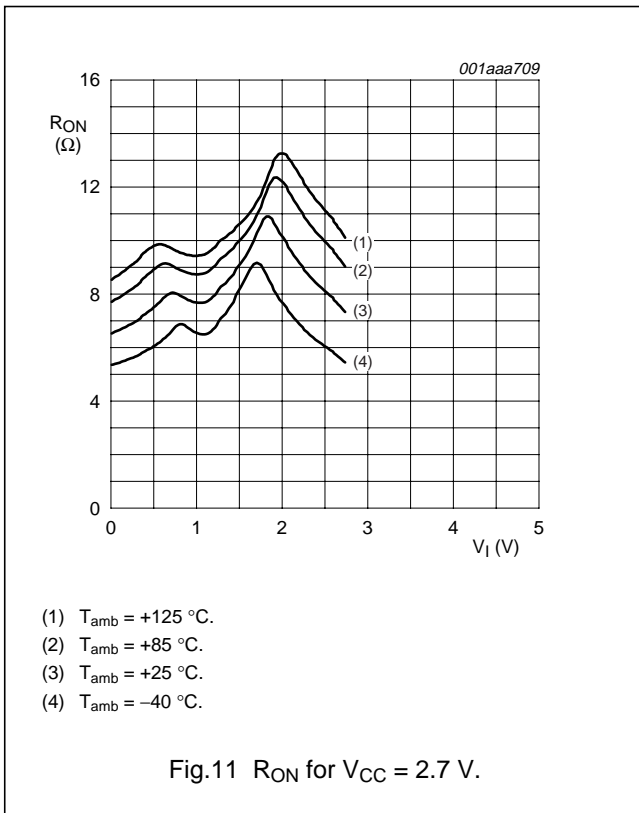
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AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay Y to Z or Z to Y	see Figs 14 and 16	1.65 to 1.95	–	0.8	2	ns
			2.3 to 2.7	–	0.4	1.2	ns
			2.7	–	0.4	1	ns
			3.0 to 3.6	–	0.3	0.8	ns
			4.5 to 5.5	–	0.2	0.6	ns
t _{PZH} /t _{PZL}	turn-ON time E to V _{OS}	see Figs 15 and 16	1.65 to 1.95	1	5.3	12	ns
			2.3 to 2.7	1	3.0	6.5	ns
			2.7	1	2.6	6	ns
			3.0 to 3.6	1	2.5	5	ns
			4.5 to 5.5	1	1.9	4.2	ns
t _{PHZ} /t _{PLZ}	turn-OFF time E to V _{OS}	see Figs 15 and 16	1.65 to 1.95	1	4.2	10	ns
			2.3 to 2.7	1	2.4	6.9	ns
			2.7	1	3.6	7.5	ns
			3.0 to 3.6	1	3.4	6.5	ns
			4.5 to 5.5	1	2.5	5	ns
T_{amb} = -40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay Y to Z or Z to Y	see Figs 14 and 16	1.65 to 1.95	–	–	3	ns
			2.3 to 2.7	–	–	2	ns
			2.7	–	–	1.5	ns
			3.0 to 3.6	–	–	1.5	ns
			4.5 to 5.5	–	–	1	ns
t _{PZH} /t _{PZL}	turn-ON time E to V _{OS}	see Figs 15 and 16	1.65 to 1.95	1	–	15.5	ns
			2.3 to 2.7	1	–	8.5	ns
			2.7	1	–	8	ns
			3.0 to 3.6	1	–	6.5	ns
			4.5 to 5.5	1	–	5.5	ns
t _{PHZ} /t _{PLZ}	turn-OFF time E to V _{OS}	see Figs 15 and 16	1.65 to 1.95	1	–	13	ns
			2.3 to 2.7	1	–	9	ns
			2.7	1	–	9.5	ns
			3.0 to 3.6	1	–	8.5	ns
			4.5 to 5.5	1	–	6.5	ns

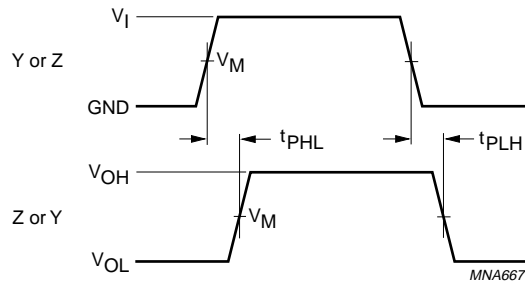
Note

1. All typical values are measured at T_{amb} = 25 °C.

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AC WAVEFORMS



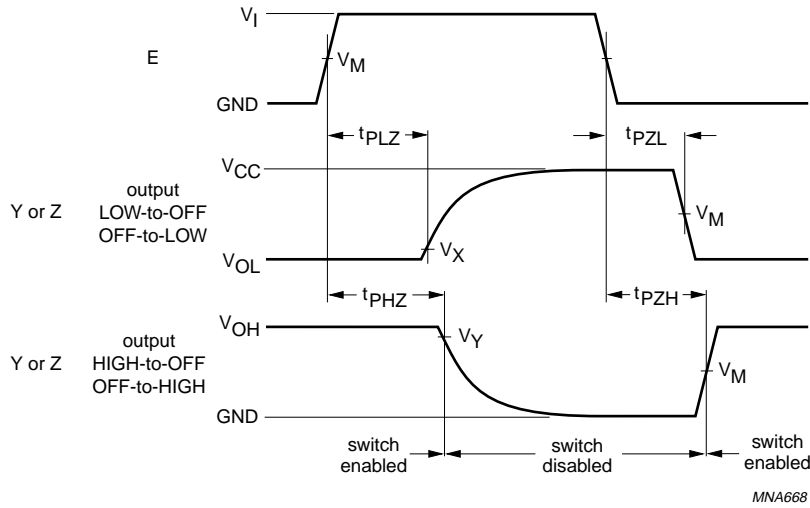
V_{CC}	V_M	V_I	INPUT $t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.14 The input (V_S) to output (V_O) propagation delays.

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V_{CC}	V_M	V_I	INPUT $t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

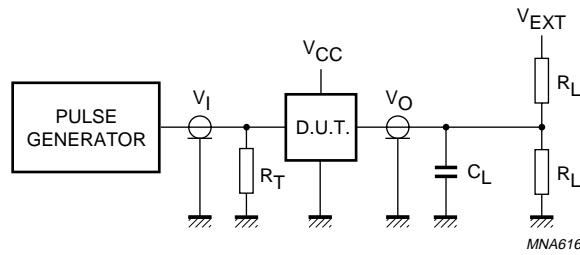
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
 $V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V;
 $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
 $V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.15 The turn-on and turn-off times.

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V _{CC}	V _I	C _L	R _L	V _{EXT}		
				t _{PLH} /t _{PHL}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.65 to 1.95 V	V _{CC}	30 pF	1 kΩ	open	GND	2 × V _{CC}
2.3 to 2.7 V	V _{CC}	30 pF	500 Ω	open	GND	2 × V _{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V _{CC}	50 pF	500 Ω	open	GND	2 × V _{CC}

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.16 Load circuitry for switching times.

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ADDITIONAL AC CHARACTERISTICSAt recommended conditions and all typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	TYP.	UNIT
d _{sin}	sine-wave distortion	R _L = 10 kΩ; C _L = 50 pF; f _i = 1 kHz; see Fig.18	1.65	0.032	%
			2.3	0.008	%
			3	0.006	%
			4.5	0.001	%
		R _L = 10 kΩ; C _L = 50 pF; f _i = 10 kHz; see Fig.18	1.65	0.068	%
			2.3	0.009	%
			3	0.008	%
			4.5	0.006	%
f _{ON(res)}	switch ON signal frequency response	R _L = 600 Ω; C _L = 50 pF; f _i = 1 MHz; see Fig.17; note 1	1.65	135	MHz
			2.3	145	MHz
			3	150	MHz
			4.5	155	MHz
		R _L = 50 Ω; C _L = 5 pF; f _i = 1 MHz; see Fig.17; note 1	1.65	>500	MHz
			2.3	>500	MHz
			3	>500	MHz
			4.5	>500	MHz
α _{OFF(ft)}	switch OFF signal feed-through attenuation	R _L = 600 Ω; C _L = 50 pF; f _i = 1 MHz; see Fig.19; note 2	1.65	-46	dB
			2.3	-46	dB
			3	-46	dB
			4.5	-46	dB
		R _L = 0 Ω; C _L = 50 pF; f _i = 1 MHz; see Fig.19; note 2	1.65	-37	dB
			2.3	-37	dB
			3	-37	dB
			4.5	-37	dB
V _{ct}	crosstalk (control input to signal output)	R _L = 600 Ω; C _L = 50 pF; f _i = 1 MHz; t _r = t _f = 2 ns; see Fig.20	1.65	69	mV
			2.3	87	mV
			3	156	mV
			4.5	302	mV
f _{max}	frequency response (-3 dB)	R _L = 50 Ω; C _L = 10 pF; see Fig.17; note 1	1.65	200	MHz
			2.3	350	MHz
			3	410	MHz
			4.5	440	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 10 MHz	2.5	9.8	pF
			3.3	12.0	pF
			5.0	17.3	pF
Q	charge injection	C _L = 0.1 nF; V _{gen} = 0 V; R _{gen} = 0 Ω; f _i = 1 MHz; R _L = 1 MΩ; see Fig.21; note 3	1.65 to 5.5	0.05	pC

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Notes

1. Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.
2. Adjust f_i voltage to obtain 0 dBm level at input.
3. Guaranteed by design.

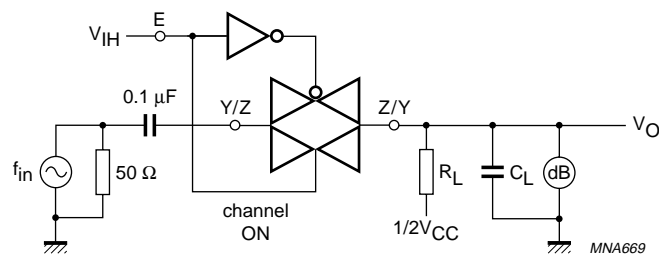
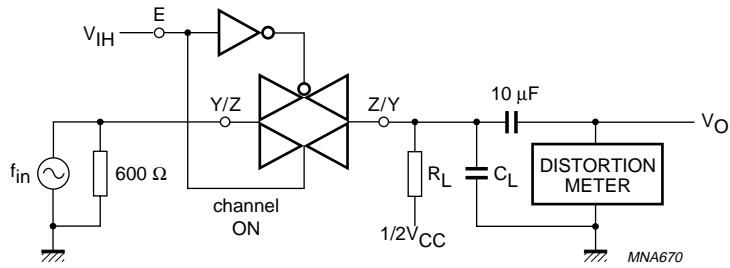


Fig.17 Test circuit for measuring the frequency response when switch is ON.

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V _{CC}	V _I
1.65 V	1.4 V (p-p)
2.3 V	2 V (p-p)
3 V	2.5 V (p-p)
4 V	4 V (p-p)

Fig.18 Test circuit for measuring sine-wave distortion.

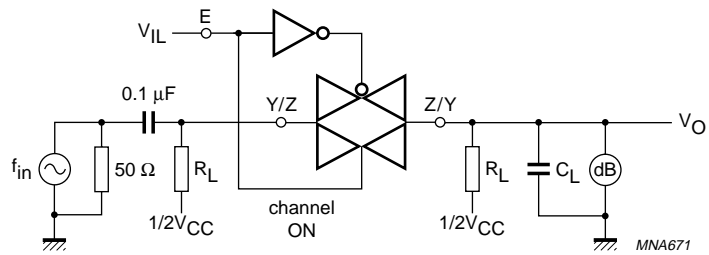


Fig.19 Test circuit for measuring feed-through when switch is OFF.

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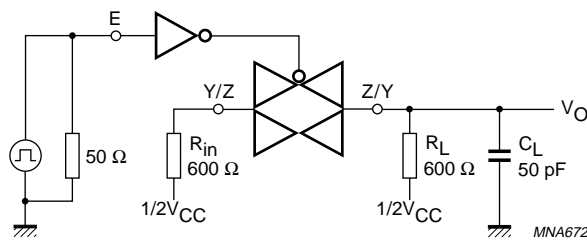
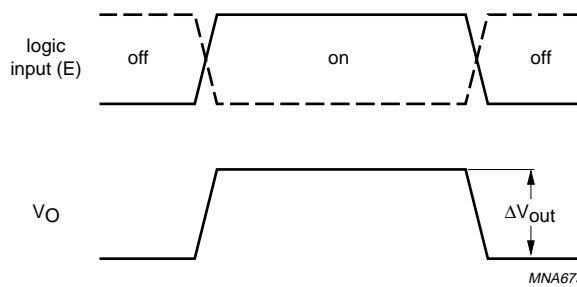
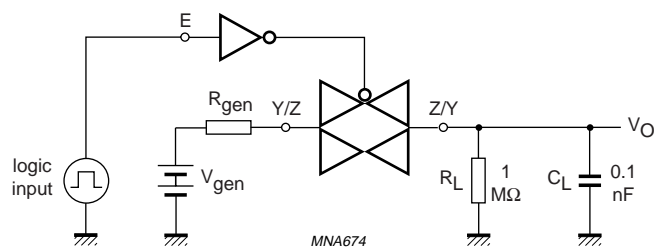


Fig.20 Crosstalk.



$$Q = (\Delta V_{out}) \times (C_L)$$

Fig.21 Charge injection test.

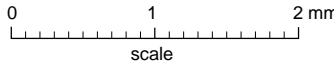
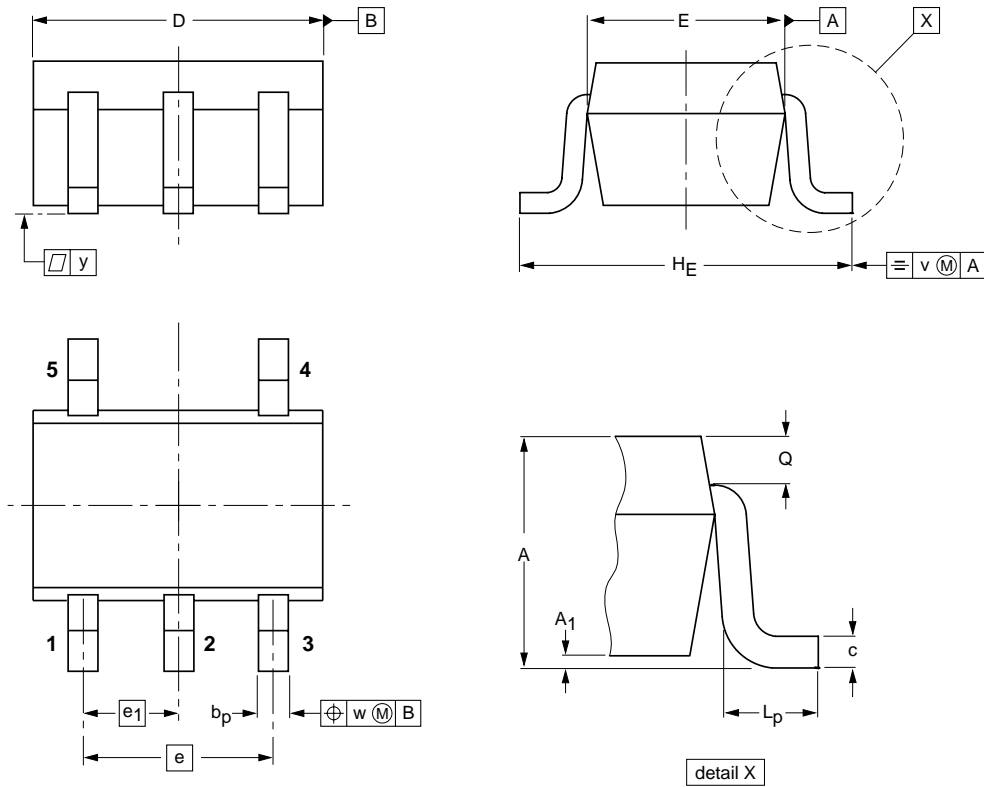
Bilateral switch

74LVC1G66

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E ⁽²⁾	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

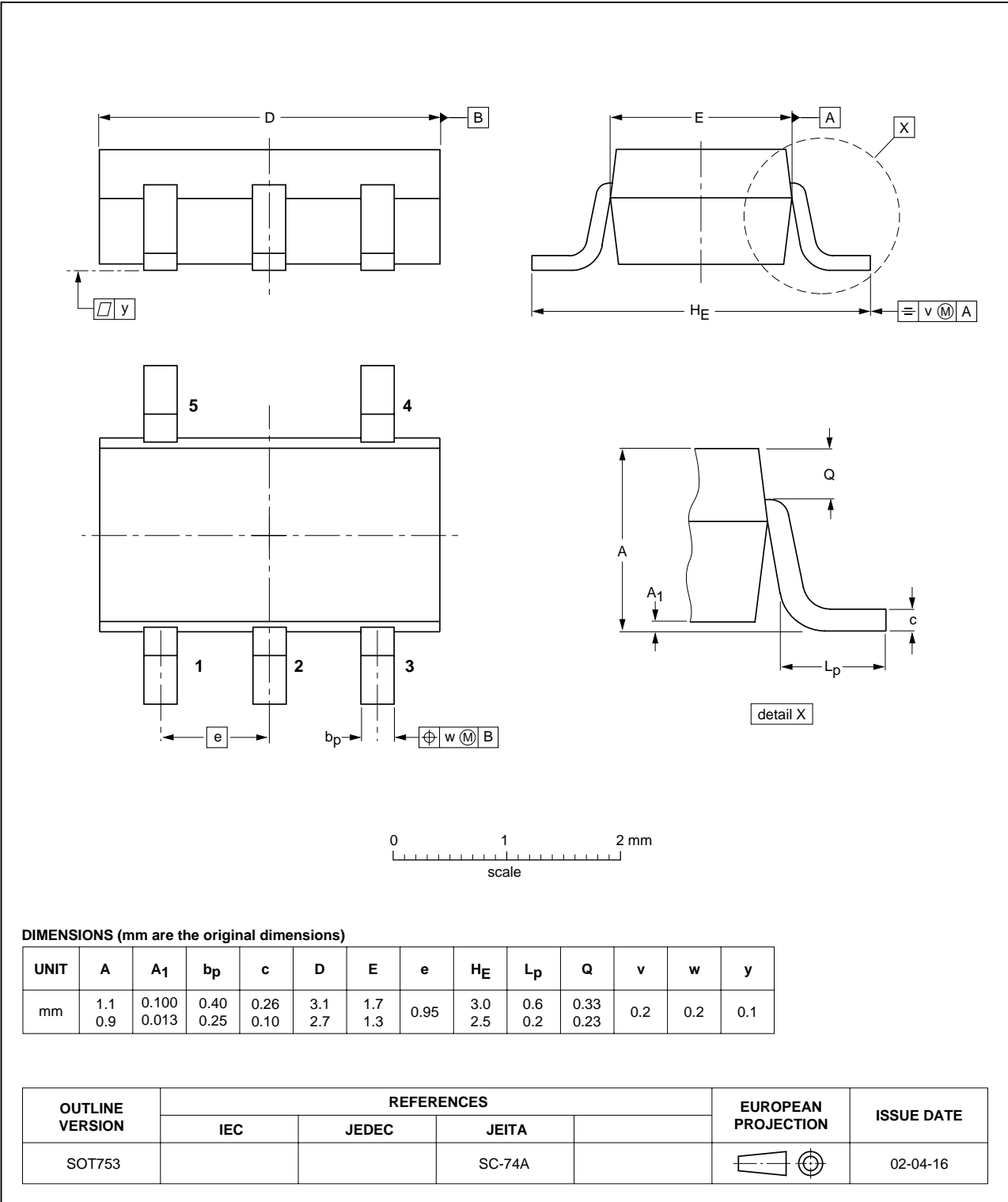
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Bilateral switch

74LVC1G66

Plastic surface mounted package; 5 leads

SOT753



Bilateral switch

74LVC1G66

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
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