

# 22-BIT PROGRAMMABLE PULSE GENERATOR (SERIES 3D3622 – SERIAL INTERFACE)



## FEATURES

- All-silicon, low-power CMOS technology
- 3.3V operation
- Vapor phase, IR and wave solderable
- Programmable via serial interface
- **Increment range:** 0.25ns through 50.0ns
- **Pulse width tolerance:** 1% (See Table 1)
- **Supply current:** 8mA typical
- **Temperature stability:** ±1.5% max (-40C to 85C)
- **Vdd stability:** ±1.0% max (3.0V to 3.6V)



## PACKAGE / PINOUT

TRIG	1	14	VDD
RES	2	13	OUT
GND	3	12	OUTB
NC	4	11	SI
NC	5	10	SC
SO	6	9	NC
GND	7	8	AE

3D3622D-xx SOIC

For mechanical dimensions, click [here](#).  
For package marking details, click [here](#).

## FUNCTIONAL DESCRIPTION

The 3D3622 device is a versatile 22-bit programmable monolithic pulse generator. A rising-edge on the trigger input (TRIG) initiates the pulse, which is presented on the output pins (OUT,OUTB). The pulse width, programmed via the serial interface, can be varied over 4,194,303 equal steps according to the formula:

$$t_{PW} = t_{inh} + addr * t_{inc}$$

where addr is the programmed address,  $t_{inc}$  is the pulse width increment (equal to the device dash number), and  $t_{inh}$  is the inherent (address zero) pulse width. The device also offers a reset input (RES), which can be used to terminate the pulse before the programmed time has expired.

The all-CMOS 3D3622 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL pulse generators. It is offered in a standard 14-pin SOIC.

## PIN DESCRIPTIONS

TRIG	Trigger Input
RES	Reset Input
OUT	Pulse Output
OUTB	Complementary Pulse Output
AE	Address Enable Input
SC	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
VDD	+3.3 Volts
GND	Ground
NC	No Internal Connection

### TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	Pulse Width Step (ns)	Minimum P.W. (ns)	Maximum Pulse Width
3D3622D-0.25	0.25 ± 0.12	10.0 ± 2.0	1.05 ms ± 10 us
3D3622D-0.4	0.40 ± 0.20	10.0 ± 2.0	1.68 ms ± 17 us
3D3622D-0.5	0.50 ± 0.25	10.0 ± 2.0	2.10 ms ± 21 us
3D3622D-1	1.00 ± 0.50	10.0 ± 2.0	4.19 ms ± 42 us
3D3622D-2	2.00 ± 1.00	10.0 ± 2.0	8.39 ms ± 84 us
3D7622D-2.5	2.50 ± 1.25	10.0 ± 2.0	10.5 ms ± 105 us
3D3622D-4	4.00 ± 2.00	10.0 ± 2.0	16.8 ms ± 170 us
3D3622D-5	5.00 ± 2.50	15.0 ± 5.0	21.0 ms ± 210 us
3D3622D-10	10.0 ± 5.00	24.0 ± 6.0	41.9 ms ± 420 us
3D3622D-20 *	20.0 ± 10.0	42.0 ± 8.0	83.9 ms ± 840 us
3D7622D-25 *	20.0 ± 10.0	15.0 ± 5.0	105 ms ± 1.0 ms
3D3622D-40 *	40.0 ± 20.0	15.0 ± 5.0	168 ms ± 1.7 ms
3D3622D-50 *	50.0 ± 25.0	15.0 ± 5.0	210 ms ± 2.1 ms

NOTES: Any increment between 0.25 and 50 ns not shown is also available as a standard device.

\* Some restrictions apply to dash numbers greater than 15. See application notes for more details.

## APPLICATION NOTES

### GENERAL INFORMATION

Figure 1 illustrates the main functional blocks of the 3D3622. Since the 3D3622 is a CMOS design, all unused input pins must be returned to well-defined logic levels, VDD or Ground.

The pulse generator architecture is comprised of a number of delay cells, which are controlled by the 6 LSB bits of the address, and an oscillator & counter, which are controlled by the 16 MSB bits of the address. Each device is individually trimmed for maximum accuracy and linearity throughout the address range. The change in pulse width from one address setting to the next is called the *increment*, or LSB. It is nominally equal to the device dash number. The minimum pulse width, achieved by setting the address to zero, is called the *inherent pulse width*.

For dash numbers larger than 15, the 6 LSB bits are invalid, and the address loaded must therefore be a multiple of 64 (ie, 0, 64, 128, 192, etc). When used in this manner, the device is essentially a 16-bit generator, with an effective increment equal to 64 times the dash number.

For best performance, it is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred. Also, signal traces should be kept as short as possible.

### PULSE WIDTH ACCURACY

There are a number of ways of characterizing the pulse width accuracy of a programmable pulse generator. The first is the *differential nonlinearity* (DNL), also referred to as the increment error. It is defined as the deviation of the increment at a given address from its nominal value. For most dash numbers, the DNL is within 0.5 LSB at every address (see Table 1: Pulse Width Step).

The *integrated nonlinearity* (INL) is determined by first constructing the least-squares best fit straight line through the pulse-width-versus-address data. The INL is then the deviation of a given width from this line. For all dash numbers, the INL is within 1.0 LSB at every address.

The *relative error* is defined as follows:

$$e_{rel} = (t_{PW} - t_{inh}) - addr * t_{inc}$$

where *addr* is the address,  $t_{PW}$  is the measured width at this address,  $t_{inh}$  is the measured

inherent width, and  $t_{inc}$  is the nominal increment. It is very similar to the INL, but simpler to calculate. For most dash numbers, the relative error is less than 1.0 LSB at every address (see Table 1).

The *absolute error* is defined as follows:

$$e_{abs} = t_{PW} - (t_{inh} + addr * t_{inc})$$

where  $t_{inh}$  is the nominal inherent delay. The absolute error is limited to 1.5 LSB or 3.0 ns, whichever is greater, at every address.

The *inherent pulse width error* is the deviation of the inherent width from its nominal value. It is limited to 1.0 LSB or 2.0 ns, whichever is greater.

### PULSE WIDTH STABILITY

The characteristics of CMOS integrated circuits are strongly dependent on power supply and temperature. The 3D3622 utilizes novel compensation circuitry to minimize the performance variations induced by fluctuations in power supply and/or temperature.

With regard to stability, the output pulse width of the 3D3622 at a given address, *addr*, can be split into two components: the *inherent pulse width* ( $t_{inh}$ ) and the *relative pulse width* ( $t_{PW} - t_{inh}$ ). These components exhibit very different stability coefficients, both of which must be considered in very critical applications.

The thermal coefficient of the relative pulse width is limited to  $\pm 250$  PPM/C (except for the -0.25), which is equivalent to a variation, over the -40C to 85C operating range, of  $\pm 1.5\%$  ( $\pm 9\%$  for the dash 0.25) from the room-temperature pulse width. This holds for all dash numbers. The thermal coefficient of the inherent pulse width is nominally +20ps/C for dash numbers less than 5, and +30ps/C for all other dash numbers.

The power supply sensitivity of the relative pulse width is  $\pm 1.0\%$  ( $\pm 3.0\%$  for the dash 0.25) over the 3.0V to 3.6V operating range, with respect to the pulse width at the nominal 3.3V power supply. This holds for all dash numbers. The sensitivity of the inherent pulse width is nominally -5ps/mV for all dash numbers.

It should also be noted that the DNL is also adversely affected by thermal and supply variations, particularly at the MSL/LSB crossovers (ie, 63 to 64, 127 to 128, etc).

## APPLICATION NOTES (CONT'D)

### TRIGGER & RESET TIMING

Figure 2 shows the timing diagram of the device when the reset input (RES) is not used. In this case, the pulse is triggered by the rising edge of the TRIG signal and ends at a time determined by the address loaded into the device. While the pulse is active, any additional triggers occurring are ignored. Once the pulse has ended, and after a short recovery time, the next trigger is recognized. Figure 3 shows the timing for the case where a reset is issued before the pulse has ended. Again, there is a short recovery time required before the next trigger can occur.

### ADDRESS UPDATE

While observing data setup ( $t_{DS}$ ) and data hold ( $t_{DH}$ ) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the clock (SC) while the enable (AE) is high, as shown in Figure 4. The falling edge of the AE activates the new pulse width value, which is reflected at the output upon the next trigger.

As shown in the figure, most of the address information for the next pulse can be loaded while the current pulse is active. It is only on the falling-edge of AE that the device adjusts to the new pulse width setting. In other words, the device controller does not need to wait for the current pulse to end before beginning an address update sequence. This can save a considerable amount of time in certain applications.

As data is shifted into the serial data input (SI), the previous contents of the 22-bit input register are shifted out of the serial output pin (SO) in MSB-to-LSB order. This allows cascading of multiple devices by connecting SO of the preceding device to SI of the succeeding device, as illustrated in Figure 5. The total number of serial data bits in a cascade configuration must be 22 times the number of units, and each group of 22 bits must be transmitted in MSB-to-LSB order.

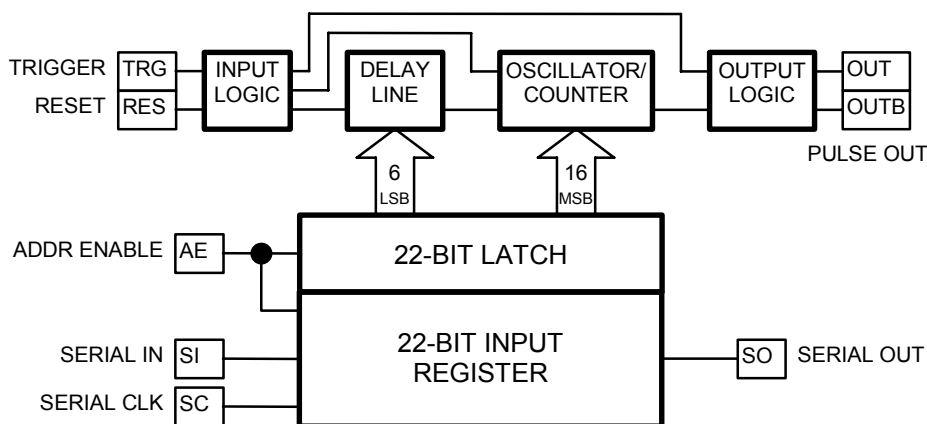


Figure 1: Functional block diagram

APPLICATION NOTES (CONT'D)

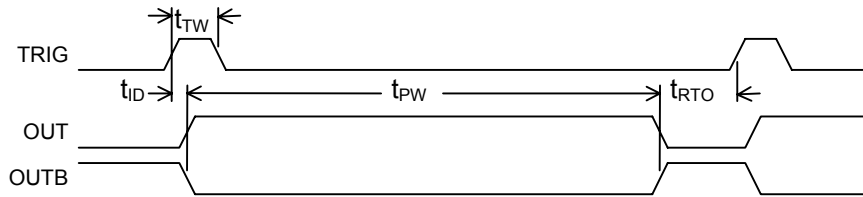


Figure 2: Timing Diagram (RES=0)

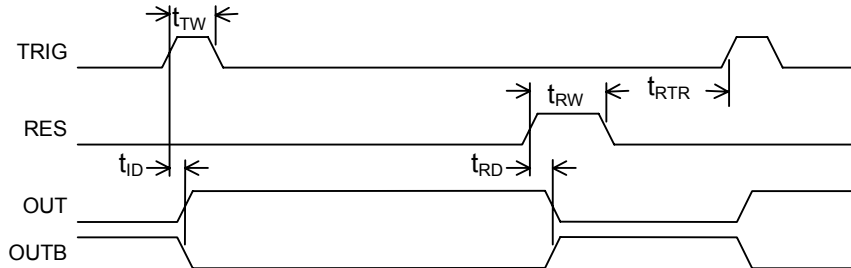


Figure 3: Timing Diagram (with reset)

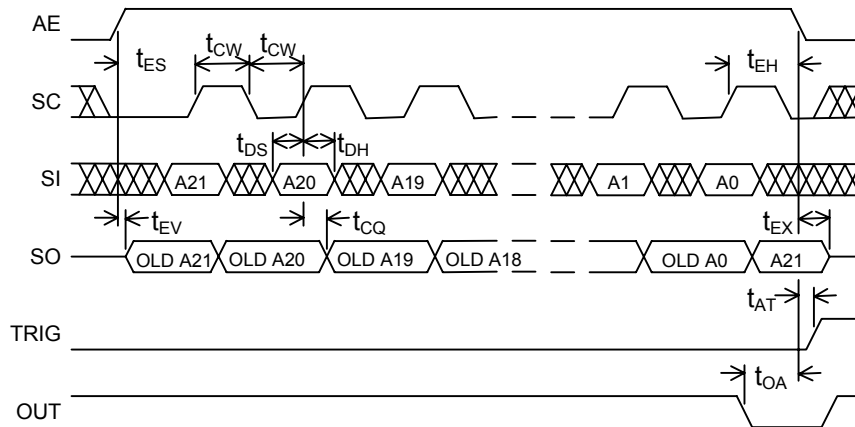


Figure 4: Address Update

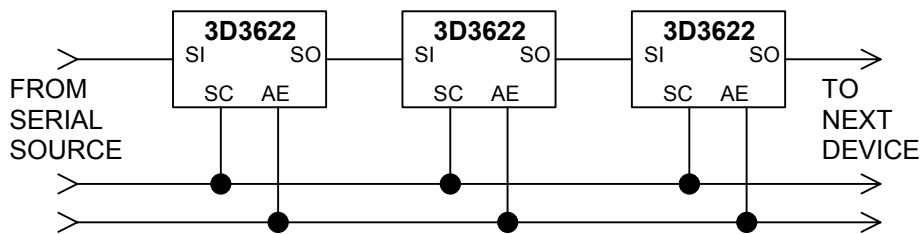


Figure 5: Cascading Multiple Devices

## DEVICE SPECIFICATIONS

### TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V <sub>DD</sub>	-0.3	7.0	V	
Input Pin Voltage	V <sub>IN</sub>	-0.3	V <sub>DD</sub> +0.3	V	
Input Pin Current	I <sub>IN</sub>	-10	10	mA	25C
Storage Temperature	T <sub>STRG</sub>	-55	150	C	
Lead Temperature	T <sub>LEAD</sub>		300	C	10 sec

### TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I <sub>DD</sub>		8.0	12.0	mA	
High Level Input Voltage	V <sub>IH</sub>	2.0			V	
Low Level Input Voltage	V <sub>IL</sub>			0.8	V	
High Level Input Current	I <sub>IH</sub>			1.0	μA	V <sub>IH</sub> = V <sub>DD</sub>
Low Level Input Current	I <sub>IL</sub>			1.0	μA	V <sub>IL</sub> = 0V
High Level Output Current	I <sub>OH</sub>		-35.0	-4.0	mA	V <sub>DD</sub> = 3.0V V <sub>OH</sub> = 2.4V
Low Level Output Current	I <sub>OL</sub>	4.0	15.0		mA	V <sub>DD</sub> = 3.0V V <sub>OL</sub> = 0.4V
Output Rise & Fall Time	T <sub>R</sub> & T <sub>F</sub>		2.0	2.5	ns	C <sub>LD</sub> = 5 pf

$$*I_{DD}(\text{Dynamic}) = 2 * C_{LD} * V_{DD} * F$$

where: C<sub>LD</sub> = Average capacitance load/output (pf)  
F = Trigger frequency (GHz)

Input Capacitance = 5 pf typical  
Output Load Capacitance (C<sub>LD</sub>) = 25 pf max

### TABLE 4: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	REFER TO
Trigger Width	t <sub>TW</sub>	5			ns	Figure 2 & 3
Trigger Inherent Delay	t <sub>ID</sub>			5	ns	Figure 2 & 3
Output Pulse Width	t <sub>PW</sub>				ns	Figure 2
Re-trigger Time	t <sub>RTO</sub>	3			ns	Figure 2
Reset Width	t <sub>RW</sub>	TBD			ns	Figure 3
Reset to Output Low	t <sub>RD</sub>			5	ns	Figure 3
End of Reset to Next Trigger	t <sub>RTR</sub>	3			ns	Figure 3
AE High to First Clock Edge	t <sub>ES</sub>	10			ns	Figure 4
AE High to Serial Output Valid	t <sub>EV</sub>			20	ns	Figure 4
Serial Clock Width	t <sub>CW</sub>	8			ns	Figure 4
Data Setup to Clock	t <sub>DS</sub>	10			ns	Figure 4
Data Hold from Clock	t <sub>DH</sub>	3			ns	Figure 4
Clock to Serial Output	t <sub>CQ</sub>			8	ns	Figure 4
Last Clock Edge to AE Low	t <sub>EH</sub>	8			ns	Figure 4
Output Low to AE Low	t <sub>OA</sub>	TBD			ns	Figure 4
AE Low to Serial Output High-Z	t <sub>EX</sub>			20	ns	Figure 4
AE Low to Trigger	t <sub>AT</sub>	10			ns	Figure 4

## TYPICAL APPLICATIONS

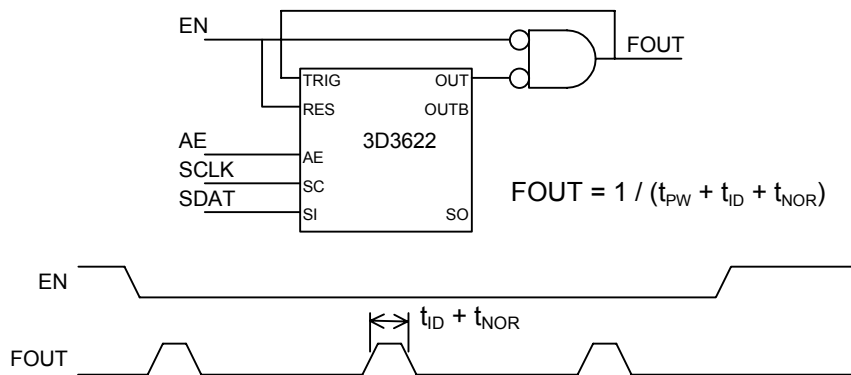


Figure 6: Programmable Oscillator

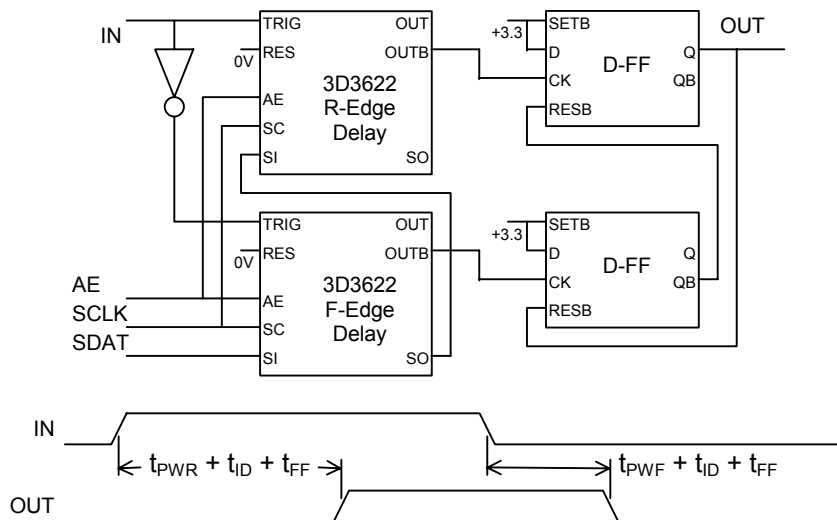


Figure 7: Programmable Delay Line

