KC80 Mode bus timings

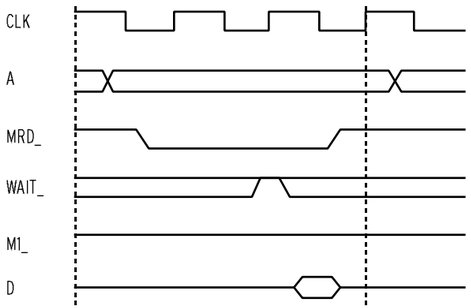


Fig. 11. KC80 Mode Opcode fetch cycle
(0 wait state.)

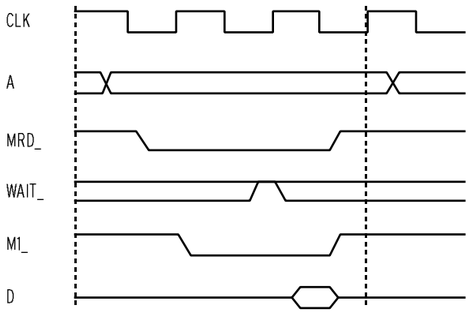


Fig. 12. KC80 Mode Memory read cycle
(0 wait state.)

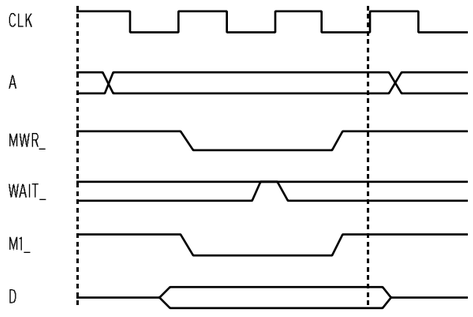


Fig. 13. KC80 Mode Memory write cycle
(0 wait state.)

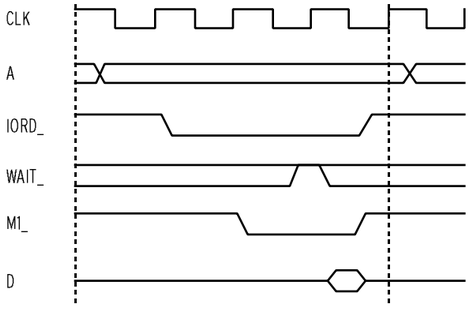


Fig. 14. KC80 Mode I/O read cycle
(0 wait state.)

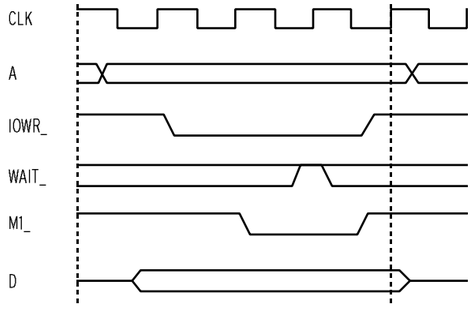


Fig. 15. KC80 Mode I/O write cycle
(0 wait state.)

High Speed 8 bit CPU
KL5C8400

GENERAL DESCRIPTIONS

KL5C8400 is a fast 8 bit CPU, which is compatible with the Z80 microprocessor at binary level. With an internal 16 bit RISC-like architecture, the performance of KL5C8400 is equivalent to the Z80 microprocessor at 44 MHz. With this high performance, the KL5C8400 is faster than typical 16 bit microcontrollers and CPUs. The advanced CMOS technology provides high performance at low power consumption.

KL5C8400 has two operation modes controlled by CNFG input (mode pin). KL5C8400 provides 1.2 times higher performance at the same clock rate in Z80 mode. In KC80 mode, KL5C8400 provides 1.3 times higher performance at the same clock rate. There is also an advantage in memory access time in KC80 mode, because KL5C8400 doesn't have M1 cycle.

In Z80 mode, KL5C8400 operates in Z80 compatible bus cycles. Then, Z80 peripherals can be used with KL5C8400 in mode 2 interrupt.

In KC80 mode, KL5C8400 fetches its opecode using the same busy cycle as memory read. Then, slower memory can be used with KL5C8400 in KC80 mode. There is also a performance advantage because it fetches its opecode in shorter opcode fetch cycle. In KC80 mode, only mode 1 interrupt can be used.

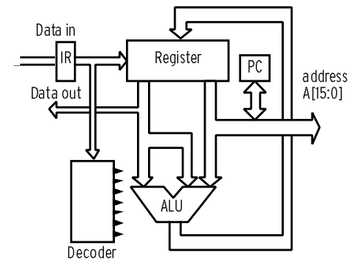
FEATURES

- **Instruction set:** Fully compatible with Z80 MPU at binary level
- **High speed operation:** 33 MHz (equivalent performance of Z80 at 44 MHz)
- **Maximum execution time:** 90 nS (3clock)
- **Low power consumtpion:**
- **Address space:** 64 kbyte
- **Operational clock frequency:** 0~33 MHz
- **Interrupt:** Maskable interrupt 1, Non-maskable 1
- **Package:** 44 pin QFP package
- **Two operation modes:** Z80 mode (CNFG = "H"), KC80 mode (CNFG = "L")

Instruction execution time comparison

Instructions	KL5C8400 (Z80 mode)	KL5C8400 (KC80 mode)	Z80
LD B, C	4 clocks	3 clocks	4 clocks
ADD HL, BC	4 clocks	3 clocks	11 clocks
DEC DE	4 clocks	3 clocks	6 clocks
POP AF	10 clocks	9 clocks	10 clocks
JR Z, +20th	10 clocks	9 clocks	12 clocks

BLOCK DIAGRAM



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KL5C8400

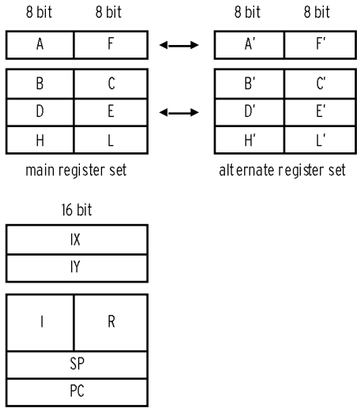

Fig. 2 KL5C8400 CPU registers

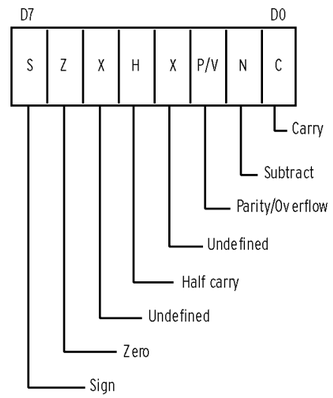

Fig. 3 Flag bit assignment

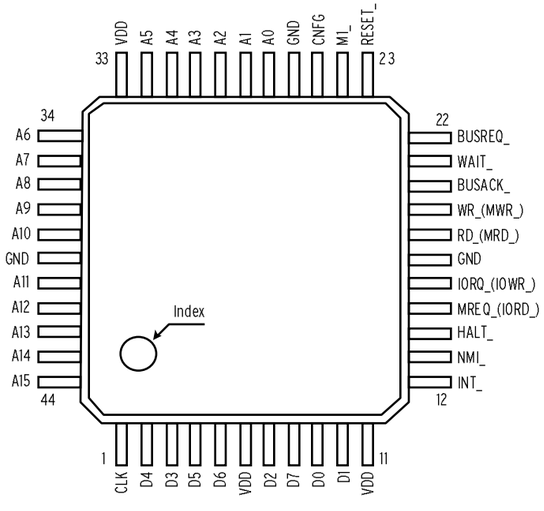

Fig. 4 QFP44 pin assignment

( ) indicates signal names in KC80 Mode.

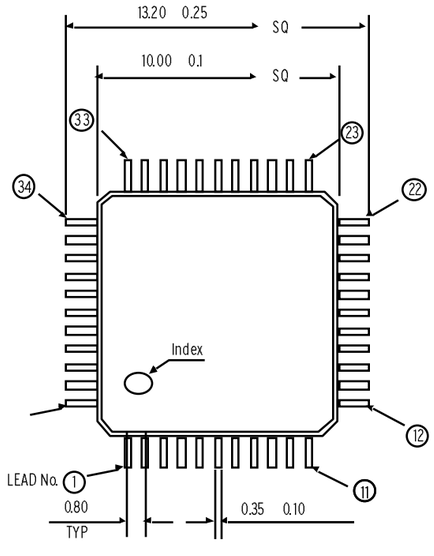

Fig. 5 QFP44 package

KL5C8400

Z80 Mode bus timings

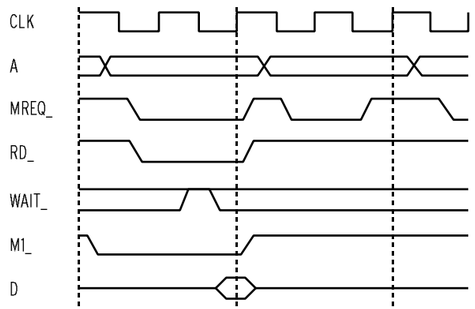

Fig. 6. Z80 Mode Opcode fetch cycle
(0 wait state.)

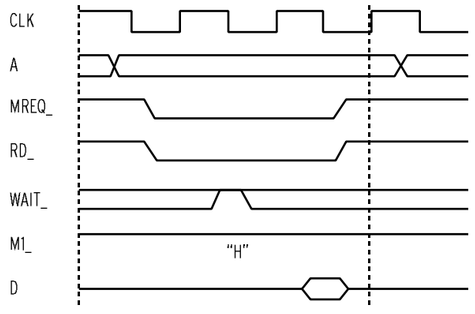

Fig. 7. Z80 Mode Memory read cycle
(0 wait state.)

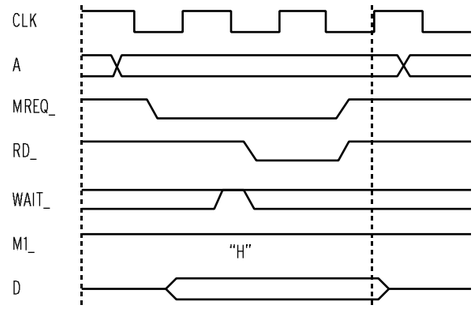

Fig. 8. Z80 Mode Memory write cycle
(0 wait state.)

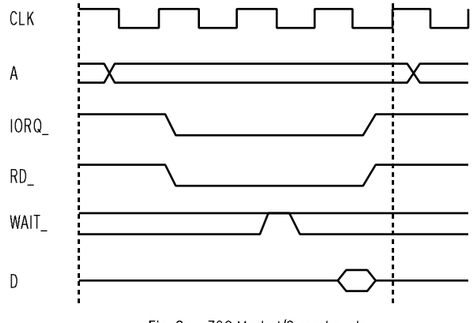

Fig. 9. Z80 Mode I/O read cycle
(0 wait state.)

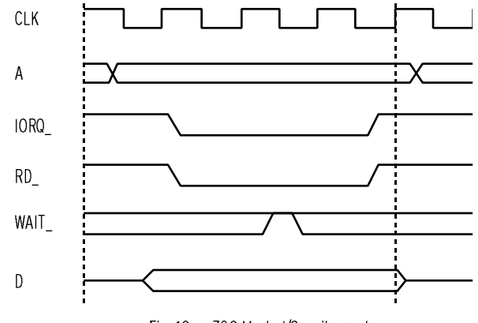

Fig. 10. Z80 Mode I/O write cycle
(0 wait state.)