

CURRENT MODE PWM CONTROL CIRCUITS—YD3843

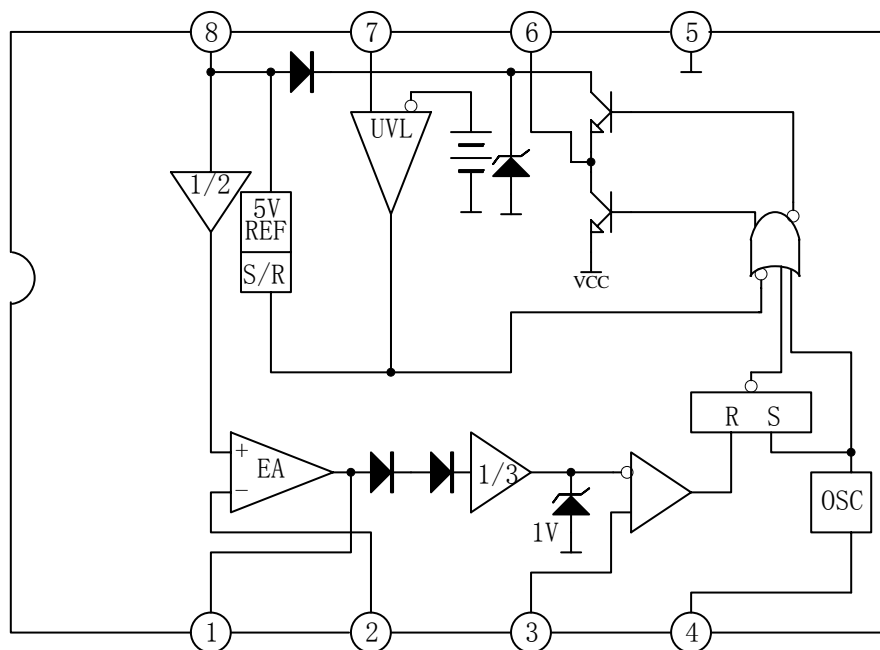
DESCRIPTION

The YD3843 provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count.

FEATURES

- *Optimized for off-line and DC to DC converts
- *Low start up current(<1mA)
- *Automatic feed forward compensation
- *Pulse-by-Pulse current limiting
- *Enhanced load response characteristic
- *Under-voltage lookout with hysteresis.
- *Double pulse Suppression
- *High current totem pole output
- *Internally trimmed band-gap reference
- *500kHz operation
- *Low Ro error amp

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(Tamb=25°C)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage(Low impedance Source)	Vcc	30	V
Supply Voltage(Icc<30mA)	Vcc	Self Limiting	V
Output Current	Io	±1	A
Output Energy(Capacitive Load)		5	μ J
Analog Inputs(pin 2, 3)	VI(ANA)	-0.3 to +6.3	V
Error Amplifier Output Sink Current	ISINK(EA)	10	mA
Power Dissipation	Pd	At Tamb≤25°C 1.0	W
Lead Temperature	Tlead	300	°C
Storage Temperature	Tstg	-65—+150	°C

Note 1: Ta>25°C, Pd derated with 8mW/°C.

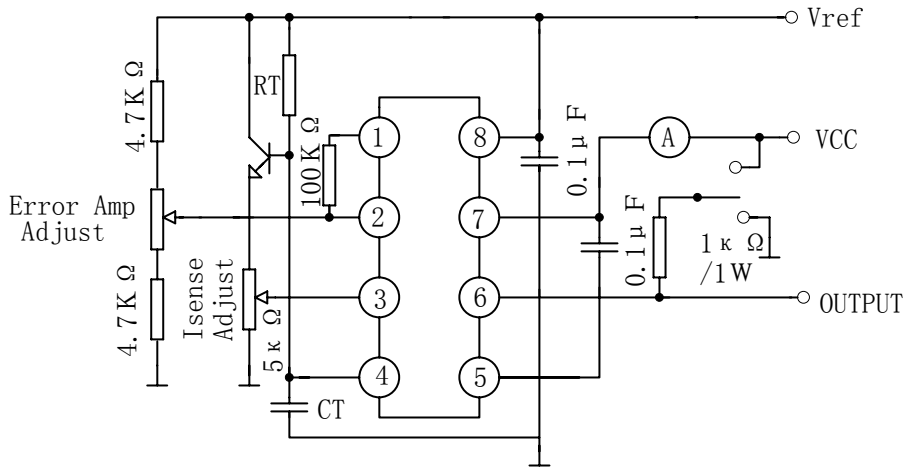
ELECTRICAL CHARACTERISTICS

(Vcc=15V, RT=10kΩ, CT=3.3nF, Tamb=0°C~70°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Output Voltage	VREF	Tj=25°C, Io=1mA	4.90	5.00	5.10	V
Line Regulation	ΔVREF	12≤VIN≤25V		6	20	mV
Load Regulation	ΔVREF	1≤Io=20mA		6	25	MV
Output Noise Voltage	Vose	10Hz≤f≤10kHz, Tj=25°C(note 2)		50	6	mV
Long Term Stability		Ta=25°C, 1000Hrs(note 2)		5	25	mV
Output Short Circuit	Isc		-30	-100	-180	mA
Oscillator Section						
Initial Accuracy	f	Tj=25°C	47	52	57	kHz
Voltage Stability	Δf/ΔVcc	12≤Vcc≤25V		0.2	1	%
Temp Stability		Tmin≤TA≤Tmax(note 2)		5		%
Amplitude	Vosc	Vpin 4 peak to peak		1.7		V
Error Amplifier Section						
Input Voltage	VI(EA)	Vpin 1=2.5V	2.42	2.50	2.58	V
Input Bias Current	IBIAS			-0.3	-2	μ A
AVOL		2≤Vo≤4V	60	90		dB
Unity Gain Bandwidth		Tj=25°C(note 2)	0.7	1	6.0	mHz
PSRR		12≤Vcc≤25V	60	70		dB
Output Sink Current	Isink	Vpin2=2.7V, Vpin 1=1.1V	2	6		mA

Output Source Current	I _{source}	V _{pin 2} =2.3V, V _{pin 1} =5V	-0.5	-0.8		mA
V _{out} High	V _{OH}	V _{pin 2} =2.3V, R _L =15kΩ to GND	5	6		V
V _{out} Low	V _{OL}	V _{pin 2} =2.7V, V _{pin 1} =1.1V		0.7	1.1	V
Current Sense Section						
Gain	G _v	(note 3, 4)	2.85	3	3.15	V/V
Maximum Input Signal	V _{I(MAX)}	V _{pin 1} =5V(note 3)	0.9	1	1.1	V
PSRR		12 ≤ V _{cc} ≤ 25V		70		dB
Input Bias Current	I _{BIAS}			-2	-10	μA
Delay to Output		V _{pin 3} =0 to 2V		150	300	ns
Output Section						
Output Low Level	V _{OL}	I _{sink} =20mA		0.1	0.4	V
		I _{sink} =200mA		1.5	2.2	V
Output High Level	V _{OH}	I _{source} =20mA	13	13.5		V
		I _{source} =200mA	12	13.5		V
Rise Time	t _r	T _j =25°C, C _L =1nF (note 2)		50	150	ns
Fall Time	t _f	T _j =25°C, C _L =1nF(note 2)		50	150	ns
UVLO Saturation		V _{cc} =5V, I _{sink} =10mA		0.7	1.2	V
Under-Voltage Lockout Output Section						
Start Threshold	V _{TH(ST)}		7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	V _{OPR(min)}		7.6	8.0	8.4	V
PWM Section						
Maximum Duty Cycle	D _(MAX)		95	07	100	%
Minimum Duty Cycle	D _(MIN)				0	%
Total Standby Current						
Start-up Current	I _{ST}			0.5	1	mA
Operating Supply Current	I _{CC(OPR)}	V _{pin 2} =V _{pin 3} =0V		11	17	mA
V _{cc} Zener Voltage	V _Z	I _{cc} =25mA		34		V

APPLICATION CIRCUIT



OUTLINE DRAWING

DIP-8

unit:mm

