FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-05604-1E

Microprocessor SPARClite

CMOS

Peripherals for SPARClite

MB86943B

■ DESCRIPTION

The MB86943B is a bus bridge that allows high-speed [data] transfers between the host processor (SPARClite* Family) and the PCI-bus. This bridge chip enables SPARClite (host CPU) access in program mode (direct master operation) to devices on a PCI bus. Also, the SPARClite host can invoke the built-in DMA function on the bridge chip to allow access to devices on the PCI bus. Access from the PCI side to devices on the SPARClite bus (SL bus) is enabled by using the bridge chip slave operation function. The DMA function can be started up from the SL-bus side. The MB86943B supports Door Bell functions and Mail Box function as well.

* : SPARClite is a trademark of SPARC International, Inc. in the United States.
Fujitsu Microelectronics, Inc. has been granted permission to use the trademark.

■ FEATURES

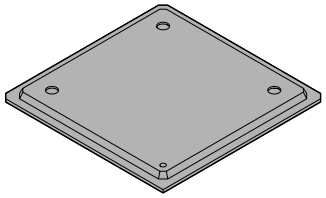
Key hardware features

- Functions for SL-bus to PCI slave (possible to work in program mode)
- Functions for PCI-bus to SL-bus slave (possible to work in program mode)
- Two-channel DMA functions (between the SL-bus and the PCI-bus)
- Functions to access the SL-bus's external areas (ECS0 through ECS2)
- Interrupt communication functions between the SL-bus and the PCI-bus by use of Door Bell and Mail Box.

(Continued)

■ PACKAGE

352-pin Plastic BGA



(BGA-352P-M03)

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Bus bridge features

The host SPARClite can access the PCI-bus's target by use of the chip's PCI-bus direct master functions (Direct Master Operation). Also the PCI-bus's other masters can access the SPARClite bus by use of the chip's PCI-bus direct slave functions (Direct Slave Operation). These functions allow individual bus masters to mutually access the PCI-bus area and SL-bus area. With the Direct Master or the Direct Slave in operation, data are transferred via the 128-byte data buffer, so that a high-speed burst transfer can be achieved.

- Direct Master Operation
  Allows the SL-bus processor to directly access the PCI space.
  Allows high-speed burst transfer via the relevant data buffer.
- Direct Slave Operation
  Allows the PCI-bus master to directly access the SL-bus space.
  Allows high-speed burst transfer via the relevant data buffer.

Provided with two independent DMA channels

- Carries out 32/64-bit transfer.
- Possible to work DMA control from the SL-bus side.
- Bidirectional DMA functions by use of the bidirectional data buffer having a capacity of 128 bytes.
- High-speed data chain mode by use of the built-in registers.
  High Speed Data Chain Mode Using Internal Registers.
  Because DMA descriptors are stored in internal registers there is no need to fetch descriptors from external memory, enabling high speed DMA operations in descriptor chain mode.

Functions to access the SL-bus's external areas

- Pins ECS0 through ECS2 (External Chip Select) allow the access to the SL-bus's external I/Os, the memory via the bridge chip.

Door Bell functions

The functions notify bidirectional interrupts; SL-bus → PCI-bus and PCI-bus → SL-bus.

Mail Box functions

Provided with eight registers possible to perform PCI write/SL read and eight registers possible to perform SL write/PCI read, so that messages can be communicated from both sides. A means is also provided to interrupt from the writing side to the reading side at same time.

The PCI-bus and the SL-bus can operate asynchronously by use of different clocks.

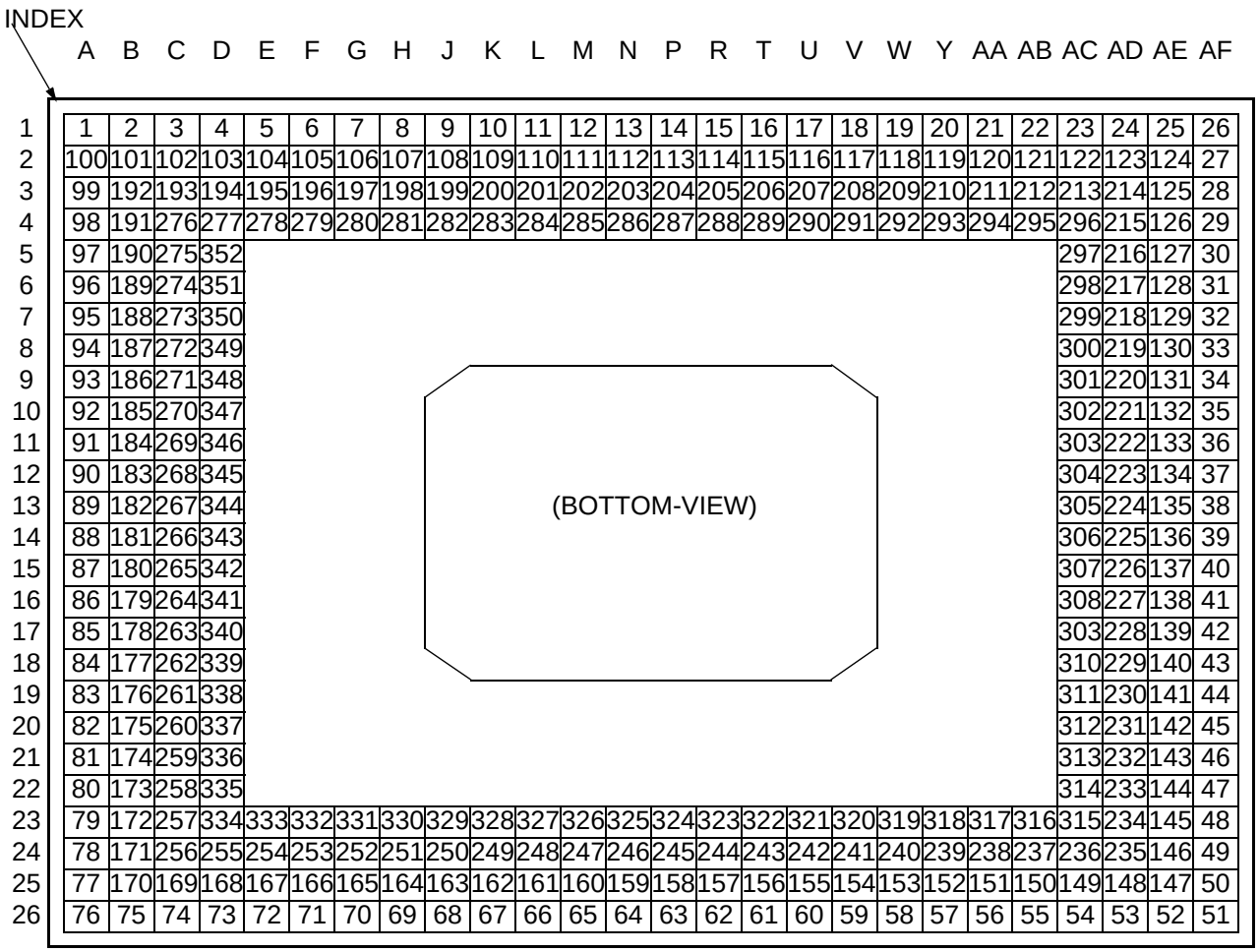
Data bus widths

SL-bus	64/32 bits.
PCI-bus	64/32 bits.

Address bus widths

SL-bus	32 bits (fixed) ADR<1:0> ignored, ASI<3:0> supported.
PCI-bus	64/32 bits.

■ PIN ASSIGNMENT



1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
2	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	27
3	99	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	125	28
4	98	191	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	215	126	29
5	97	190	275	352																			297	216	127	30
6	96	189	274	351																			298	217	128	31
7	95	188	273	350																			299	218	129	32
8	94	187	272	349																			300	219	130	33
9	93	186	271	348																			301	220	131	34
10	92	185	270	347																			302	221	132	35
11	91	184	269	346																			303	222	133	36
12	90	183	268	345																			304	223	134	37
13	89	182	267	344																			305	224	135	38
14	88	181	266	343																			306	225	136	39
15	87	180	265	342																			307	226	137	40
16	86	179	264	341																			308	227	138	41
17	85	178	263	340																			303	228	139	42
18	84	177	262	339																			310	229	140	43
19	83	176	261	338																			311	230	141	44
20	82	175	260	337																			312	231	142	45
21	81	174	259	336																			313	232	143	46
22	80	173	258	335																			314	233	144	47
23	79	172	257	334	333	332	331	330	329	328	327	326	325	324	323	322	321	320	319	318	317	316	315	234	145	48
24	78	171	256	255	254	253	252	251	250	249	248	247	246	245	244	243	242	241	240	239	238	237	236	235	146	49
25	77	170	169	168	167	166	165	164	163	162	161	160	159	158	157	156	155	154	153	152	151	150	149	148	147	50
26	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51

Signals (259 pins); 248 pins of them already used

V_{DD3} (32 pins) Iinternal LOGIC, Power-supply for I/Os	282, 301, 320, 339, 196, 108, 20, 23 287, 306, 325, 344, 299, 131, 45, 48 291, 310, 329, 348, 54, 154, 70, 73 296, 315, 334, 277 79, 177, 270, 98	
V_{DD5} (21 pins) Power-supply for PCI I/Os	281, 300, 319, 338, 194, 198, 112, 15, 209, 212 286, 305, 324, 343, 215, 272, 275 292, 311, 330, 349	
V_{SS} (38 pins) Iinternal LOGIC, GND common to I/Os	1, 26, 51, 76, 195, 6, 285, 288, 210, 121 279, 298, 317, 336, 216, 129, 39, 312 284, 303, 322, 341, 55, 64, 331, 289, 308, 327, 346, 80, 89, 186, 273, 190 294, 313, 332, 351	
VPDP (1 pin) A feed-through current prevention cell	92	When mounted, connected to V_{SS}
OVSENS (1 pin) A power-sensing cell	93	When mounted, connected to V_{SS}

PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-tribute
FJ	JEDEC			FJ	JEDEC			FJ	JEDEC		
1	A1	V_{SS}	V_{SS}	284	L4	V_{SS}	V_{SS}	286	N4	V_{DD5}	V_{DD5}
279	F4	V_{SS}	V_{SS}	109	K2	AD[08]	PCI I/O	19	W1	AD[57]	PCI I/O
282	J4	V_{DD3}	V_{DD3}	10	K1	AD[10]	PCI I/O	290	U4	AD[60]	PCI I/O
2	B1	AD[19]	PCI I/O	201	L3	C/BE[0]#	PCI I/O	117	V2	AD[56]	PCI I/O
101	B2	AD[18]	PCI I/O	110	L2	AD[04]	PCI I/O	207	U3	AD[62]	PCI I/O
103	D2	FRAME#	PCI I/O	202	M3	AD[06]	PCI I/O	20	Y1	V_{DD3}	V_{DD3}
102	C2	AD[17]	PCI I/O	11	L1	AD[07]	PCI I/O	208	V3	AD[58]	PCI I/O
3	C1	C/BE[2]#	PCI I/O	287	P4	V_{DD3}	V_{DD3}	21	AA1	AD[53]	PCI I/O
194	D3	V_{DD5}	V_{DD5}	12	M1	AD[05]	PCI I/O	118	W2	AD[54]	PCI I/O
195	E3	V_{SS}	V_{SS}	285	M4	V_{SS}	V_{SS}	210	Y3	V_{SS}	V_{SS}
278	E4	TRDY#	PCI I/O	112	N2	V_{DD5}	V_{DD5}	209	W3	V_{DD5}	V_{DD5}
4	D1	IRDY#	PCI I/O	111	M2	AD[00]	PCI I/O	22	AB1	AD[51]	PCI I/O
104	E2	(N.C.)	N.C.	13	N1	AD[03]	PCI I/O	119	Y2	AD[55]	PCI I/O
105	F2	STOP#	PCI I/O	203	N3	AD[02]	PCI I/O	293	Y4	AD[52]	PCI I/O
196	F3	V_{DD3}	V_{DD3}	14	P1	AD[01]	PCI I/O	120	AA2	AD[49]	PCI I/O
5	E1	DEVSEL#	PCI I/O	204	P3	REQ64#	PCI I/O	211	AA3	AD[50]	PCI I/O
280	G4	AD[15]	PCI I/O	113	P2	ACK64#	PCI I/O	23	AC1	V_{DD3}	V_{DD3}
106	G2	SERR#	PCI I/O	114	R2	C/BE[6]#	PCI I/O	121	AB2	V_{SS}	V_{SS}
197	G3	PAR	PCI I/O	15	R1	V_{DD5}	V_{DD5}	212	AB3	V_{DD5}	V_{DD5}
198	H3	V_{DD5}	V_{DD5}	288	R4	V_{SS}	V_{SS}	24	AD1	AD[45]	PCI I/O
6	F1	V_{SS}	V_{SS}	16	T1	C/BE[4]#	PCI I/O	295	AB4	AD[48]	PCI I/O
107	H2	AD[12]	PCI I/O	291	V4	V_{DD3}	V_{DD3}	213	AC3	AD[46]	PCI I/O
7	G1	PERR#	PCI I/O	115	T2	PAR64	PCI I/O	122	AC2	AD[47]	PCI I/O
199	J3	AD[13]	PCI I/O	205	R3	C/BE[7]#	PCI I/O	123	AD2	AD[42]	PCI I/O
108	J2	V_{DD3}	V_{DD3}	17	U1	AD[63]	PCI I/O	25	AE1	AD[43]	PCI I/O
200	K3	AD[11]	PCI I/O	206	T3	C/BE[5]#	PCI I/O	214	AD3	AD[44]	PCI I/O
8	H1	C/BE[1]#	PCI I/O	18	V1	AD[59]	PCI I/O	292	W4	V_{DD5}	V_{DD5}
283	K4	AD[09]	PCI I/O	116	U2	AD[61]	PCI I/O	294	AA4	V_{SS}	V_{SS}
9	J1	AD[14]	PCI I/O	289	T4	V_{SS}	V_{SS}	296	AC4	V_{DD3}	V_{DD3}
281	H4	V_{DD5}	V_{DD5}								

V_{DD3} : A 3.3 V power-supply pin (for supplying I/O power and internal power)
V_{DD5} : Either a 5 V power-supply pin or 3.3 V power-supply pin (for supplying power to PCI I/Os)
N.C. : Use this in an open state.

PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-trib-ute	PKG Pin number		Pin name	At-tribute
FJ	JEDEC			FJ	JEDEC			FJ	JEDEC		
26	AF1	V_{SS}	V_{SS}	303	AC11	V_{SS}	V_{SS}	305	AC13	V_{DD5}	V_{DD5}
298	AC6	V_{SS}	V_{SS}	132	AE10	DACK1#	O	44	AF19	ADR<23>	I/O*
301	AC9	V_{DD3}	V_{DD3}	35	AF10	EOP1#	O	309	AC17	ADR<24>	I/O*
27	AF2	AD[41]	PCI I/O	222	AD11	(N.C.)	N.C.	140	AE18	ADR<25>	I/O*
124	AE2	AD[40]	PCI I/O	133	AE11	ADR<2>	I/O*	228	AD17	ADR<26>	I/O*
126	AE4	AD[36]	PCI I/O	223	AD12	ADR<3>	I/O*	45	AF20	V_{DD3}	V_{DD3}
125	AE3	AD[38]	PCI I/O	36	AF11	ADR<4>	I/O*	229	AD18	ADR<27>	I/O*
28	AF3	AD[39]	PCI I/O	306	AC14	V_{DD3}	V_{DD3}	46	AF21	ADR<28>	I/O*
215	AD4	V_{DD5}	V_{DD5}	37	AF12	ADR<5>	I/O*	141	AE19	ADR<29>	I/O*
216	AD5	V_{SS}	V_{SS}	304	AC12	ADR<6>	I/O*	231	AD20	ADR<30>	I/O*
297	AC5	AD[34]	PCI I/O	135	AE13	ADR<7>	I/O*	230	AD19	ADR<31>	I/O*
29	AF4	AD[37]	PCI I/O	134	AE12	ADR<8>	I/O*	47	AF22	(N.C.)	N.C.
127	AE5	AD[33]	PCI I/O	38	AF13	ADR<9>	I/O*	142	AE20	BMREQ#	I/O*
128	AE6	AD[35]	PCI I/O	224	AD13	ADR<10>	I/O*	312	AC20	V_{SS}	V_{SS}
217	AD6	AD[32]	PCI I/O	39	AF14	V_{SS}	V_{SS}	143	AE21	BMACK#	I/O*
30	AF5	(N.C.)	N.C.	225	AD14	ADR<11>	I/O*	232	AD21	ERROR#	I*
299	AC7	V_{DD3}	V_{DD3}	136	AE14	ADR<12>	I/O*	48	AF23	V_{DD3}	V_{DD3}
129	AE7	V_{SS}	V_{SS}	137	AE15	ADR<13>	I/O*	144	AE22	RGSL#	I*
218	AD7	EAS#	O	40	AF15	ADR<14>	I/O*	233	AD22	BMINH#	I*
219	AD8	ECS0#	O	307	AC15	ADR<15>	I/O*	49	AF24	WINDOWS#	I*
31	AF6	ECS1#	O	41	AF16	ADR<16>	I/O*	314	AC22	ASI<0>	I*
130	AE8	ECS2#	O	310	AC18	V_{DD3}	V_{DD3}	234	AD23	ASI<1>	I*
32	AF7	EBMREQ#	O	138	AE16	ADR<17>	I/O*	145	AE23	ASI<2>	I*
220	AD9	EBMACK#	I*	226	AD15	ADR<18>	I/O*	146	AE24	ASI<3>	I*
131	AE9	V_{DD3}	V_{DD3}	42	AF17	ADR<19>	I/O*	50	AF25	SRSTO#	t/s O
221	AD10	DRQ0#	I*	227	AD16	ADR<20>	I/O*	235	AD24	SRSTI#	I*
33	AF8	DACK0#	O	43	AF18	ADR<21>	I/O*	311	AC19	V_{DD5}	V_{DD5}
302	AC10	EOP0#	O	139	AE17	ADR<22>	I/O*	313	AC21	V_{SS}	V_{SS}
34	AF9	DRQ1#	I*	308	AC16	V_{SS}	V_{SS}	315	AC23	V_{DD3}	V_{DD3}
300	AC8	V_{DD5}	V_{DD5}								

* : With a pull-up resistor
V_{DD3} : A 3.3 V power-supply pin (for supplying I/O power and internal power)
V_{DD5} : Either a 5 V power-supply pin or 3.3 V power-supply pin (for supplying power to PCI I/Os)
N.C. : Use this in an open state.

PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-tribute
FJ	JEDEC			FJ	JEDEC			FJ	JEDEC		
51	AF26	V_{SS}	V_{SS}	322	T23	V_{SS}	V_{SS}	324	P23	V_{DD5}	V_{DD5}
317	AA23	V_{SS}	V_{SS}	155	U25	D<0>	I/O*	69	H26	D<22>	I/O*
320	V23	V_{DD3}	V_{DD3}	60	U26	D<1>	I/O*	328	K23	D<23>	I/O*
52	AE26	CLKIN	I	243	T24	D<2>	I/O*	163	J25	DP5	I/O*
147	AE25	TMS	I*	156	T25	D<3>	I/O*	249	K24	D<24>	I/O*
149	AC25	TRST#	I*	244	R24	D<4>	I/O*	70	G26	V_{DD3}	V_{DD3}
148	AD25	TCK	I*	61	T26	D<5>	I/O*	250	J24	D<25>	I/O*
53	AD26	TDO	O	325	N23	V_{DD3}	V_{DD3}	71	F26	D<26>	I/O*
236	AC24	TDI	I*	62	R26	D<6>	I/O*	164	H25	D<27>	I/O*
237	AB24	BREQ#	O	323	R23	D<7>	I/O*	252	G24	D<28>	I/O*
316	AB23	BGRNT#	I*	158	P25	DP7	I/O*	251	H24	D<29>	I/O*
54	AC26	V_{DD3}	V_{DD3}	157	R25	D<8>	I/O*	72	E26	D<30>	I/O*
150	AB25	BRIN#	I*	63	P26	D<9>	I/O*	165	G25	D<31>	I/O*
151	AA25	BGOUT#	O	245	P24	D<10>	I/O*	331	G23	V_{SS}	V_{SS}
238	AA24	PBREQ#	I*	64	N26	V_{SS}	V_{SS}	166	F25	DP4	I/O*
55	AB26	V_{SS}	V_{SS}	246	N24	D<11>	I/O*	253	F24	D<32>	I/O*
318	Y23	BE0#	I/O*	159	N25	D<12>	I/O*	73	D26	V_{DD3}	V_{DD3}
152	Y25	BE1#	I/O*	160	M25	D<13>	I/O*	167	E25	D<33>	I/O*
239	Y24	BE2#	I/O*	65	M26	D<14>	I/O*	254	E24	D<34>	I/O*
240	W24	BE3#	I/O*	326	M23	D<15>	I/O*	74	C26	D<35>	I/O*
56	AA26	BE4#	I/O*	66	L26	DP6	I/O*	333	E23	D<36>	I/O*
153	W25	BE5#	I/O*	329	J23	V_{DD3}	V_{DD3}	255	D24	D<37>	I/O*
57	Y26	BE6#	I/O*	161	L25	D<16>	I/O*	168	D25	D<38>	I/O*
241	V24	BE7#	I/O*	247	M24	D<17>	I/O*	169	C25	D<39>	I/O*
154	V25	V_{DD3}	V_{DD3}	67	K26	D<18>	I/O*	75	B26	DP3	I/O*
242	U24	(N.C.)	N.C.	248	L24	D<19>	I/O*	256	C24	D<40>	I/O*
58	W26	RDWR#	I/O*	68	J26	D<20>	I/O*	330	H23	V_{DD5}	V_{DD5}
321	U23	AS#	I/O*	162	K25	D<21>	I/O*	332	F23	V_{SS}	V_{SS}
59	V26	(N.C.)	N.C.	327	L23	V_{SS}	V_{SS}	334	D23	V_{DD3}	V_{DD3}
319	W23	V_{DD5}	V_{DD5}								

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PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-tribute	PKG Pin number		Pin name	At-tribute
FJ	JEDEC			FJ	JEDEC			FJ	JEDEC		
76	A26	V_{SS}	V_{SS}	341	D16	V_{SS}	V_{SS}	343	D14	V_{DD5}	V_{DD5}
336	D21	V_{SS}	V_{SS}	178	B17	D<62>	I/O*	94	A8	REQ#	PCI O
339	D18	V_{DD3}	V_{DD3}	85	A17	D<63>	I/O*	347	D10	PRST#	PCI I
77	A25	D<41>	I/O*	264	C16	DP0	I/O*	186	B9	V_{SS}	V_{SS}
170	B25	D<42>	I/O*	179	B16	(N.C.)	N.C.	270	C10	V_{DD3}	V_{DD3}
172	B23	D<43>	I/O*	265	C15	READY#	t/s O	95	A7	AD[29]	PCI I/O
171	B24	D<44>	I/O*	86	A16	READYIN#	I	271	C9	GNT#	PCI I
78	A24	D<45>	I/O*	344	D13	V_{DD3}	V_{DD3}	96	A6	AD[27]	PCI I/O
257	C23	D<46>	I/O*	87	A15	RDYOUT#	I	187	B8	AD[30]	PCI I/O
258	C22	D<47>	I/O*	342	D15	MEXC#	t/s O	273	C7	V_{SS}	V_{SS}
335	D22	DP2	I/O*	181	B14	IRQ#	O	272	C8	V_{DD5}	V_{DD5}
79	A23	V_{DD3}	V_{DD3}	180	B15	(N.C.)	N.C.	97	A5	AD[25]	PCI I/O
173	B22	D<48>	I/O*	88	A14	HOST	I*	188	B7	AD[31]	PCI I/O
174	B21	D<49>	I/O*	266	C14	SLD64	I*	350	D7	AD[28]	PCI I/O
259	C21	D<50>	I/O*	89	A13	V_{SS}	V_{SS}	189	B6	AD[26]	PCI I/O
80	A22	V_{SS}	V_{SS}	267	C13	BST8	I*	274	C6	AD[24]	PCI I/O
337	D20	D<51>	I/O*	182	B13	(N.C.)	N.C.	98	A4	V_{DD3}	V_{DD3}
175	B20	D<52>	I/O*	183	B12	TEST0	O	190	B5	V_{SS}	V_{SS}
260	C20	D<53>	I/O*	90	A12	TEST1	O	275	C5	V_{DD5}	V_{DD5}
261	C19	D<54>	I/O*	345	D12	TEST2	O	99	A3	AD[23]	PCI I/O
81	A21	D<55>	I/O*	91	A11	TEST3	O	352	D5	IDSEL	PCI I
176	B19	DP1	I/O*	348	D9	V_{DD3}	V_{DD3}	276	C4	AD[20]	PCI I/O
82	A20	D<56>	I/O*	184	B11	(N.C.)	N.C.	191	B4	C/BE[3]#	PCI I/O
262	C18	D<57>	I/O*	268	C12	(N.C.)	N.C.	192	B3	AD[22]	PCI I/O
177	B18	V_{DD3}	V_{DD3}	92	A10	VPDP	VPDP	100	A2	AD[21]	PCI I/O
263	C17	D<58>	I/O*	269	C11	INTA#	PCI O	193	C3	AD[16]	PCI I/O
83	A19	D<59>	I/O*	93	A9	OVSENSE	OVSNS	349	D8	V_{DD5}	V_{DD5}
340	D17	D<60>	I/O*	185	B10	CLK	PCI I	351	D6	V_{SS}	V_{SS}
84	A18	D<61>	I/O*	346	D11	V_{SS}	V_{SS}	277	D4	V_{DD3}	V_{DD3}
338	D19	V_{DD5}	V_{DD5}								

* : With a pull-up resistor
V_{DD3} : A 3.3 V power-supply pin (for supplying I/O power and internal power)
V_{DD5} : Either a 5 V power-supply pin or 3.3 V power-supply pin (for supplying power to PCI I/Os)
OVSENSE : A power-sensing pin. Usually fixed to L.
TEST0 to TEST3 : TEST pins. Use them in an open state.
N.C. : Use this in an open state.
VPDP : A TEST pin. Usually fixed to L.

■ PIN DESCRIPTION

1. PCI Bus interface (89 pins))

Function class	Pin name	I/O	Number of pins	Description
System	CLK	I	1	A pin for the PCI-bus clock input. The PCI-bus interface operates in synchronization with this clock, up to 33 MHz.
	PRST#	I	1	A pin for the PCI system reset input. A signal for PCI system reset. This signal, when asserted, initializes everything within the companion chip.
Address data bus	AD[31:00]	t/s I/O	32	Pins for the address data signals. The 32 lower-order bits of PCI-bus address data.
	C/BE[3:0]#	t/s I/O	4	Pins for the command byte enable signals for the PCI-bus. In address phase, these pins indicate a PCI-bus command. In data phase, these pins indicate the effective byte lane of AD[31:00].
	PAR	t/s I/O	1	A pin for the PCI-bus parity signal. Indicates the even parity of AD[31:00] and C/BE[3:0]#, 36 signals in total.
Bus control	FRAME#	s/t/s I/O	1	A pin for the frame signal. This signal indicates that the PCI bus cycle is being executed. This pin outputs the master (initiator) signal on the PCI bus. When the MB86943B is the initiator, this pin is used in output state.
	IRDY#	s/t/s I/O	1	A pin for the initiator ready signal. Indicates that the PCI-bus master (initiator) is ready to complete a bus cycle.
	TRDY#	s/t/s I/O	1	A pin for the target ready signal. Indicates that the accessed PCI target (resource) is ready to complete a bus cycle.
	DEVSEL#	s/t/s I/O	1	A pin for the device select signal. Indicates that a PCI target decodes the address on the AD line to respond to a bus cycle.
	STOP#	s/t/s I/O	1	A pin for the stop signal. Indicates that the accessed PCI target is waiting for the bus cycle to finish before the PCI-bus master finishes access in whole or in part.
Bus control	IDSEL	I	1	A pin for the initialize device select signal input. The signal line AD[31:11] is used as the IDSEL signal line for each PCI resource. For this purpose, AD[31:11] are all used as an input pin for any resource. The signal lines AD[31:11] are driven by the PCI-bus master so as to select a specific PCI resource configuration space.
Arbitration control	REQ#	t/s O	1	A pin for the request signal output. A signal that conveys that the companion chip requests the PCI-bus right. With the PRST# signal asserted, this pin is put to a tri-state when involved in a point-to-point signal.

(Continued)

(Continued)

Function class	Pin name	I/O	Number of pins	Description
Arbitration control	GNT#	I	1	A pin for the grant signal input. A signal that notifies that the companion chip gained the PCI-bus from the PCI central arbiter in response to the request for the PCI-bus right made by the companion chip. This is a point-to-point signal.
Error notification	PERR#	s/t/s I/O	1	A pin for the parity error signal. Indicates, in PCI-bus data phase, that a parity error occurred in data transferred on the signal lines - AD, C/BE#, PAR, and PAR64. When data are input to the companion chip, this pin is used for output. When data are output from the companion chip, this pin is used for input.
	SERR#	o/d	1	A pin for the system error signal. Indicates, in PCI-bus address phase, that a parity error occurred in an address transferred on the signal lines - AD, C/BE#, PAR, and PAR64. When an error occurs that the companion chip can detect, the error can be notified as an SERR# by means of making suitable settings in the PCI SERR# Enable Register.
Interrupt notification	INTA#	o/d	1	A pin for the interrupt output. A pin that notifies the PCI-bus of an interrupt. When an error occurs that the companion chip can detect, the error can be notified as an INTA# by means of making suitable settings in the PCI-bus Interrupt Enable Register.
PCI 64-bit expansion	AD[63:32]	t/s I/O	32	Pins for the 64-bit expanded address data signals. The 32 higher-order bits of PCI-bus address data.
	C/BE[7:4]#	t/s I/O	4	Pins for the 64-bit expansion command byte enable signals. Pins for command byte enable signals for the PCI-bus. These pins are meaningless in address phase. In data phase, these pins indicate the effective byte lane of AD[63:32].
	PAR64	t/s I/O	1	A pin for the 64-bit expansion PCI-bus parity signal. Indicates the even parity of AD[63:32] and C/BE[7:4]# 36 signals in total.
	REQ64#	s/t/s I/O	1	A pin for the 64-bit data access request signal. Indicates that the PCI-bus master can execute a 64-bit data bus cycle. When a high-level signal is input to the SLD64 pin with the SPARClite bus being in 64-bit data operation and when the companion chip operates as the PCI bus master, the REQ64# signal is asserted concurrently with the FRAME# signal, and the 64-bit data cycles are always required.
	ACK64#	s/t/s I/O	1	A pin for the 64-bit data access enable signal. Indicates that the accessed PCI target can execute a 64-bit data bus cycle.

Note : t/s : Used as a tri-state output driver
s/t/s : Used as a sustained tri-state output driver
o/d : Used as an open drain output driver
pull up : Built-in pull-up resistance

2. SPARClite bus interface pins (138 pins)

Function class	Pin name	I/O	Number of pins	Description
System clock	CLKIN	I	1	A pin for SPARClite bus clock input. The SPARClite bus interface operates in synchronization with this clock, up to 50 MHz.
Reset	SRSTI#	I pull up	1	A pin for reset input from the SPARClite-bus. When the “L” level is input to this pin, the following operation is activated. (1) Clearing of the SL-bus Init Done bit of the SL-bus Configuration Register. (2) Clearing of the registers other than those related to the PCI Configuration. (3) Assertion of the SRSTO# signal.
	SRSTO#	t/s O	1	A pin for the reset output to the SPARClite-bus. This pin is asserted in one of the instances given below. (1) When the PRST# signal is input. (2) When the SRSTI# signal is input. (3) When “1” is set in the Software Reset bit of the Reset Register, which is related to the PCI Configuration.
Bus definition	HOST	I pull up	1	A pin for the PCI-bus host definition. A pin that decides whether or not the SPARClite should generate PCI configuration cycles as the host CPU of the PCI-bus. This pin is an input pin fixed either to the “L” level or to the “H” level. When the “H” level is being input to this pin: The SPARClite becomes the host CPU of the PCI-bus, and the companion chip is defined as a host bridge. In this instance, use of the SL-bus configuration related PCI Configuration Address Register and the PCI Configuration Address Register allows generation of configuration cycles into the PCI-bus. When the “L” level is being input to this pin: The PCI Configuration Address Register and the PCI Configuration Data Register, which are related to the SL-bus Configuration, are ignored when written and become indeterminate registers when read, so that configuration cycles cannot be generated into the PCI-bus.
	SLD64	I pull up	1	A pin for the SPARClite data bus width definition. A pin that decides the data bus width in the SPARClite-bus cycles in which the companion chip intervenes. This pin is an input pin fixed either to the “L” level or to the “H” level. When the “H” level is being input to this pin: The SPARClite-bus is defined as a 64-bit data width - D<63:0>, BE0# to BE7#, and PARITY0 to PARITY7 are regarded as valid. When the “L” level is being input to this pin: The SPARClite-bus is defined as a 32-bit data width - D<31:0>, BE4# to BE7#, and PARITY4 to PARITY7 are regarded as valid. D<63:32>, BE0# to BE3#, and PARITY0 to PARITY3 assume the state of high input impedance.

(Continued)

Function class	Pin name	I/O	Number of pins	Description
Bus definition	BST8	I pul up	1	A pin for the SPARClite-bus burst transfer length definition. A pin that decides a burst transfer length in the SPARClite-bus cycles in which the companion chip intervenes. This pin is an input pin fixed either to the “L” level or to the “H” level. When the “H” level is being input to this pin: The SPARClite-bus, when subjected to a burst transfer, is defined as an 8-burst transfer. When the “L” level is being input to this pin: The SPARClite bus, when subjected to a burst transfer, is defined as a 4-burst transfer.
Interrupt notification	IRQ#	O	1	A pin for the interrupt signal to the SPARClite. When a cause of interrupt specified by the SL-bus Interrupt Enable Register occurs, this pin is switched to the “L” level to notify the interrupt.

(Continued)

Function class	Pin name	I/O	Number of pins	Description
Address bus	ADR<31:2>	I/O pull up	30	Pins for the address signal. When the companion chip has the bus right: This pin outputs an address signal. This pin is effective over a bus cycle period, and the output value during an idle cycle is not guaranteed. The value sequentially changes under a burst transfer. ADR<5:3> under burst transfer with a 64-bit bus width in operation changes as given below. [For 4-burst transfer] (1) 000→001→010→011 (2) 100→101→110→111 [For 8-burst transfer] 000→001→010→011→100→101→110→111 ADR<4:2> under a burst transfer with a 32-bit bus width in operation changes as given below. [For 4-burst transfer] (1) 000→001→010→011 (2) 100→101→110→111 [For 8-burst transfer] 000→001→010→011→100→101→110→111 When the companion chip doesn't have the bus right: This pin becomes an address input pin to be used to request the direct master access involved in internal registers. When SLD64 = "1" (a 64-bit data width specified) ADR<31:3> is regarded as a valid address in carrying out a single transfer. When a 4-burst transfer is in operation, the 2 lower-order bits ADR<4:3> need to be 00, and when an 8-burst transfer is in operation, the 3 lower-order bits ADR<5:3> need to be 000. In other instances, a burst response called forth by the BMACK# signal is not made, but a single transfer is carried out. When SLD64 = "0" (a 32-bit data width specified) ADR<31:2> is regarded as a valid address in carrying out a single transfer. When a 4-burst transfer is in operation, the lower order 2 bits of address ADR<3:2> need to be 00, and when an 8-burst transfer is in operation, the lower order 3 bits of address ADR<4:2> need to be 000. In other instances, a burst response called forth by the BMACK# signal is not made, but a single transfer is carried out.

(Continued)

Function class	Pin name	I/O	Number of pins	Description
Data bus	D<63:0>	I/O pull up	64	Pins for the data signal. When the companion chip has the bus right: These pin form a bidirectional data bus. If data is of double-word type, the data needs to be aligned to an address of a multiple of 8, if data is of single-word type, the data needs to be aligned to a multiple of 4. D<31:0> is used in 32-bit burst mode. When the companion chip doesn't have the bus right: These pins form a data bus used to access internal registers, the external ECS space, and the PCI space from the SPARClite. Access by use of 64-bit bus width and access by use of 32-bit bus width are supported. Reading from the SPARClite is effected in conformity with a data size requested. In writing, valid bytes are specified by use of BE0# to BE7# for a 64-bit bus width, and by use of BE4# to BE7# for a 32-bit bus width. Specifying discontinuous BE#s is forbidden.
Data bus information	BE0# to BE7#	I/O pull up	8	Pins for the byte enable signal. When SLD64 = "1" (a 64-bit data width specified) The valid bytes enabled for D<63:0> are BE0# to BE7#. When SLD64 = "0" (a 32-bit data width specified) The valid byte enabled for D<31:0> are BE4# to BE7#. When the companion chip has the bus right: These pins output "L"s to valid bytes both in write and read. These signals are effective over a bus cycle. When the companion chip doesn't have the bus right: These pins are for a signal for specifying the valid byte data. In reading, any data of 64-bit width or 32-bit width are regarded as valid. In writing, data corresponding to active BEx#s are written. Discontinuous BEx#s are forbidden.
	PARITY0 to PARITY7	I/O pull up	8	Pins for the parity signals. These are data parity signals. When SLD64 = "1" (a 64-bit data width specified) The parity bits for D<63:0> are PARITY0 to PARITY7. When SLD64 = "0" (a 32-bit data width specified) The parity bits for D<31:0> are PARITY4 to PARITY7. When the companion chip has the bus right: When reading as viewed from the companion chip, these pins work as parity input; when writing, these pins work as parity output. When the companion chip doesn't have the bus right and accessed via the companion chip: When reading as viewed from the SPARClite, these pins work as parity output; when writing, these pins work as parity input.

(Continued)

Function class	Pin name	I/O	Number of pins	Description
Address information	ASI<3:0>	I pull up	4	Pins for the address space identification input signal. When the companion chip has the bus right: These signals are meaningless. When the companion chip doesn't have the bus right: These pins are input pins for the address space identification signals output from the SPARClite. These pins pass input signals used for the SPARClite to intervene in the companion chip and to identify an address space. These pins are sampled at the cycle immediately subsequent to the cycle in which AS# is asserted.
	WINDOWS#	I pull up	1	A pin for the windows input signal. When the companion chip has the bus right: This signal is meaningless. When the companion chip doesn't have the bus right: Some types of SPARClite CPUs do not support every bit of ADR<31:0>. Thus, in using one of SPARClites of such type, inputting the "L" level to this pin allows ADR<31:28> and ASI<3:0> not to be subjected to decoding. This pin is sampled at the cycle immediately subsequent to the cycle in which AS# is asserted.
	RGSL#	I pull up	1	A pin for the register select input signal. When the companion chip has the bus right: This signal is meaningless. When the companion chip doesn't have the bus right: The "L" level signal input to this pin when the SPARClite accesses internal registers of the companion chip. This pin needs to be asserted during the relevant access cycle.

(Continued)

Function class	Pin name	I/O	Number of pins	Description
Cycle control	AS#	I/O pull up	1	A pin for the address strobe signal. When the companion chip has the bus right: An address strobe is output only when “1” is set in the SDRAM Mode bit of the SL-bus Configuration Register. An “L” is asserted for one clock cycle in the first cycle of the bus cycle. When the companion chip doesn’t have the bus right: The address strobe is fed.
	RDWR#	I/O pull up	1	A pin for the read/write signal. When the companion chip has the bus right: This is a read/write signal. An “L” is output if the current cycle is a write cycle; the “H” is output over the period of a read cycle. The output level is kept up from the beginning to the end of the bus cycle. When the companion chip doesn’t have the bus right: This signal specifies the read/write when the SPARClite accesses internal registers, the PCI space, and the ECS space. This pin is sampled at the cycle immediately subsequent to the cycle in which AS# is asserted. And if it is “H”, then read operation is carried out; if it is “L”, then write operation is carried out.
	BMREQ#	I/O pull up	1	A pin for the burst transfer enable signal. When the companion chip has the bus right: A signal for a request for burst transfer toward the SPARClite. Either a direct slave or DMA access occurs only when “1” is set in the SDRAM Mode bit of the SL-bus Configuration Register. If the condition to carry out burst transfer is being satisfied, then make this signal “L” to request burst transfer. At the same time, the EBMREQ# signal is asserted, too. The EBMREQ# signal is deasserted at the same time with the first ready cycle. When the companion chip doesn’t have the bus right: A signal for a request for burst transfer from the SPARClite. The level of this signal is determined at the cycle immediately subsequent to the cycle in which AS# is asserted. If it is “L” and if the timing permits burst transfer, then the burst transfer is performed in response to the BMACK#; if the timing doesn’t permit burst transfer, then a BMACK# response is not made, and only a single transfer is carried out. In accessing an internal register or the ECS space from the SPARClite, the burst transfer is not responded even if a request for burst transfer is asserted.

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Function class	Pin name	I/O	Number of pins	Description
Cycle control	BMACK#	I/O pull up	1	A pin for the burst transfer response signal. When the companion chip has the bus right: This signal is acknowledgment input from the SPARClite in burst mode. If the “L” level is input at the same cycle as READY# with burst transfer requested (with the “L” output to BMREQ#), the burst transfer mode is assumed. (This operation is feasible in both schemes - either the “L” is input in the same cycle as READY# or the “L” was input at a prior cycle and is kept until reaching the cycle of READY#.) When the companion chip doesn’t have the bus right: In an instance in which the SPARClite decodes an address space accessed via the companion chip, this terminal outputs acknowledgment in burst mode.
	BMINH#	I pull up	1	A pin for the burst transfer inhibit input signal. When the companion chip has the bus right: This signal is meaningless. When the companion chip doesn’t have the bus right: An input pin for a signal to disable a burst transfer request. With the “L” input to this pin, the burst response with the BMACK# output is not performed even though a burst transfer is requested from the SPARClite. The level of this signal is determined at the cycle immediately subsequent to the cycle in which AS# is asserted; if it is “L”, the BMACK# output is maintained at the “H” level.
	READY#	t/s O pull up	1	A pin for the ready signal output. When the companion chip has the bus right: If the companion chip has the bus right: This signal is output if a time-out occurs in the built-in ready timer. To make the ready timer effective, a longer time period needs to be set in the ready timer than the amount of wait given to the wait generator in each ECS space and than the setting in the external watchdog timer. When the companion chip doesn’t have the bus right: In reading the internal register or the PCI space from the SPARClite, the “L” is output when data is made ready on the data bus. In writing to the internal register or to the PCI space, the “L” is output when data is taken into the companion chip. In accessing the ECS space from the SPARClite, a ready output signal internally generated comes out of this pin. This pin outputs a ready signal generated by the built-in wait generator. Also, it outputs this signal when a time-out occurs in the built-in ready timer. For this reason, to make the ready timer effective, a longer time period needs to be set in the ready timer than the amount of wait given to the wait generator and than the setting in the external watchdog timer.

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Function class	Pin name	I/O	Number of pins	Description
Cycle control	READYIN#	I pull up	1	A pin for the ready signal input. This is a ready signal input when the companion chip has the bus right. This pin goes “L” when the data is made ready on the data bus in a read cycle or when the data is written in a write cycle. In carrying out burst transfer, ready signals need to be input a predetermined number of times with respect to a single-time assertion of AS# or EAS#.
	RDYOUT#	I pull up	1	A pin for the SPARClite ready signal input. In using the wait generator of the SPARClite to access the ECS space from the SPARClite with no internal READY generated in the companion chip and with no READYIN# input from outside, connect RDYOUT# of the SPARClite to this pin. If the RDYOUT# output pin of the SPARClite has been connected to the READYIN# pin of the companion chip, no connection to this pin is required. In this instance, connect a pull-up resistor to this pin.
	MEXC#	t/s O pull up	1	A pin for the memory access exception signal output. A pin for outputting a memory access exception in a bus cycle of the SPARClite in which the companion chip intervenes. This signal is output together with the READY# signal when a time-out occurs in the built-in ready timer.
	ERROR#	I pull up	1	A pin for the error notification signal input. An input pin for error notification signal from the SPARClite. When “1” is set in the SPARC_Error bit of the PCI-bus Interrupt Enable Register, an INTA# interrupt into the PCI-bus is asserted when the “L” level is input to this pin. This behavior has no effect on the companion chip’s operation.

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Function class	Pin name	I/O	Number of pins	Description
Bus right control	BREQ#	O	1	A pin for the bus use right request signal output. A request signal for the bus use right passed from the companion chip to the SAPRClite. This signal is output when a SPARClite-bus request by means of DMA or a direct slave request occurs, or when the bus right is requested by a daisy-chain-connected device by means of the BRIN# signal input. The BREQ# signal is asserted when the BGRNT# signal is deasserted.
	BGRNT#	I pull up	1	A pin for the bus grant signal input. A signal enabling the bus right passed from the SPARClite to BREQ#. When the companion chip receives this signal, it either starts a transaction or outputs BGOUT# to a daisy-chain-connected device, and enables the bus right. Once BGRNT# is asserted to BREQ#, BGRNT# must not be deasserted until BREQ# is deasserted. If violated, the operation is not guaranteed.
	PBREQ#	I pull up	1	A pin for the bus-release request signal input. A pin for a bus-release request signal input from the SPARClite. If the “L” level is input to this pin while the companion chip retains the bus right, the bus-release request is canceled after the current cycle is completed or after the transfer on a cache line size basis is completed.
	BRIN#	I pull up	1	A pin for the bus-use right request signal input. A pin for a bus-use request signal input from a daisy-chain-connected device. The “L” level input to this pin enables the BREQ# to request for the SAPRClite-bus. If the bus right is enabled by BGRNT# at this moment, this terminal outputs BGOUT# after a round robin arbitration within the companion chip, and enables a daisy-chain-connected device to use the bus right. The assertion of BRIN# needs to be effected at the time when the BGOUT# signal is deasserted.
	BGOUT#	O	1	A pin for the bus-use right enabling signal output. A pin for a bus-use enabling signal output to a daisy-chain-connected device.

3. External ECS space control pins (6 pins)

Function class	Pin name	I/O	Number of pins	Description
ECS space control	EAS#	O	1	A pin for the address strobe signal output to the ECS space. When the companion chip has the bus right: This pin outputs an address strobe. The “L” is asserted for the first one clock cycle of the bus cycle. When the companion chip doesn’t have the bus right: This signal is meaningless.
	ECS[0:2]#	O	3	Pins for outputting a chip select signal to pick the ECS space. When the companion chip has the bus right: Pins for outputting a chip select signal to pick the ECS space. This signal is effective over a bus cycle period, and is negated during an idle cycle. When the companion chip doesn’t have the bus right: When the APARClite accesses the ECS space, these pins are used to output a chip select signal to pick the ECS space. This signal is effective over a bus cycle period started by EAS#, and is negated during an idle cycle.
	EBMREQ#	O	1	A pin for outputting a signal requesting burst transfer to the ECS space. When the companion chip has the bus right: A signal requesting the burst transfer to the ECS space. If either a direct slave or DMA access occurs and if the condition for burst transfer has been satisfied, this signal goes “L” and the burst transfer is requested. The deasserts this signal concurrently with the first ready cycle. When the companion chip doesn’t have the bus right: This pin switches to “H” level output.
	EBMACK#	I pull up	1	A pin for inputting a signal responding to burst transfer from the ECS space. When the companion chip has the bus right: This signal is acknowledgment input from the ECS space in burst transfer mode. If the “L” level is input in the same cycle as READYIN# when the burst transfer is requested by EBMREQ# (with the “L” output to EBMREQ#), the switches to burst transfer mode. (This operation is feasible in both schemes - either the “L” is input in the same cycle as READYIN# or the “L” was input in a prior cycle and is kept until reaching the cycle of READYIN#.) When the companion chip doesn’t have the bus right: This signal is meaningless.

4. DMAC control pins (6 pins)

Function class	Pin name	I/O	Number of pins	Description
DMA control	DREQ0#, DREQ1#	I pull up	2	Pins for DMA request signal input. A signal that requests the start of transfer when the built-in DMAC is started up in external startup mode. Since this signal is triggered at the “L” level, this signal needs to be kept asserted until the DACK0, 1# is encountered.
	DACK0#, DACK1#	O	2	Pins for DMA acknowledgment signal output. An acknowledgment signal indicating that the DREQ0, 1# is accepted. This signal is asserted concurrently with EAS#.
	EOP0#, EOP1#	O	2	Pins for DMA end signal output. A signal for the end of process. This signal indicates that transfer on a descriptor basis involved in DMA has been completed. This signal is asserted over a time period where the closing READYIN# is waited for to be input.

5. JTAG pins (5 pins)

Function class	Pin name	I/O	Number of pins	Description
JTAG	TDI	I pull up	1	A pin for JTAG test data input. A pin for inputting data used in testing JTAG. Have this pin stay “H” level except when enabling the JTAG features.
	TMS	I pull up	1	A pin for JTAG test mode input. A pin for inputting a mode setting used in testing JTAG. Have this pin stay “H” level except when enabling the JTAG features.
	TCLK	I pull up	1	A pin for JTAG test clock input. A pin for inputting a clock used in testing JTAG. Have this pin stay “H” level except when enabling the JTAG features.
	TRST#	I pull up	1	A pin for JTAG test reset input. A pin for inputting reset used in testing JTAG. Have this pin stay “H” level except when enabling the JTAG features.
	TDO	O	1	A pin for JTAG test data output. A pin for outputting data used in testing JTAG.

6. TEST pins (4 pins)

Function class	Pin name	I/O	Number of pins	Description
TEST pins	TEST0, TEST1, TEST2, TEST3	O	4	Pins for test output. Leave them open.

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage (PCI I/O)	V_{DD5}	–0.5	6.0	V
Power supply voltage (SPARClite I/O, internal)	V_{DD3}	–0.5	4.0	V
Input voltage (PCI I/O)	V_{I5}	–0.5	V_{DD5} + 0.5	V
Input voltage (SPARClite I/O)	V_{I3}	–0.5	V_{DD3} + 0.5	V
Storage ambient temperature	T_{STG}	–55	125	°C
Overshoot	—	Within V_{DD} + 0.1 V (Within 50 ns)		—
Undershoot	—	Within V_{SS} – 0.1 V (Within 50 ns)		—

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage (PCI I/O)	V_{DD5} = 5 V	V_{DD5}	4.75	5.0	5.25	V
	V_{DD5} = 3.3 V		3.15	3.3	3.45	V
Power supply voltage (SPARClite I/O,internal)		V_{DD3}	3.15	3.3	3.45	V
“L” level input voltage		V_{IL}	–0.3	—	0.8	V
“H” level input voltage (PCI I/O)		V_{IH5}	2.0	—	V_{DD5} + 0.3	V
“H” level input voltage (SPARClite I/O,internal)		V_{IH3}	2.0	—	V_{DD3} + 0.3	V
Operating ambient temperature		Ta	0	25	70	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating conditionranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRIC CHARACTERISTICS

1. DC Characteristics

(V_{SS} = 0.0 V, Ta = 0 °C to +70 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
"L" level input voltage	V_{IL}	—	0	—	0.8	V
"H" level input voltage (PCI)	V_{IH5}	—	2.0	—	V_{DD5}	V
"H" level input voltage	V_{IH3}	—	2.0	—	V_{DD3}	V
"L" level output voltage	V_{OL}	I_{OL} = 2 mA	0	—	0.4	V
"H" level output voltage (PCI)	V_{OH5}	I_{OH} = –2 mA	V_{DD5} – 0.5	—	V_{DD5}	V
"H" level output voltage	V_{OH3}	I_{OH} = –2 mA	V_{DD3} – 0.5	—	V_{DD3}	V
Input leakage current	I_{LI}	V_{IN} = 0 or V_{DD}	–5	—	5	µA
Trial state output leakage current	I_{LZ}	V_{OUT} = 0 or V_{DD}	–5	—	5	µA
Power supply current (V_{DD5})	I_{DD}	—	—	TBD	TBD	mA
Power supply current (V_{DD3})		—	—	TBD	TBD	mA
Power consumption (V_{DD5} + V_{DD3})	P_D	—	—	TBD	TBD	W
Pin capacity (PCI pin)	C_{PIN}	V_{DD5} = V_{DD3} = V_I = 0, f = 1 MHz, 25 °C	—	—	18	pF
Pin capacity (pins other than PCI pin)			—	—	16	

2. AC Characteristics

Cautions for the measurement are as follows:

- Each parameter, unless otherwise specified, is valid within the specified temperature range and power supply range.
- Each voltage is measured with respect to the GND (V_{SS} = 0 V) level. The reference point for measuring timing is 1.5 V, the input level is from 0.4 V through 2.4 V, the rise time and the fall time of incoming signal are not more than 1.5 V ns.
- Do not short-circuit two or more output pins for one second or longer.
- The external output capacitive load is 50 pF.

(1) SPARClite-IF

All SPARClite interface AC characteristics are defined from the rising edge of the CLKIN signal.

- Clock input

(Ta = 0 °C to +70 °C)

Parameter	Pin name	Value		Unit
		Min.	Max.	
CLKIN period	CLKIN	20	CLK period × 3	ns
CLKIN "H" time	CLKIN	8	—	ns
CLKIN "L" time	CLKIN	8	—	ns
CLKIN rise time	CLKIN	—	2	ns
CLKIN fall time	CLKIN	—	2	ns

• Output

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value		Unit
			Min.	Max.	
Data signal	Output valid delay	D<63:0>	—	13	ns
	Output hold		2	—	
An address signal	Output valid delay	ADR<31:2>	—	13	ns
	Output hold		2	—	
Parity signals	Output valid delay	PARITY0 to PARITY7	—	13	ns
	Output hold		2	—	
A signal for byte enabling	Output valid delay	BE0# to BE7#	—	13	ns
	Output hold		2	—	
A signal for address strobe	Output valid delay	AS#	—	13	ns
	Output hold		2	—	
Read/write signal	Output valid delay	RDWR#	—	13	ns
	Output hold		2	—	
Bus use right request signal	Output valid delay	BREQ#	—	13	ns
	Output hold		2	—	
A signal for burst transfer request	Output valid delay	BMREQ#	—	13	ns
	Output hold		2	—	
A signal for burst transfer response	Output valid delay	BMACK#	—	13	ns
	Output hold		2	—	
Ready signal output	Output valid delay	READY#	—	13	ns
	Output hold		2	—	
Memory access exception signal output	Output valid delay	MEXC#	—	13	ns
	Output hold		2	—	
Bus use right enable signal	Output valid delay	BGOUT#	—	13	ns
	Output hold		2	—	
An interrupt signal	Output valid delay	IRQ#	—	13	ns
	Output hold		2	—	
Bus reset output signal	Output valid delay	SRSTO#	—	13	ns
	Output hold		2	—	

• Input

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value		Unit
			Min.	Max.	
A signal for address space identification input	Input setup time	ASI<3:0>	6	—	ns
	Input hold time		2	—	
An address signal	Input setup time	ADR<31:2>	6	—	ns
	Input hold time		2	—	
Data signal	Input setup time	D<63:0>	6	—	ns
	Input hold time		2	—	
Parity signal	Input setup time	PARITY0 to PARITY7	6	—	ns
	Input hold time		2	—	
A signal for byte enabling	Input setup time	BE0# to BE7#	6	—	ns
	Input hold time		2	—	
A signal for address strobe	Input setup time	AS#	6	—	ns
	Input hold time		2	—	
A signal for burst transfer request	Input setup time	BMREQ#	6	—	ns
	Input hold time		2	—	
A signal for burst transfer response	Input setup time	BMACK#	6	—	ns
	Input hold time		2	—	
Bus grant signal	Input setup time	BGRNT#	6	—	ns
	Input hold time		2	—	
Bus-use right request signal	Input setup time	BRIN#	6	—	ns
	Input hold time		2	—	
Bus-release request signal	Input setup time	PBREQ#	6	—	ns
	Input hold time		2	—	
Ready signal input	Input setup time	READYIN#	6	—	ns
	Input hold time		2	—	
SPARClite ready signal input	Input setup time	RDYOUT#	6	—	ns
	Input hold time		2	—	
A signal for register select input	Input setup time	RGSL#	6	—	ns
	Input hold time		2	—	
A signal for windows input	Input setup time	WINDOWS#	6	—	ns
	Input hold time		2	—	
A signal for burst transfer inhibit input	Input setup time	BMINH#	6	—	ns
	Input hold time		2	—	
Error notification signal	Input setup time	ERROR#	6	—	ns
	Input hold time		2	—	
Bus reset input signal	Input setup time	SRSTI#*	Asynchronous Only the width specified		ns
	Input hold time				
Data bus width definition signal	Input setup time	SLD64	Used by being tied to “H” or “L”		ns
	Input hold time		Used by being tied to “H” or “L”		
Bus host definition signal	Input setup time	HOST	Used by being tied to “H” or “L”		ns
	Input hold time		Used by being tied to “H” or “L”		
Bus burst transfer length signal	Input setup time	BST8	Used by being tied to “H” or “L”		ns
	Input hold time		Used by being tied to “H” or “L”		

* : RESET input from SPARClite-bus (SRSTI#) requires at least 16 CLKIN cycles.

(2) External ECS Space Control Signals

All AC characteristics of the signals given below are defined from the rising edge of the CLKIN signal.

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value		Unit
			Min.	Max.	
An address strobe signal to the ECS space	Output valid delay	EAS#	—	13	ns
	Output hold		2	—	
A chip select signal to pick the ECS space	Output valid delay	ECS0# to ECS2#	—	13	ns
	Output hold		2	—	
A signal requesting burst transfer to the ECS	Output valid delay	EBMREQ#	—	13	ns
	Output hold		2	—	
A signal responding to burst transfer from the	Input setup time	EBMACK#	6	—	ns
	Input hold time		2	—	

(3) DMAC Control Signals

All AC characteristics of the signals given below are defined from the rising edge of the CLKIN signal.

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value		Unit
			Min.	Max.	
DMA acknowledgment signal	Output valid delay	DACK0#, DACK1#	—	13	ns
	Output hold		2	—	
DMA end signal	Output valid delay	EOP0#, EOP1#	—	13	ns
	Output hold		2	—	
DMA request signal	Input setup time	DRQ0#, DRQ1#	6	—	ns
	Input hold time		2	—	

(4) PCIbus-IF

All PCIbus interface AC characteristics are defined from the rising edge of the CLKIN signal.

- Clock input

(Ta = 0 °C to +70 °C)

Parameter	Pin name	Value				Unit
		V_{DD5} = 3.3 V		V_{DD5} = 5 V		
		Min.	Max.	Min.	Max.	
CLKIN period	CLK	30	CLKIN period × 3	30	CLKIN period × 3	ns
CLKIN “H” time	CLK	13	—	13	—	ns
CLKIN “L” time	CLK	13	—	13	—	ns
CLKIN rise time	CLK	—	2	—	2	ns
CLKIN fall time	CLK	—	2	—	2	ns

• Output

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value				Unit
			V_{DD5} = 3.3 V		V_{DD5} = 5 V		
			Min.	Max.	Min.	Max.	
Address data signal	Output valid delay	AD[31:00]	—	12	—	14	ns
	Output hold		2	—	2	—	
Command byte enable signal	Output valid delay	C/BE[3:0]#	—	12	—	14	ns
	Output hold		2	—	2	—	
PCI bus parity signal	Output valid delay	PAR	—	12	—	14	ns
	Output hold		2	—	2	—	
Frame signal	Output valid delay	FRAME#	—	11	—	11	ns
	Output hold		2	—	2	—	
Initiator ready signal	Output valid delay	IRDY#	—	11	—	11	ns
	Output hold		2	—	2	—	
Target ready signal	Output valid delay	TRDY#	—	11	—	11	ns
	Output hold		2	—	2	—	
Stop signal	Output valid delay	STOP#	—	11	—	11	ns
	Output hold		2	—	2	—	
Device select signal	Output valid delay	DEVSEL#	—	11	—	11	ns
	Output hold		2	—	2	—	
Request signal	Output valid delay	REQ#	—	11	—	11	ns
	Output hold		2	—	2	—	
Parity error signal	Output valid delay	PERR#	—	11	—	11	ns
	Output hold		2	—	2	—	
System error signal	Output valid delay	SERR#	Asynchronous 1 CLK cycle at the minimum				ns
	Output hold						
Interrupt notification signal	Output valid delay	INTA#	Asynchronous				ns
	Output hold						

- 64-bit expansion output

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value				Unit
			V_{DD5} = 3.3 V		V_{DD5} = 5 V		
			Min.	Max.	Min.	Max.	
64-bit expanded address data signals	Output valid delay	AD[63:32]	—	12	—	14	ns
	Output hold		2	—	2	—	
64-bit expansion command byte enable signals	Output valid delay	C/BE[7:4]#	—	12	—	14	ns
	Output hold		2	—	2	—	
64-bit expansion PCI bus parity signal	Output valid delay	PAR64	—	12	—	14	ns
	Output hold		2	—	2	—	
64-bit data access request signal	Output valid delay	REQ64#	—	12	—	14	ns
	Output hold		2	—	2	—	
64-bit data access enable signal	Output valid delay	ACK64#	—	12	—	14	ns
	Output hold		2	—	2	—	

• Input

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value		Unit
			Min.	Max.	
An address data signal	Input setup time	AD[31:00]	7	—	ns
	Input hold time		1	—	
Command byte enable signal	Input setup time	C/BE[3:0]#	7	—	ns
	Input hold time		1	—	
PCI bus parity signal	Input setup time	PAR	7	—	ns
	Input hold time		1	—	
Frame signal	Input setup time	FRAME#	7	—	ns
	Input hold time		1	—	
Initiator ready signal	Input setup time	IRDY#	7	—	ns
	Input hold time		1	—	
Target ready signal	Input setup time	TRDY#	7	—	ns
	Input hold time		1	—	
Stop signal	Input setup time	STOP#	7	—	ns
	Input hold time		1	—	
Device select signal	Input setup time	DEVSEL#	7	—	ns
	Input hold time		1	—	
Request signal	Input setup time	REQ#	7	—	ns
	Input hold time		1	—	
Parity error signal	Input setup time	PERR#	7	—	ns
	Input hold time		1	—	
System error signal	Input setup time	SERR#	7	—	ns
	Input hold time		1	—	
Initialize device select signal	Input setup time	IDSEL#	7	—	ns
	Input hold time		1	—	
PCI system reset signal	Input setup time	PRST#*	Asynchronous Only the width specified		ns
	Input hold time				

*: RESET input for PCI-bus (PRST#)requires at least 16 CLK cycles.

- 64-bit expansion input

(Ta = 0 °C to +70 °C)

Parameter		Pin name	Value		Unit
			Min.	Max.	
64-bit expanded address data signals	Input setup time	AD[63:32]	7	—	ns
	Input hold time		1	—	
64-bit expansion command byte enable signals	Input setup time	C/BE[7:4]#	7	—	ns
	Input hold time		1	—	
64-bit expansion PCI bus parity signal	Input setup time	PAR64	7	—	ns
	Input hold time		1	—	
64-bit data access request signal	Input setup time	REQ64#	7	—	ns
	Input hold time		1	—	
64-bit data access enable signal	Input setup time	ACK64#	7	—	ns
	Input hold time		1	—	

(5) Other Signals

(Ta = 0 °C to +70 °C)

Parameter	Pin name	Value		Unit
		Min.	Max.	
Test pin	TEST0, TEST1, TEST2, TEST3	Open		—

■ CAUTIONS AS TO BOARD WRITING

- In connecting the power source and GND, use multiple V_{DD} and V_{SS} pins. For the system board in which MB86943B is used, use a multi-layer board that includes the power (V_{DD}) and GND (V_{SS}) so as to supply stable power. Leave pins labeled “N.C.” non-connected.
- Insert a sufficient decoupling capacitor close to MB86943B. There is a possibility that the fluctuations in output level on a number of pins (especially those with a large capacitive load) among output pins of MB86943B have an effect that causes power supply to vary.
- For a system that operates at a high frequency, a low-inductance capacitor and interconnection are recommended. The inductance can be decreased by means of making the distance between MB86943B and the decoupling capacitor short.
- MB86943B requires two power supply systems - V_{DD5} (5 V or 3.3 V system) and V_{DD3} (3.3 V system). To power on or shut off them, follow the steps in sequence given below.

  To power on $V_{DD3} \rightarrow V_{DD5} \rightarrow$ Signal

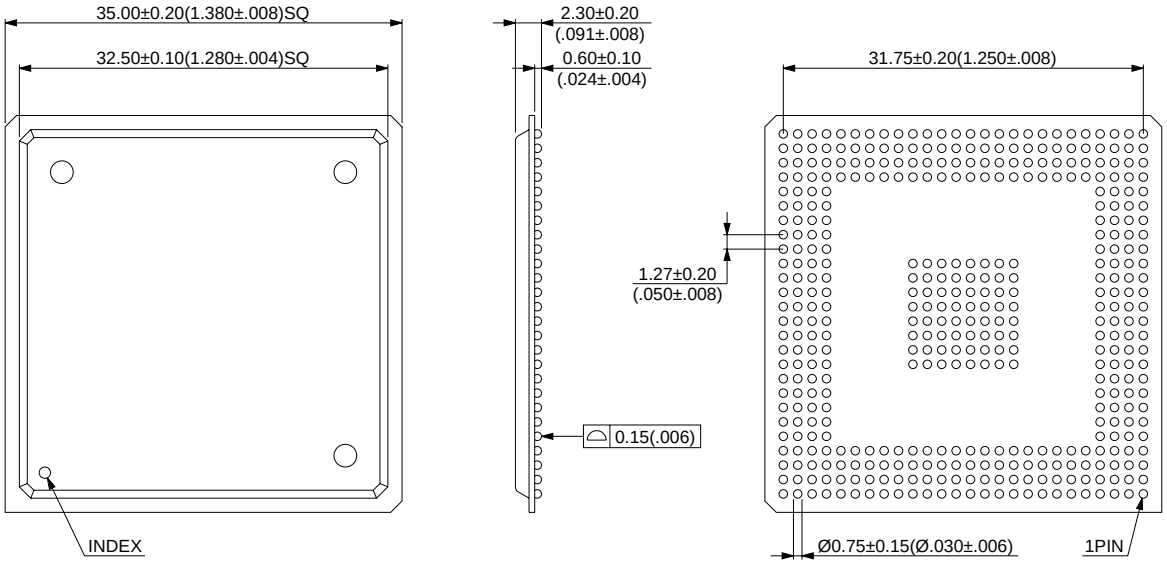
  To shut off Signal $\rightarrow V_{DD5} \rightarrow V_{DD3}$

■ ORDERINGINFORMATION

Part number	Package	Remarks
MB86943BPB	352-pin Plastic BGA (BGA-352P-M03)	

■ PACKAGE DIMENSION

352-pin Plastic BGA
(BGA-352P-M03)



Dimensions in mm (inches)

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