FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

ICS844001-21

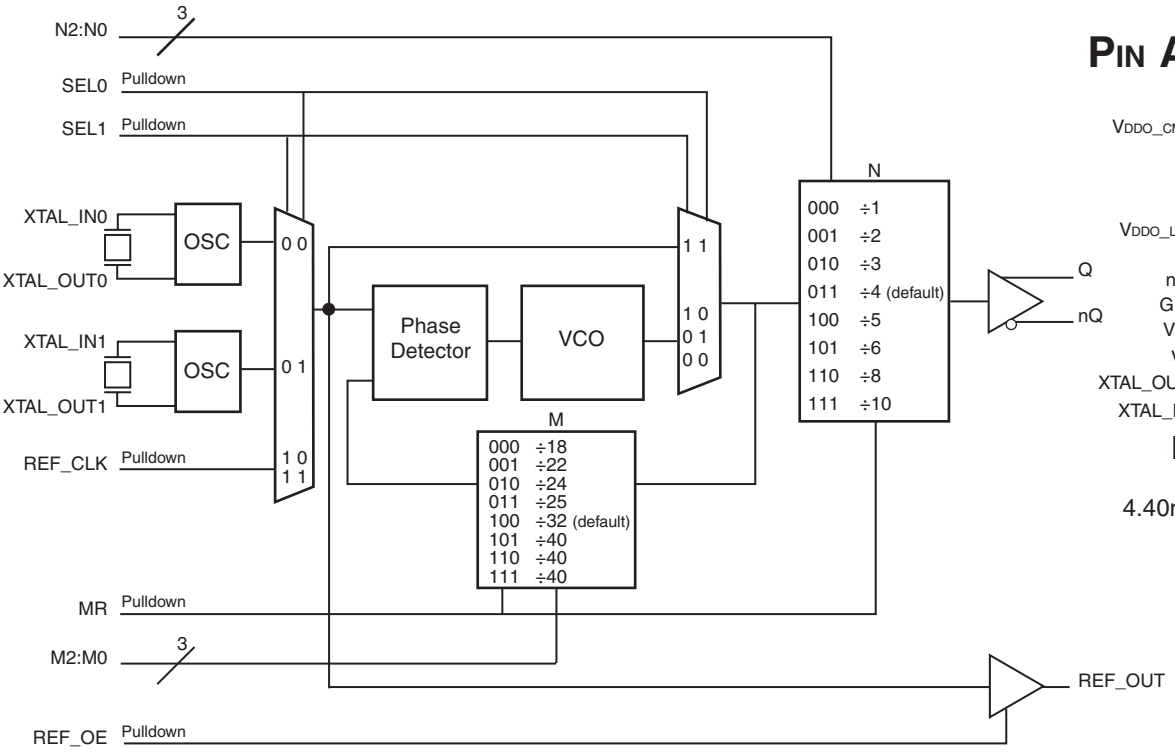
General Description

The ICS844001-21 is a a highly versatile, low phase noise LVDS Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 25.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The ICS844001-21 is packaged in a small 24-pin TSSOP package.

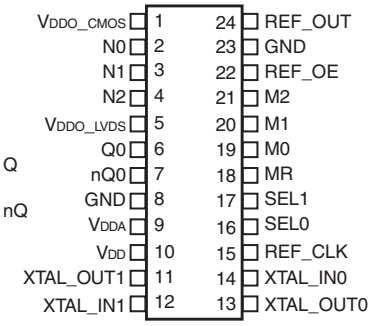
Features

- One differential LVDS output pair and one LVCMOS reference output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 560MHz - 700MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.92ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS844001-21
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDO_CMOS}	Power		Output supply pin for LVCMOS output.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default ÷4. LVCMOS/LVTTL interface levels.
4	N2	Input	Pulldown	
5	V_{DDO_LVDS}	Power		Output supply pin for LVDS outputs.
6, 7	Q, nQ	Ouput		Differential output pair. LVDS interface levels.
8, 23	GND	Power		Power supply ground.
9	V_{DDA}	Power		Analog supply pin.
10	V_{DD}	Power		Core supply pin.
11 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS/LVTTL interface levels.
16, 17	SEL0, SEL1	Input	Pulldown	MUX select pins. LVCMOS/LVTTL interface levels.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default ÷32. LVCMOS/LVTTL interface levels.
21	M2	Input	Pullup	
22	REF_OE	Input	Pulldown	Reference clock output enable. Default Low. LVCMOS/LVTTL interface levels.
24	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{out}	Output Impedance	REF_OUT			7		Ω

TABLE 3A. COMMON CONFIGURATIONS TABLE

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
24.75	24	8	594	74.25	HDTV
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	3	562.5	187.5	12 Gig Ethernet

TABLE 3B. PROGRAMMABLE M DIVIDER FUNCTION TABLE

Inputs			M Divider Value	Input Frequency (MHz)	
M2	M1	M0		Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0 (default)
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

TABLE 3C. PROGRAMMABLE N DIVIDER FUNCTION TABLE

Inputs			N Divide Value
N2	N1	N0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4 (default)
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

TABLE 3D. BYPASS MODE FUNCTION TABLE

Inputs		Reference	PLL Mode
SEL1	SEL0		
0	0	XTAL0	Active (default)
0	1	XTAL1	Active
1	0	REF_CLK	Active
1	1	REF_CLK	Bypass

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Outputs, V_O (LVCMOS)	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_LVDS} = V_{DDO\_CMOS}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
$V_{DDO\_LVDS, \_CMOS}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			110		mA
I_{DDA}	Analog Supply Current			15		mA
$I_{DDO\_LVDS, \_CMOS}$	Output Supply Current			40		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO\_CMOS}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, SEL0, SEL1, OE_REF, MR, M0, M1, N2	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		M2, N0, N1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_CLK, SEL0, SEL1, OE_REF, MR, M0, M1, N2	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		M2, N0, N1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1	REF_OUT		2.6			V
V_{OL}	Output Low Voltage: Note 1	REF_OUT				0.5	V

NOTE 1: Output terminated with 50Ω to V_{DDO_CMOS}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit Diagram".

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO\_LVDS}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.5		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

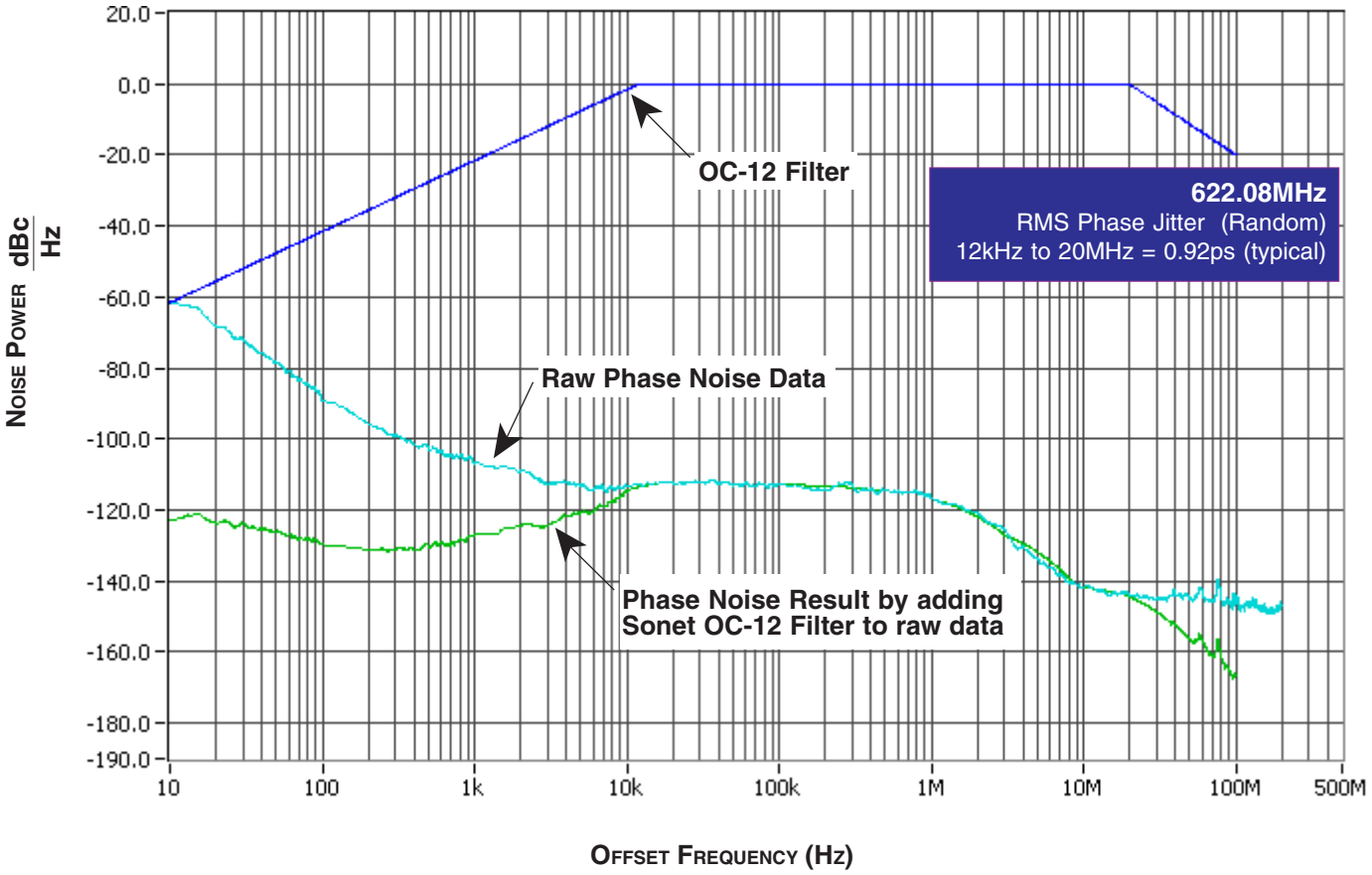
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_LVDS} = V_{DDO\_CMOS}$ = 3.3V±5%, TA = 0°C TO 70°C

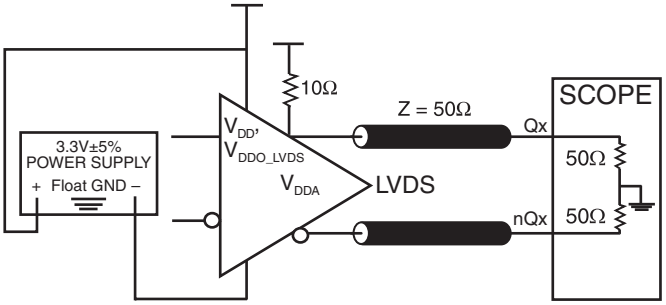
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			56		700	MHz
t_{PD}	Propagation Delay, NOTE 1	REF_CLK to REF_OUT			2.95		ns
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 2, 3		622.08MHz (12kHz - 20MHz)		0.92		ps
t_R / t_F	Output Rise/Fall Time	Q, nQ	20% to 80%		300		ps
		REF_OUT	20% to 80%		300		ps
odc	Output Duty Cycle	Q, nQ			50		%
		REF_OUT			50		%

NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO_CMOS}/2 of the output.
NOTE 2: Phase jitter measured using a 25MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

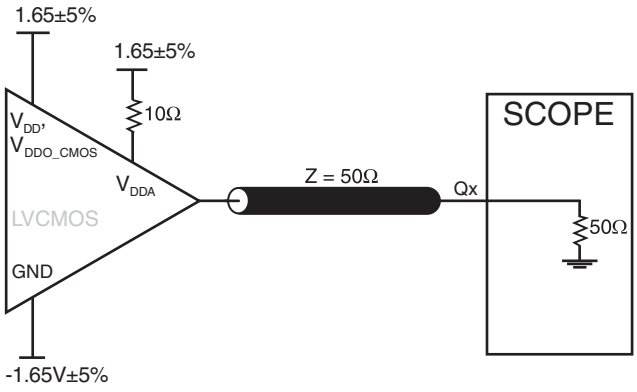
Typical Phase Noise at 622.08MHz



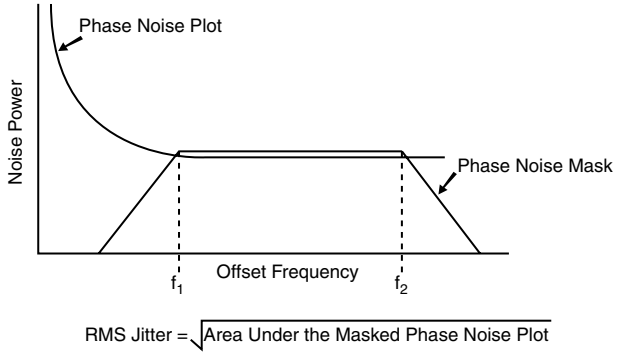
PARAMETER MEASUREMENT INFORMATION



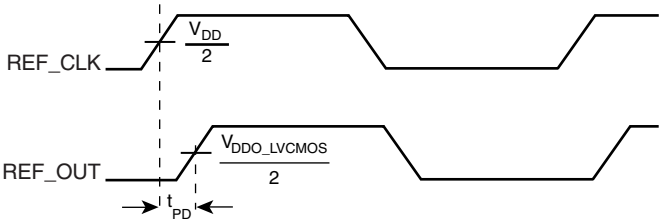
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



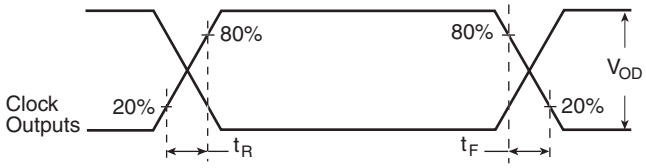
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



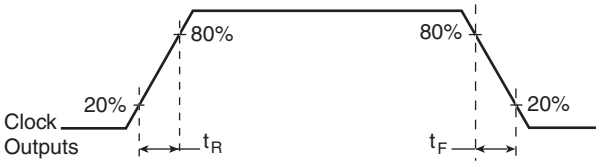
RMS PHASE JITTER



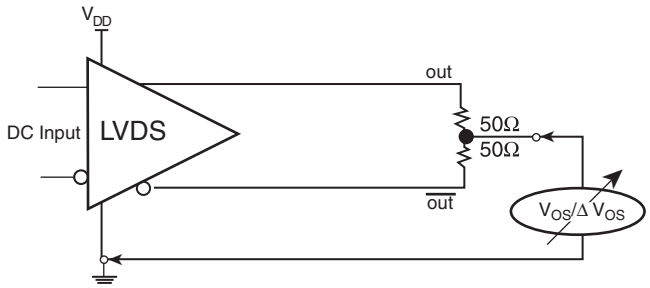
PROPAGATION DELAY



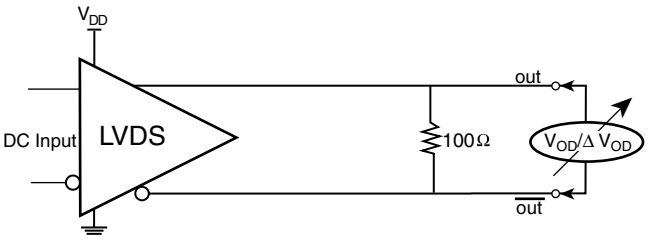
LVDS OUTPUT RISE/FALL TIME



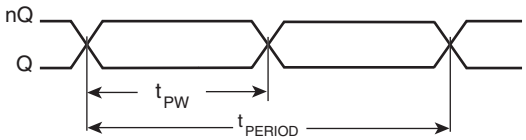
LVCMOS OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP

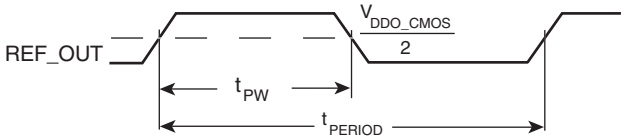


DIFFERENTIAL OUTPUT VOLTAGE SETUP



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844001-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a 0.01µF bypass capacitor should be connected to each V_{DDA}.

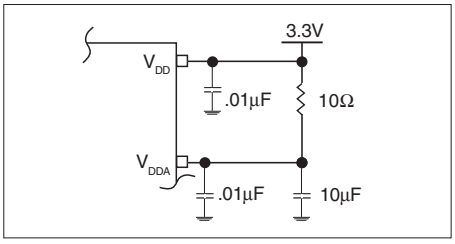


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS OUTPUT

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVCMOS OUTPUT

All unused LVCMOS output can be left floating. There should be no trace attached.

CRYSTAL INPUT INTERFACE

The ICS844001-21 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

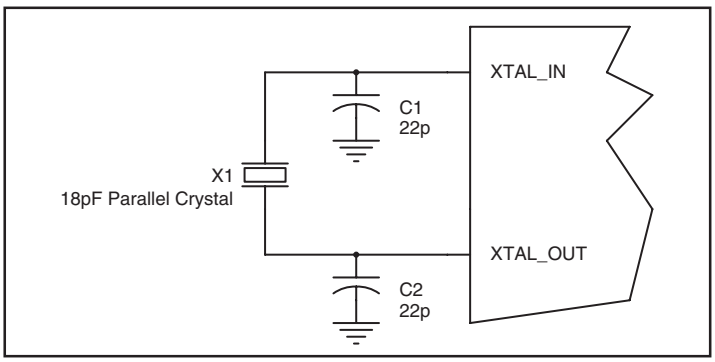


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

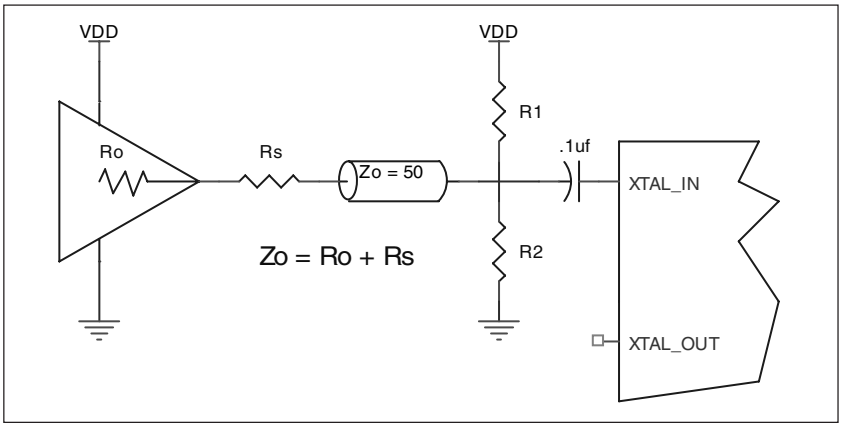


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

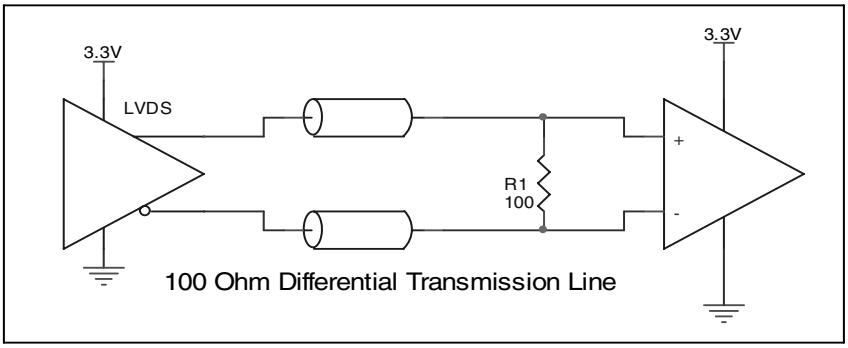


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

Schematic Example

Figure 5 shows an example of ICS844001-21 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. One example of LVDS and one example of LVCMOS terminations are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

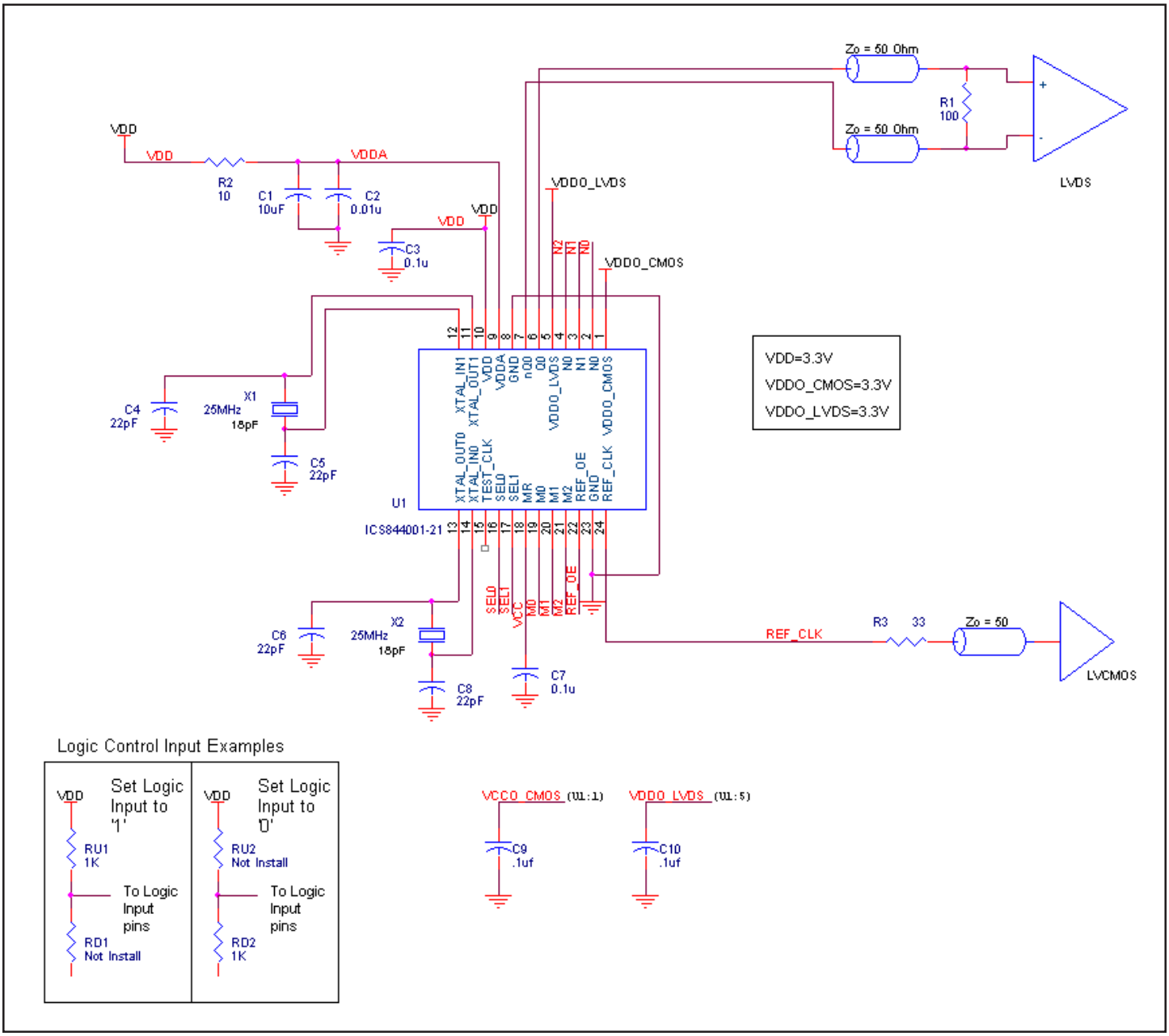


Figure 5. ICS844001-21 Schematic Layout

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844001-21. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844001-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = V_{DD_MAX} * (I_{DD} + I_{DDO_LVDS} + I_{DDA}) = 3.465V * (110mA + 40mA + 15mA) = **572mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO_CMOS}/2
  Output Current I_{OUT} = $V_{DDO\_CMOS\_MAX}$ / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 7Ω)] = **30.4mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 72Ω * (30.4mA)^2 = **6.47mW per output**
- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * frequency * (V_{DDO_CMOS})^2 = 8pF * 25MHz * (3.465V)^2 = **2.4 mW**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Total Power (R_{OUT}) + Total Power (125MHz) + Total Power (25MHz)
  = 572mW + 6.47mW + 2.4mW
  = 581mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 7 is:

70°C + 0.581W * 82.3°C/W = 118°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-TSSOP, FORCED CONVECTION

	θ_{JA} by Velocity (Meters per Second)		
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78°C/W	75.9°C/W

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78°C/W	75.9°C/W

TRANSISTOR COUNT

The transistor count for ICS844001-21 is: 4045

Package Outline - G Suffix for 24 Lead TSSOP

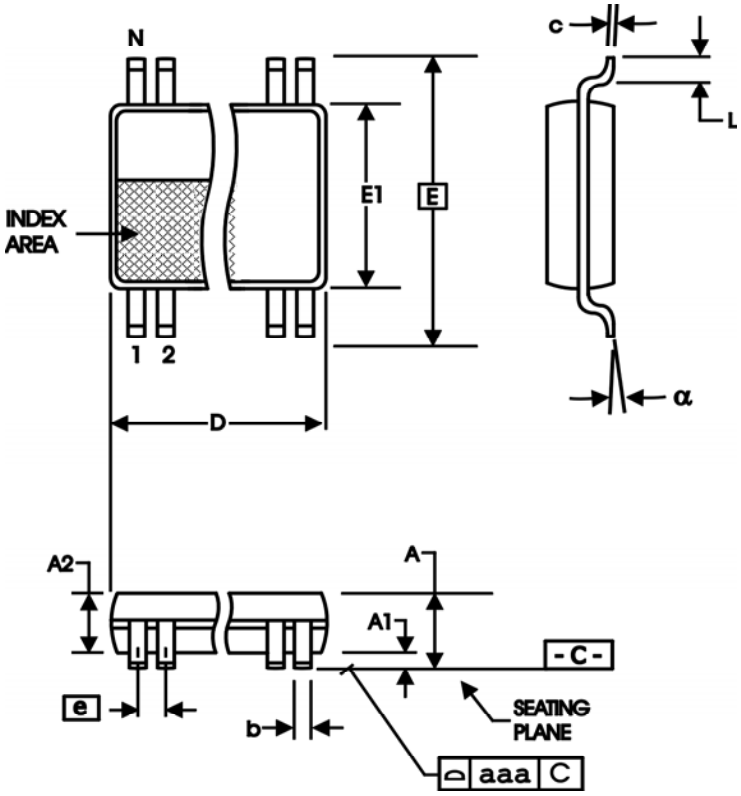


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844001AG-21	ICS844001AG21	24 Lead TSSOP	tube	0°C to 70°C
ICS844001AG-21T	ICS844001AG21	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS844001AG-21LF	TBD	24 Lead "Lead Free" TSSOP	tube	0°C to 70°C
ICS844001AG-21LFT	TBD	24 Lead "Lead Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Pats that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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