

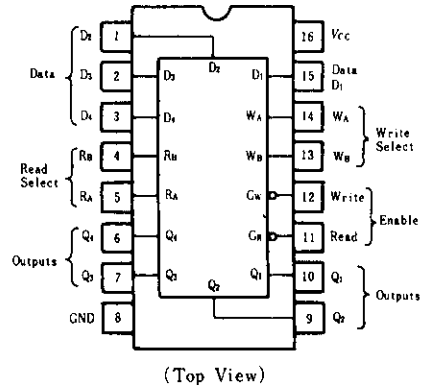
# HD74LS670 ● 4-by-4 Register File (with three-state outputs)

The HD74LS670, 16-bit register file incorporates the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the the four word locations to either write-in or retrieve data.

This permits simultaneous writing into one location and reading from another word location. Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input,  $G_W$ , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input,  $G_R$ , is high, the data outputs are inhibited and go into the high-impedance state. The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word.

When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

## ■ PIN ARRANGEMENT



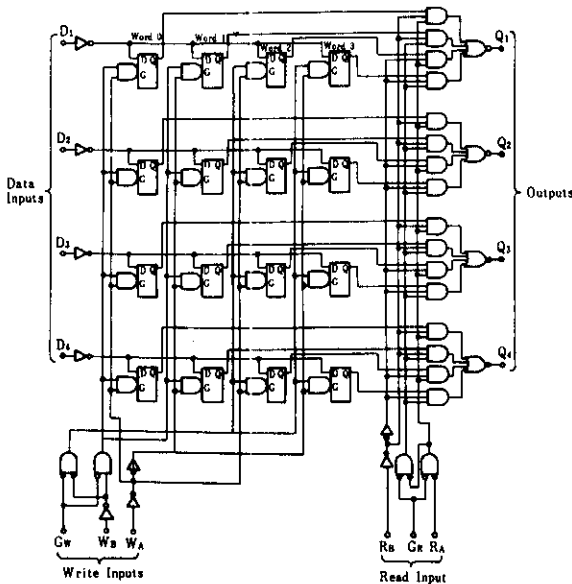
## ■ FUNCTION TABLE

Write Inputs			Word			
$W_B$	$W_A$	$G_W$	0	1	2	3
L	L	L	$Q = D$	$Q_0$	$Q_0$	$Q_0$
L	H	L	$Q_0$	$Q = D$	$Q_0$	$Q_0$
H	L	L	$Q_0$	$Q_0$	$Q = D$	$Q_0$
H	H	L	$Q_0$	$Q_0$	$Q_0$	$Q = D$
X	X	H	$Q_0$	$Q_0$	$Q_0$	$Q_0$

Read Inputs			Outputs			
$R_B$	$R_A$	$G_R$	$Q_1$	$Q_2$	$Q_3$	$Q_4$
L	L	L	$W_0 B_1$	$W_0 B_2$	$W_0 B_3$	$W_0 B_4$
L	H	L	$W_1 B_1$	$W_1 B_2$	$W_1 B_3$	$W_1 B_4$
H	L	L	$W_2 B_1$	$W_2 B_2$	$W_2 B_3$	$W_2 B_4$
H	H	L	$W_3 B_1$	$W_3 B_2$	$W_3 B_3$	$W_3 B_4$
X	X	H	Z	Z	Z	Z

Notes: H = high level, L = low level, X = irrelevant, Z = high impedance (off)  
 $(Q=D)$  = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.  
 $Q_0$  = The level of Q before the indicated input conditions were established.  
 $W_0 B_1$  = The first bit of word 0, etc.

## ■ BLOCK DIAGRAM



# HD74LS670

## RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V	
Output current	$I_{OH}$	—	—	-2.6	mA	
	$I_{OL}$	—	—	8	mA	
Pulse width	Read enable	$t_w$	25	—	—	ns
	Write enable		60	—	—	
Setup time	Data	$t_{su}$	10	—	—	ns
	Write enable		15	—	—	
Hold time	Data	$t_h$	15	—	—	ns
	Write enable		5	—	—	
Latch time	$t_{LATCH}$	60	—	—	ns	

## ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$		—	—	0.8	V	
Output voltage	$V_{OH}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-2.6\text{mA}$	2.4	—	—	V	
	$V_{OL}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$				V	
Off-state output current	$I_{OZH}$	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}$	$V_O=2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{OZL}$		$V_O=0.4\text{V}$	—	—	-20	
Input current	$I_{IH}$	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	Any D, R or W	—	—	20	$\mu\text{A}$
			$G_W$	—	—	40	
			$G_R$	—	—	60	
	$I_{IL}$	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	Any D, R or W	—	—	-0.4	mA
			$G_W$	—	—	-0.8	
			$G_R$	—	—	-1.2	
$I_I$	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	Any D, R or W	—	—	0.1	mA	
		$G_W$	—	—	0.2		
		$G_R$	—	—	0.3		
Short-circuit output current	$I_{OS}$	$V_{CC}=5.25\text{V}$	-30	—	-130	mA	
Supply current	$I_{CC}^{**}$	$V_{CC}=5.25\text{V}$	—	30	50	mA	
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V	

\*  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

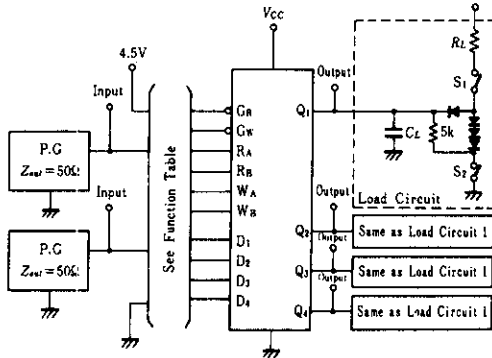
\*\* : Maximum  $I_{CC}$  is guaranteed for the following worst case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

## SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit	
Propagation delay time	$t_{PLH}$	Read	$Q_1 \sim Q_4$	$C_L=15\text{pF}, R_L=2\text{k}\Omega$	—	23	40	ns	
	$t_{PHL}$	select			—	25	45		
	$t_{PLH}$	Write enable	$Q_1 \sim Q_4$		—	26	45		
	$t_{PHL}$				—	28	50		
		$t_{PLH}$	Data		$Q_1 \sim Q_4$	—	25		45
		$t_{PHL}$				—	23		40
Output enable time	$t_{ZH}$	Read enable	$Q_1 \sim Q_4$		—	15	35		
	$t_{ZL}$				—	22	40		
Output disable time	$t_{HZ}$			$C_L=5\text{pF}, R_L=2\text{k}\Omega$	—	30	50		
	$t_{LZ}$				—	16	35		

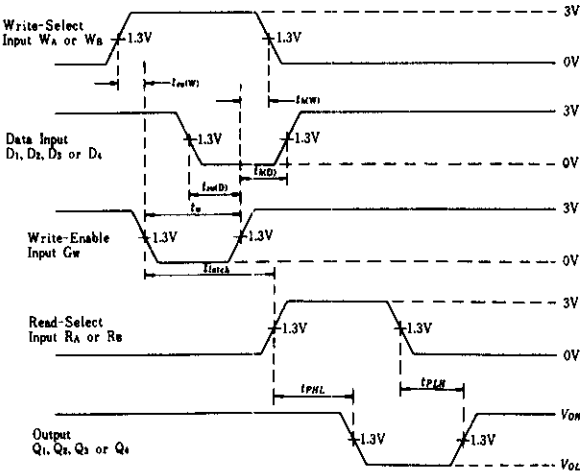
## TESTING METHOD

### Test Circuit



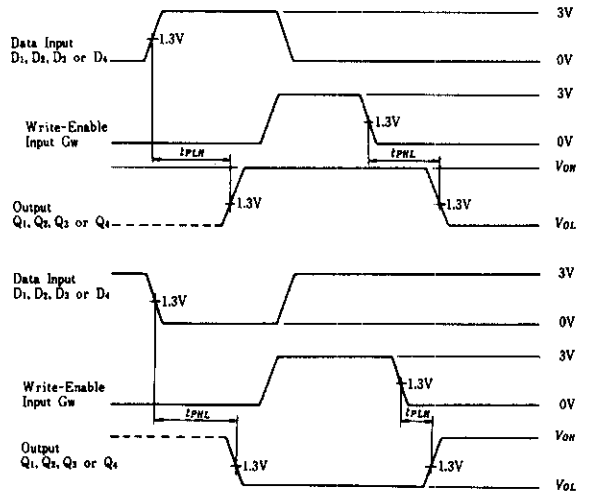
- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2. All diodes are 1S2074  $\text{\textcircled{R}}$ .

### Waveform-1



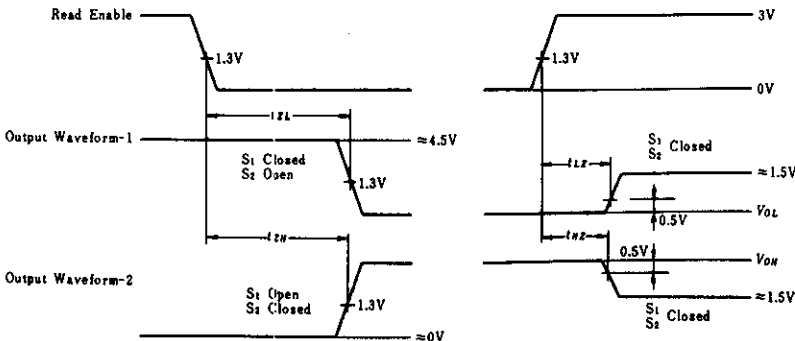
- Notes:
1. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
  2. When measuring delay times from a read-select inputs, the read-enable input is low.
  3. Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%

### Waveform-2



- Note:
- Each select address is tested. Prior to the start of each of the above test both write and read address inputs are stabilized with  $W_A = R_A$  and  $W_B = R_B$ . During the test  $G_R$  is low.

### Waveform-3



Waveform A is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform B is for an output with internal conditions such that the output is high except when disabled by the read-enable input.



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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