FAIRCHILD SEMICONDUCTOR®

January 2007

FAN7311
LCD Backlight Inverter Drive IC

Features

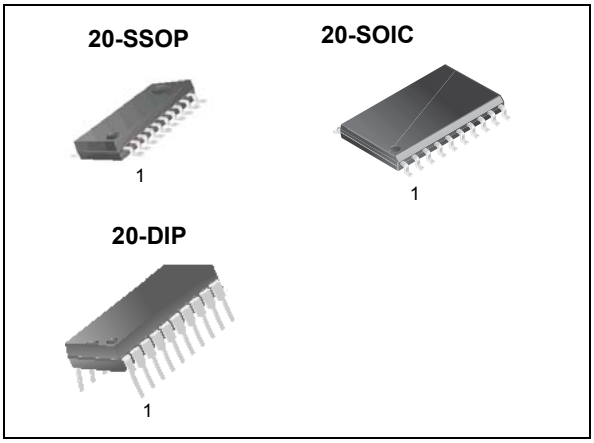
- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 5V to 25.5V
- Backlight Lamp Ballast and Soft Dimming
- Reduced Number of Required External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS Full-Bridge Topology
- Soft-Start Capability
- PWM Control at Fixed Frequency
- Analog and Burst Dimming Function
- Programmable Striking Frequency
- Open-Lamp Protection
- Open-Lamp Regulation
- 20-Pin SSOP/SOIC/DIP

Applications

- LCD TV
- LCD Monitor

Description

The FAN7311 provides all the control functions for a series parallel resonant converter as well as a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz, depending on the cold cathode fluorescent lamp (CCFL) and the transformer's characteristics. The FAN7311 uses a new patent-pending phase-shift control.



Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7311G	20-SSOP	Yes	-25°C to 85°C	Rail
FAN7311GX	20-SSOP	Yes		Tape & Reel
FAN7311M	20-SOIC	Yes		Rail
FAN7311MX	20-SOIC	Yes		Tape & Reel
FAN7311N	20-DIP	Yes		Rail

Protected by U.S. Patent: 5,652,479; 7,158,390.

Internal Block Diagram

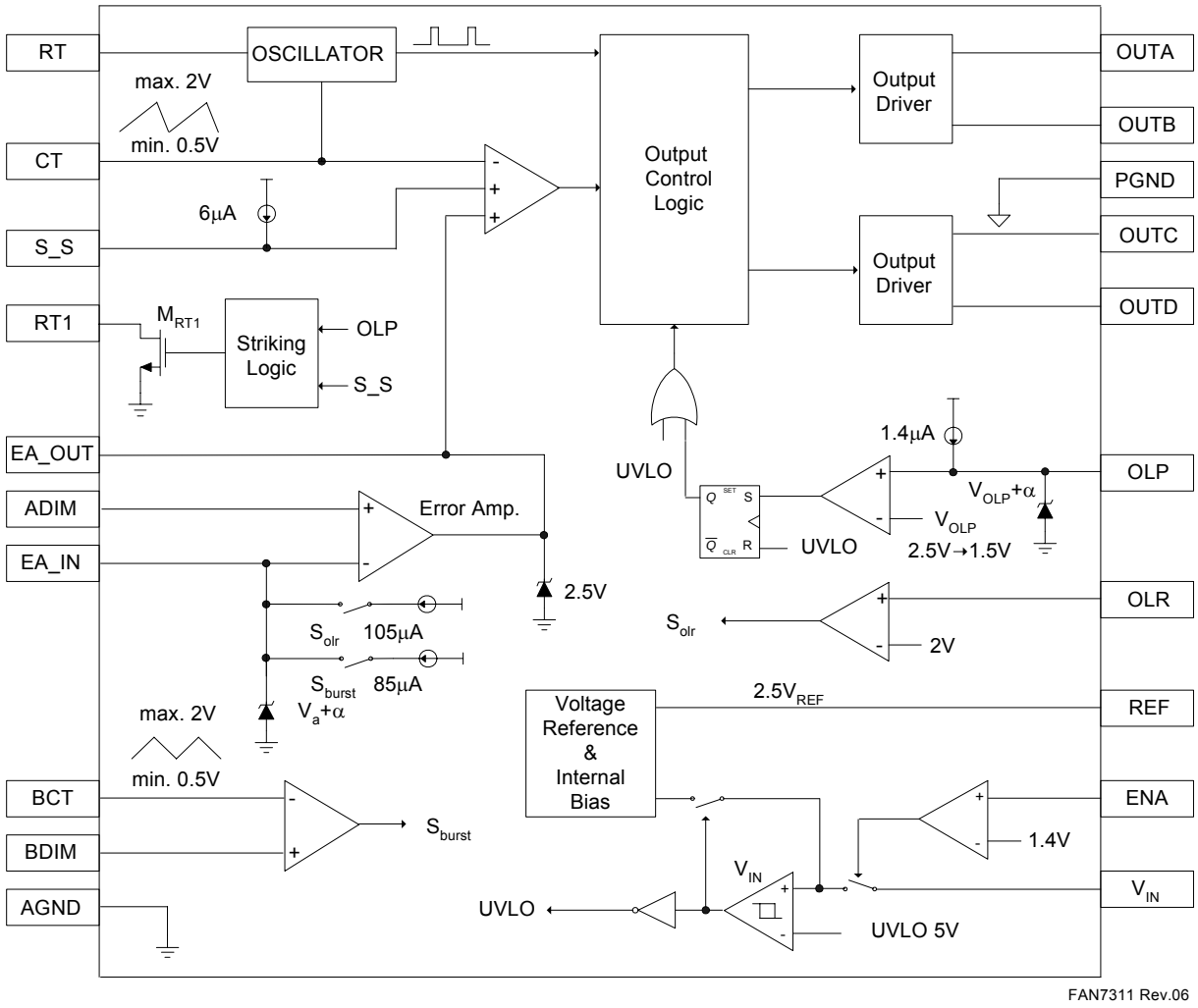


Figure 1. Functional Block Diagram of FAN7311

Pin Assignments

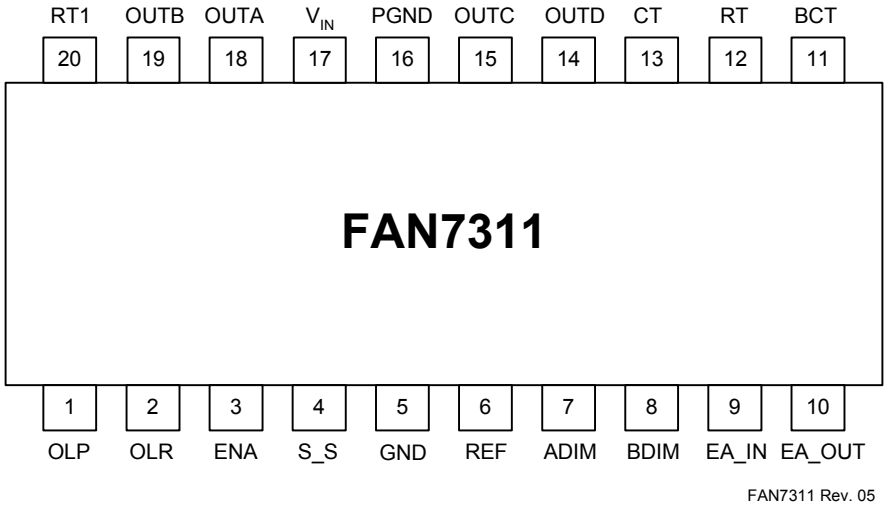


Figure 2. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description	Pin #	Name	Description
1	OLP	Open-Lamp Protection	11	BCT	Burst Dimming Timing Capacitor
2	OLR	Open-Lamp Regulation	12	RT	Timing Resistor
3	ENA	Enable Input	13	CT	Timing Capacitor
4	S_S	Soft-Start	14	OUTD	NMOSFET Drive Output D
5	GND	Analog Ground	15	OUTC	PMOSFET Drive Output C
6	REF	2.5V Reference Voltage	16	PGND	Power Ground
7	ADIM	Analog Dimming Input	17	V_{IN}	Supply Voltage
8	BDIM	Burst Dimming Input	18	OUTA	PMOSFET Drive Output A
9	EA_IN	Error Amplifier Input	19	OUTB	NMOSFET Drive Output B
10	EA_OUT	Error Amplifier Output	20	RT1	Striking Frequency Resistor

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

For typical values, T_A=25°C and V_{IN}=12V. For min. and max. values, T_A is the operating ambient temperature range with -25°C ≤ T_A ≤ 85°C and 5V ≤ V_{IN} ≤ 25.5V, unless otherwise specified.

Symbol	Characteristics	Value	Unit
V_{IN}	Supply Voltage	5 to 25.5	V
T_A	Operating Temperature Range	-25 to 85	°C
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
θ_{JA}	Thermal Resistance Junction-to-Ambient (still air)[1]		°C/W
	20-SSOP	112	
	20-SOIC	70	
	20-DIP	TBD[2]	
P_D	Power Dissipation		W
	20-SSOP	1.1	
	20-SOIC	1.8	
	20-DIP	TBD	

Notes:

1. Thermal resistance test board size: 76.2 * 114.3 * 1.6mm (1S0P). JEDEC standard: JESD51-2, JESD51-3.
2. To be determined.

Electrical Characteristics

For typical values, T_A=25°C and V_{IN}=12V. For min. and max. values, T_A is the operating ambient temperature range with -25°C ≤ T_A ≤ 85°C and 5V ≤ V_{IN} ≤ 25.5V, unless otherwise specified. Specifications from -25°C to 85°C are guaranteed by design based on final characterization results.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION (Recommend X7R Capacitor)						
ΔV_{ref}	Line Regulation	5 ≤ V_{IN} ≤ 25.5V		2	25	mV
V25	2.5V Regulation Voltage		2.45	2.50	2.55	V
OSCILLATOR SECTION (MAIN)						
f_{osc}	Oscillation Frequency	T_A = 25°C, CT = 270pF, RT = 18kΩ	110.4	115.0	119.6	kHz
		CT = 270pF, RT = 18kΩ	108	115	122	
V_{cth}	CT High Voltage			2.0		V
V_{ctl}	CT Low Voltage			0.5		V
OSCILLATOR SECTION (BURST)						
f_{oscb}	Oscillation Frequency	T_A = 25°C, CTB = 10nF, RT=18kΩ	209.25	225.00	240.75	Hz
		CTB = 10nF, RT=18kΩ	206.25	225.00	241.75	
V_{bcth}	BCT High Voltage			2		V
V_{bctl}	BCT Low Voltage			0.5		V
ERROR AMP SECTION						
A_v	Open Loop Gain(3)			80		dB
G_{BW}	Unit Gain Bandwidth(3)			1.5		MHz
V_{eh}	Feedback Output High Voltage	EA_IN = 0V	2.00	2.27	2.54	V
I_{sin}	Output Sink Current	EA_OUT = 1.5V			-1	mA
I_{sur}	Output Source Current	EA_OUT = 1.5V	1			mA
I_{olr}	EA_IN Driving Current on OLR		75	105	135	µA
I_{burst}	EA_IN Driving Current on Burst Dimming		61	85	109	µA
V_{fbh}	Feedback High Voltage on Burst Dimming	R(EA_IN) = 60kΩ	V_a+0.1	V_a+0.4	V_a+0.7	V
SOFT-START SECTION						
I_{SS}	Soft-Start Current	S_S=1V	4	6	8	µA
V_{ssh}	Soft-Start Clamping Voltage(3)			4		V
PROTECTION SECTION						
V_{olp0}	Open-Lamp Protection Voltage 0	Start at open lamp	2.2	2.5	2.8	V
V_{olp1}	Open-Lamp Protection Voltage 1	Normal -> open lamp	1.3	1.5	1.7	V
V_{olr}	Open-Lamp Regulation Voltage		1.75	2.00	2.25	V
I_{olp}	Open-Lamp Protection Charging Current		0.7	1.4	2.1	µA
UNDER-VOLTAGE LOCKOUT SECTION						
V_{th}	Start Threshold Voltage				5	V
I_{st}	Startup Current	V_{IN} = V_{th}-0.2		130	180	µA
I_{op}	Operating Supply Current	V_{IN} = 12V		1.5	4.0	mA
I_{sb}	Stand-by Current	V_{IN} = 12V		200	370	µA

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (Continued)

For typical values, T_A=25°C and V_{IN}=12V. For min. and max. values, T_A is the operating ambient temperature range with -25°C ≤ T_A ≤ 85°C and 5V ≤ V_{IN} ≤ 25.5V, unless otherwise specified. Specifications from -25°C to 85°C are guaranteed by design based on final characterization results.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
ON/OFF SECTION						
V_{on}	On State Input Voltage		2		5	V
V_{off}	Off Stage Input Voltage				0.7	V
OUTPUT SECTION						
V_{pdhv}	PMOS Gate High Voltage	V_{IN} = 12V		V_{IN}		V
V_{phlv}	PMOS Gate Low Voltage	V_{IN} = 12V	V_{IN}-10.5	V_{IN}-8.5	V_{IN}-6.5	V
V_{ndhv}	NMOS Gate Drive Voltage	V_{IN} = 12V	6.5	8.5	10.5	V
V_{ndhv}	NMOS Gate Drive Voltage	V_{IN} = 12V		0		V
V_{puv}	PMOS Gate Voltage With UVLO Activated	V_{IN} = V_{th}-0.2	V_{IN}-0.3			V
V_{nuv}	NMOS Gate Voltage With UVLO Activated	V_{IN} = V_{th}-0.2			0.3	V
t_r	Rising Time(4)	V_{IN} = 12V, C_L=2nF		200	500	ns
t_f	Falling Time(4)	V_{IN} = 12V, C_L=2nF		200	500	ns
MAX./MIN. OVERLAP						
	Min. Overlap Between Diagonal Switches(4)	f_{osc} = 100kHz		0		%
	Max. Overlap Between Diagonal Switches(4)	f_{osc} = 100kHz		100		%
DELAY TIME						
	PDR_A/NDR_B(4)	RT = 18kΩ		450		ns
	PDR_C/NDR_D(4)	RT = 18kΩ		450		ns

Note:

4. These parameters, although guaranteed, are not 100% tested in production.

Function Description

UVLO: The under-voltage lockout circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the V_{IN} value. The UVLO circuit turns on the control circuit when V_{IN} exceeds 5V. When V_{IN} is lower than 5V, the IC's standby current is less than 200μA.

ENA: Applying voltage higher than 2V to the ENA pin enables operation of the IC. Applying voltage lower than 0.7V to the ENA pin disables operation of the inverter.

Soft-Start: The soft-start function requires that the S_S pin is connected through a capacitor to GND. A soft-start circuit ensures a gradual increase in the input and output power. The capacitor connected to the S_S pin determines the rate at which the duty ratio rises. It is charged by a 6μA current source.

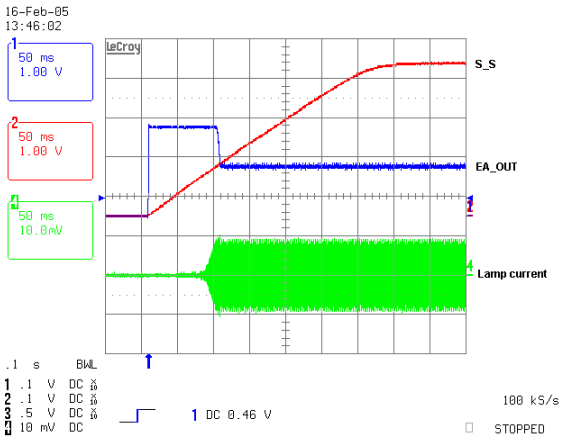


Figure 3. Soft-Start During Initial Operation

Main Oscillator: The timing capacitors (CTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed by adjusting the RT and CT values. The main frequency can be calculated as shown below.

$$f_{op} = \frac{19}{32 \cdot RT \cdot CT} \qquad (1)$$

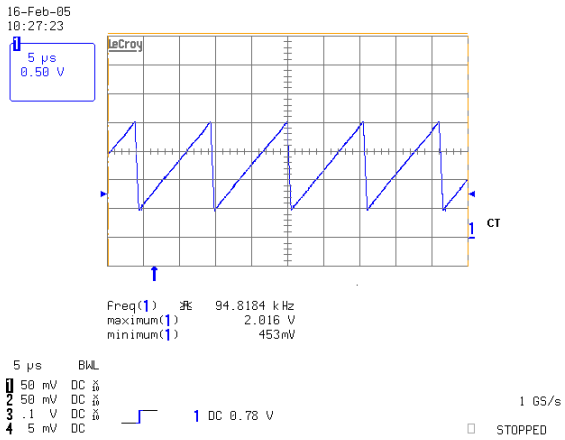


Figure 4. Main Oscillator Waveform

Burst Oscillator & Burst Dimming: The timing capacitors (BCTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed by adjusting the RT and BCT values. The burst dimming frequency can be calculated as shown in Equation 2.

$$f_{burst} = \frac{3.75}{96 \cdot RT \cdot CT} \qquad (2)$$

To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

By comparing the input of BDIM pin with the 0.5~2V triangular wave of the burst oscillator, the PWM pulses for burst dimming. The PWM pulse controls EA_OUT's voltage by summing 85μA into the EA_IN pin.

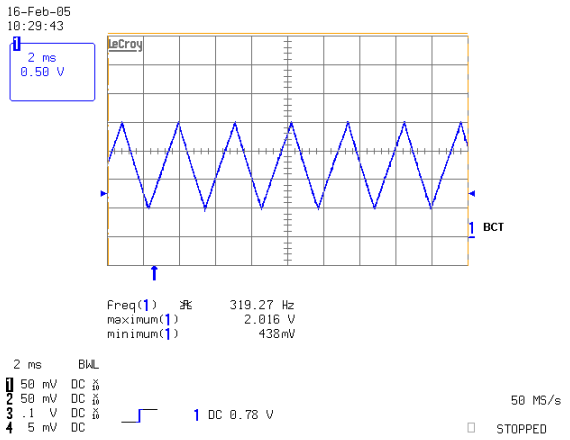


Figure 5. Burst Oscillator Waveform

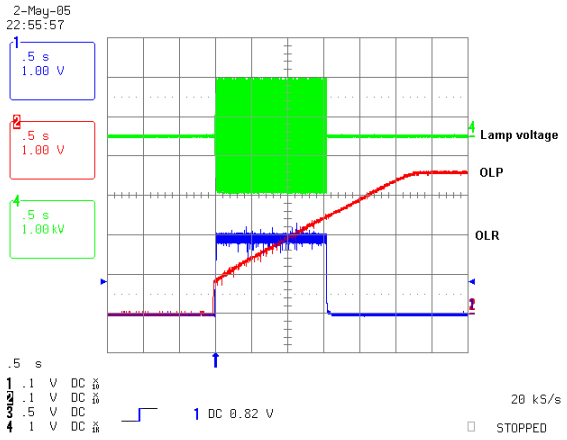


Figure 7. OLR Voltage During Striking Mode

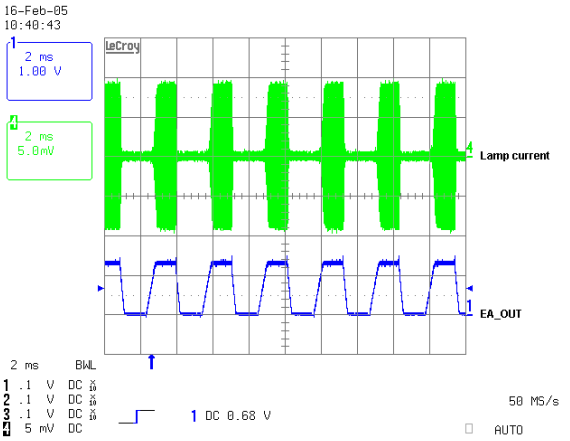


Figure 6. Burst Dimming

Open Lamp Regulation and Open-Lamp Protection: It is necessary to suspend power stage operation if an open lamp occurs, because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters regulation mode and controls the EA_OUT voltage. This limits the lamp voltage by summing 105µA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4µA internal current source. Once it reaches 2.5V, the IC enters shut down where all output is high.

Output Drives: The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair drives the other half-bridge.

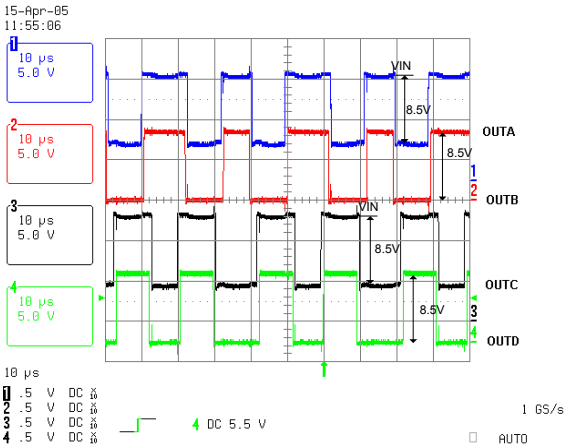


Figure 8. Phase-Shift Control Waveforms

Timing Diagram

The FAN7311 uses the improved phase-shift control full-bridge to drive CCFL. As a result, the temperature difference between the left and the right leg is almost zero. The detail timing is shown below.

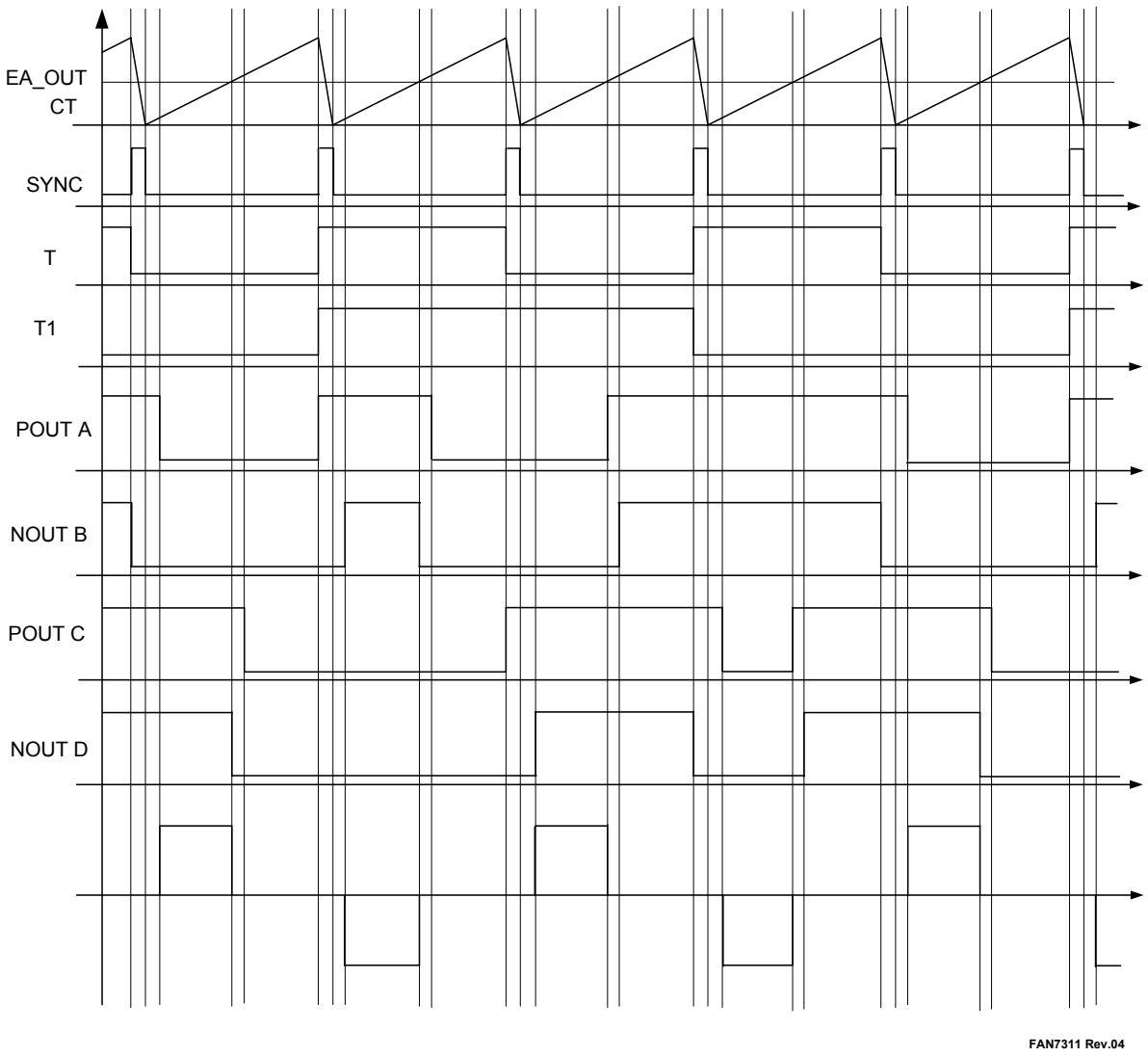


Figure 9. Phase-Shift Control Waveforms

Typical Application Circuits

Application	Lamps	Input Voltage
19-inch LCD Monitor	4	13V

1. Schematic

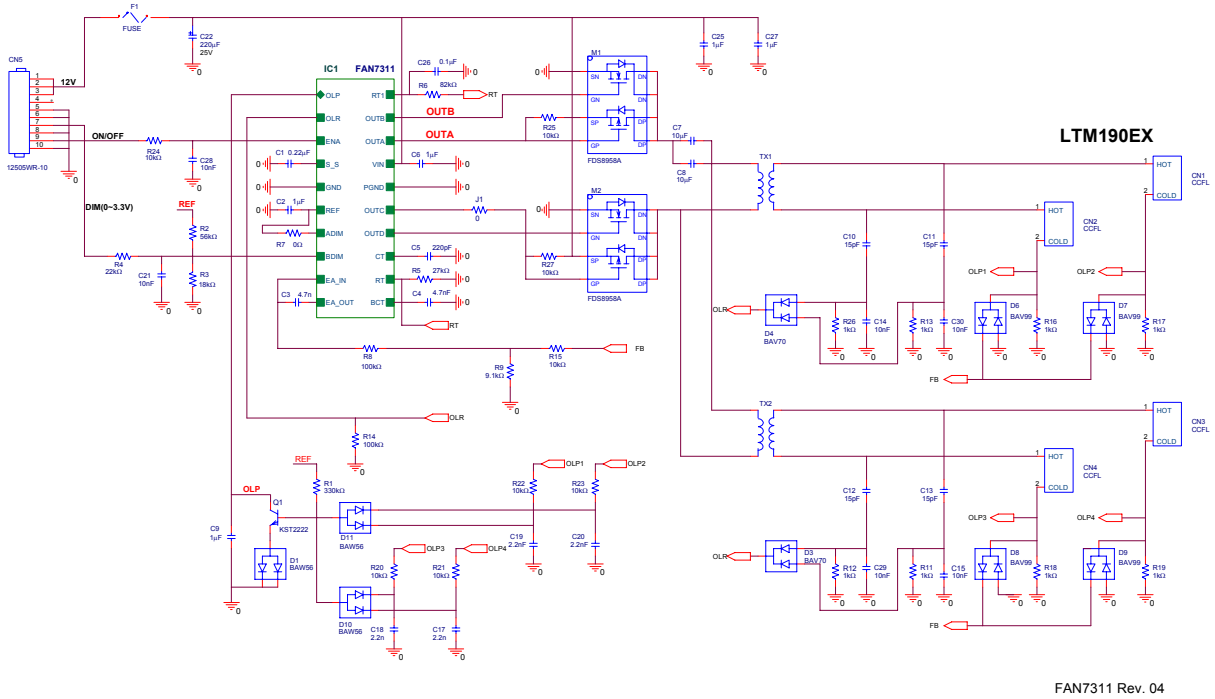


Figure 10. Typical Application Circuit

2. Transformer Schematic Diagram

- Supported by Namyang electronics (http://www.namyangelec.co.kr)

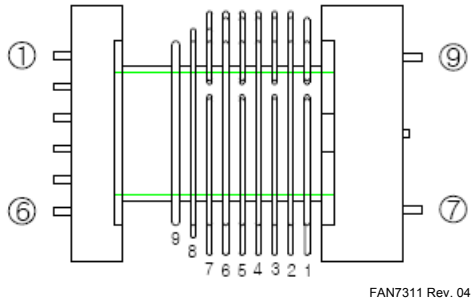


Figure 11. Transformer Schematic

3. Core & Bobbin

- Core: EFD2124
- Material: PL7
- Bobbin: EFE2124

4. Winding Specification

Pin No.	Wire	Turns	Inductance	Leakage Inductance	Remarks
5 --> 2	1 UEW 0.45 ϕ	19	115 µH	21.5µH	1KHz, 1V
7 --> 9	1 UEW 0.04 ϕ	2300	1.5 H	280mH	1KHz, 1V

5. BOM of the Application Circuit

Part Ref.	Value	Description / Vendor	Part Ref.	Value	Description / Vendor
Fuse			C5	220pF	50V 1608 J
F1	24V 3A	Fuse	C6	1µF	50V 2012 K
Resistor (SMD)			C7	10µF	16V 3216
R1	330kΩ	1608 J	C8	10µF	16V 3216
R2	56kΩ	1608 F	C9	1µF	16V 1608 K
R3	18kΩ	1608 F	C10	15pF	3KV 3216
R4	22kΩ	1608 F	C11	15pF	3KV 3216
R5	27kΩ	1608 F	C12	15pF	3KV 3216
R6	82kΩ	1608 F	C13	15pF	3KV 3216
R8	100kΩ	1608 F	C14	10nF	50V 1608 K
R9	9.1kΩ	1608 F	C15	10nF	50V 1608 K
R11	1kΩ	1608 F	C17	2.2nF	50V 1608 Z
R12	1kΩ	1608 F	C18	2.2nF	50V 1608 Z
R13	1kΩ	1608 F	C19	2.2nF	50V 1608 Z
R14	100kΩ	1608 F	C20	2.2nF	50V 1608 Z
R15	10kΩ	1608 F	C21	10nF	50V 1608 Z
R16	1kΩ	1608 F	C25	1µF	50V 2012 K
R17	1kΩ	1608 F	C26	0.1µF	16V 1608 K
R18	1kΩ	1608 F	C27	1µF	50V 2012 K
R19	1kΩ	1608 F	C28	10nF	50V 1608 Z
R20	10kΩ	1608 J	C29	10nF	50V 1608 K
R21	10kΩ	1608 J	C30	10nF	50V 1608 K
R22	10kΩ	1608 J	**Diode / TR (SMD)**		
R23	10kΩ	1608 J	D1	BAW56	Fairchild Semiconductor
R24	10kΩ	1608 J	D3	BAV70	Fairchild Semiconductor
R25	10kΩ	1608 J	D4	BAV70	Fairchild Semiconductor
R26	1kΩ	1608 F	D6	BAV99	Fairchild Semiconductor
R27	10kΩ	1608 J	D7	BAV99	Fairchild Semiconductor
Capacitor (SMD)			D8	BAV99	Fairchild Semiconductor
C1	0.22µF	16V 1608 K	D9	BAV99	Fairchild Semiconductor
C2	1µF	50V 2012 K	D10	BAW56	Fairchild Semiconductor
C3	4.7nF	50V 1608 K	D11	BAW56	Fairchild Semiconductor
C4	4.7nF	50V 1608 K	Q1	KST2222	Fairchild Semiconductor

5. BOM of the Application Circuit (Continued)

Part Ref.	Value	Description / Vendor	Part Ref.	Value	Description / Vendor
Electrolytic capacitor			**Wafer (SMD)**		
C22	220µF	25V	CN1	35001WR-02A	
MOSFET (SMD)			CN2	35001WR-02A	
M1	FDS8958A	Fairchild semiconductor	CN3	35001WR-02A	
M2	FDS8958A	Fairchild semiconductor	CN4	35001WR-02A	
Transformer (SMD)			CN5	12505WR-10	
TX1	EFD2124	**Supported by Namyang electronics (http://www.namyangelec.co.kr)**			
TX2	EFD2124				

Mechanical Dimensions

20-SSOP

Dimensions are in millimeters unless otherwise specified.

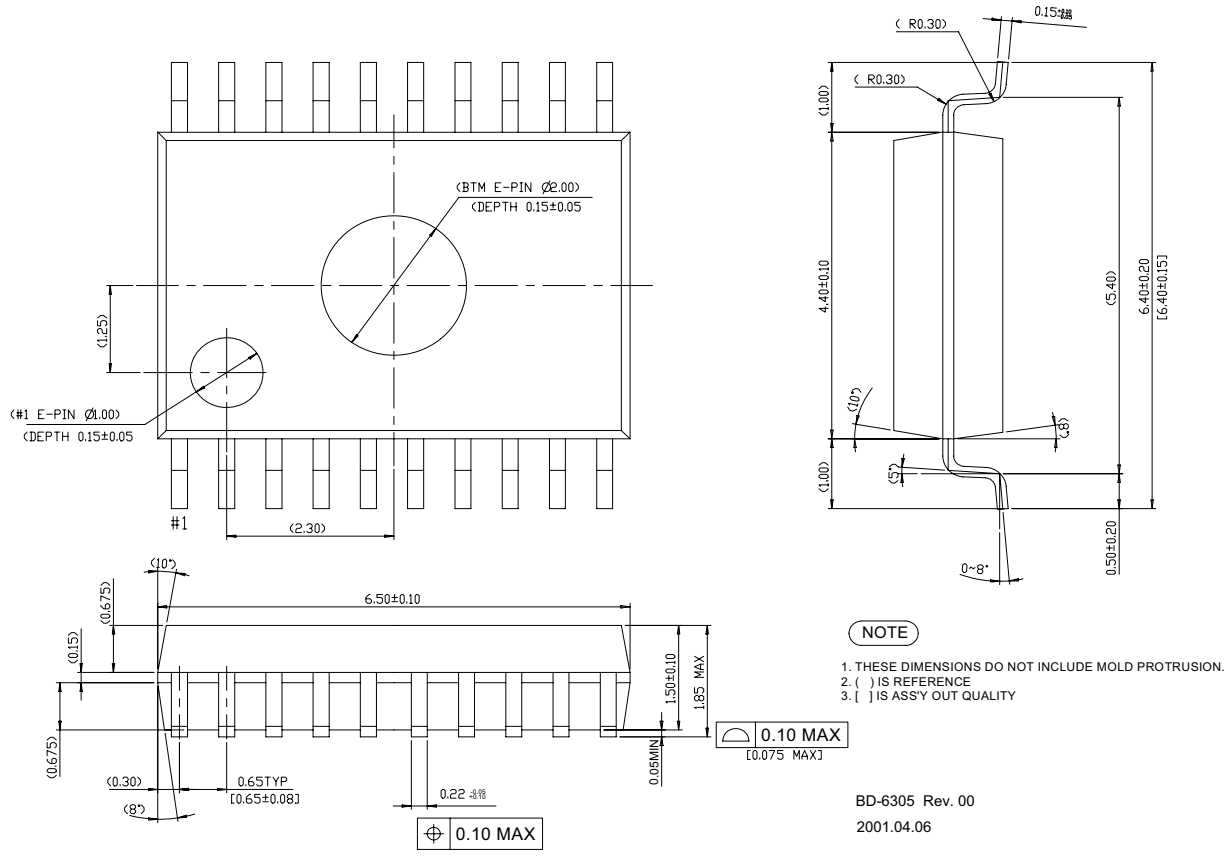
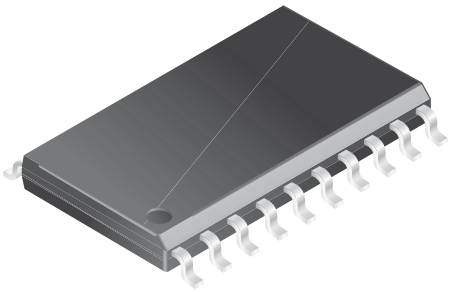


Figure 12. 20-Lead Shrink Small Outline Package (SSOP)

Mechanical Dimensions (Continued)

20-SOIC

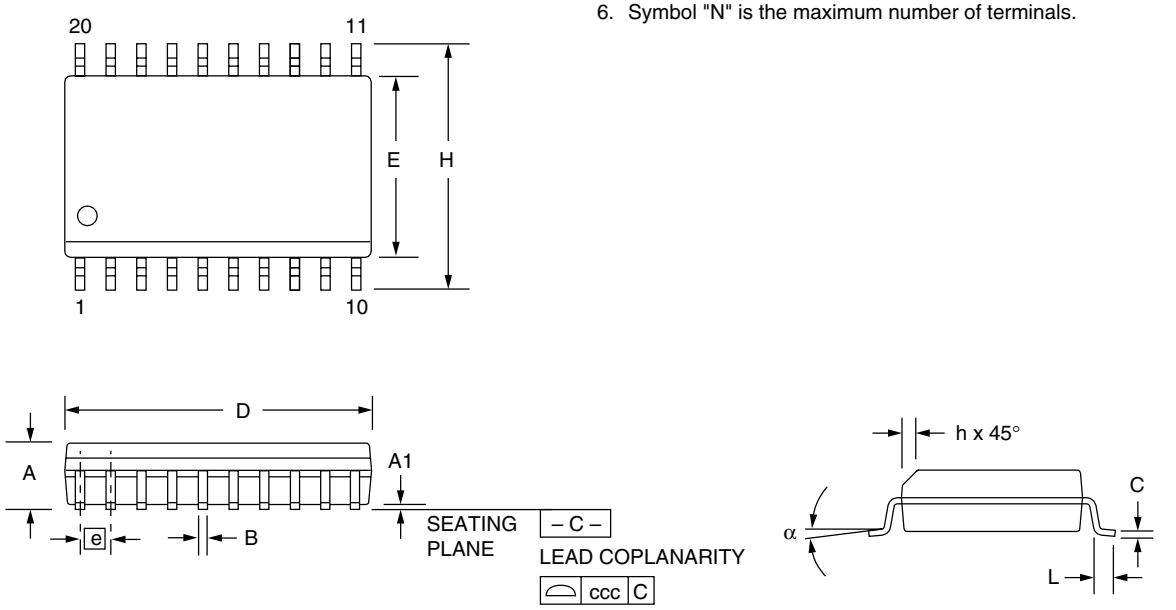
Dimensions are in millimeters unless otherwise specified.



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



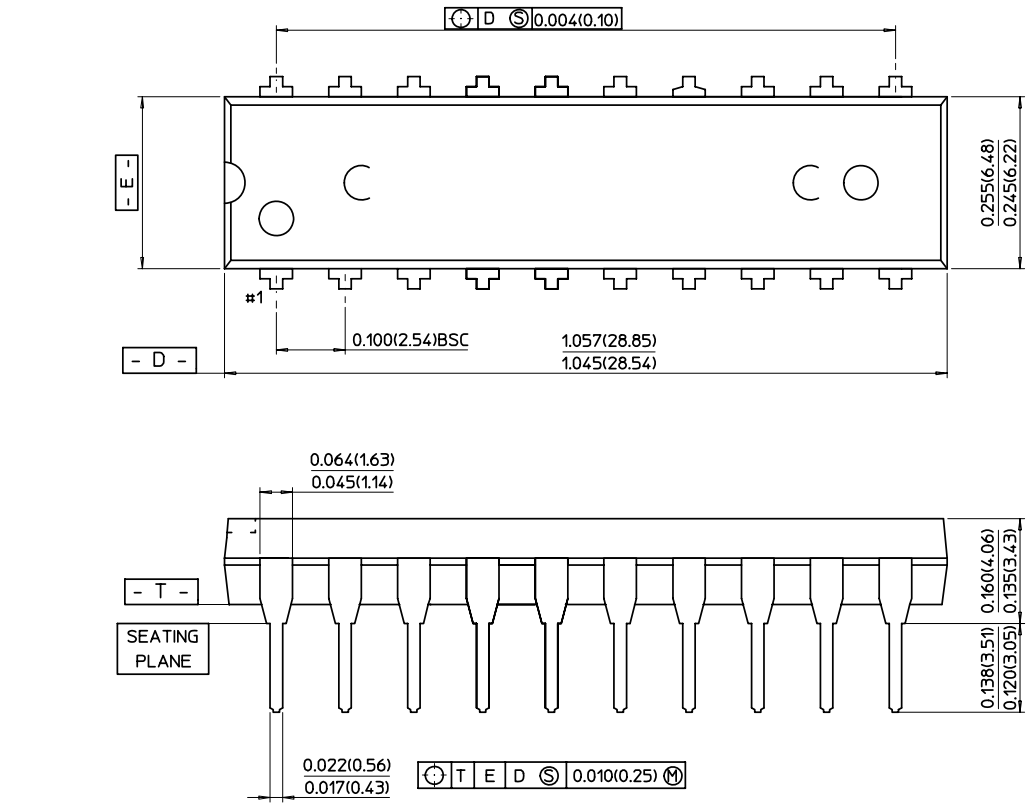
January 2001, Rev. A
soic20_dim.pdf

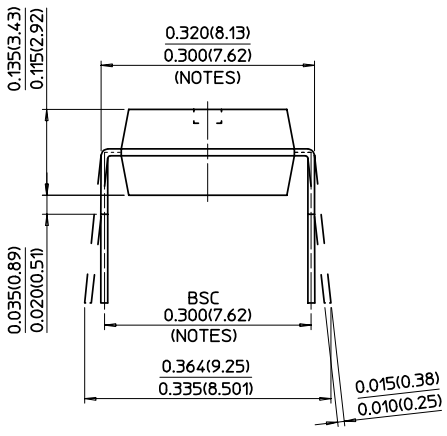
Figure 13. 20-Lead Small Outline Integrated Circuit (SOIC)

Mechanical Dimensions (Continued)

20-DIP

Dimensions are in millimeters unless otherwise specified.





NOTES

1. Controlling dimension : Inches. Metrics are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AE for standard Dual In Line(DIP) package 0.300 inch row sapcing (plastic) 20 leads (Issue B,7/85).
3. Dimension and tolerancing per ANSI Y14,5M-1982.
4. "T","D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from the top.

BD5256 REV. 00
2000. 08. 10

Figure 14. 20-Lead Dual In-Line Package (DIP)

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Bottomless™	GTO™	OPTOLOGIC®	SPM™	Wire™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	
CoolFET™	I^2C™	PACMAN™	SuperFET™	
CROSSVOLT™	*i-Lo*™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC®	
Programmable Active Droop™				

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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