T-31-25

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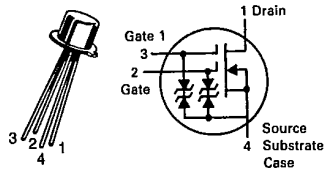
CASE 20-03, STYLE 9
TO-72 (TO-206AF)



DUAL-GATE MOSFET FM AMPLIFIER

N-CHANNEL — DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Gate-Source Voltage	V_{GS}	±7.0	Vdc
Drain Current	I_D	30	mAdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300	mW
Operating and Storage Channel Temperature Range	$T_{channel}$, T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1} = −4.0 Vdc, V_{G2} = +4.0 Vdc)	$V_{(BR)DSX}$	25	—	—	Vdc
Gate 1-Source Breakdown Voltage (I_{G1} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G1SO}$	±7.0	—	±20	Vdc
Gate 2-Source Breakdown Voltage (I_{G2} = ±10 μAdc, V_{G2S} = 0)	$V_{(BR)G2SO}$	±7.0	—	±20	Vdc
Gate 1 Leakage Current (V_{G1S} = ±6.0 Vdc, V_{G2S} = 0, V_{DS} = 0)	I_{G1SS}	—	—	20	nAdc
Gate 2 Leakage Current (V_{G2S} = ±6.0 Vdc, V_{G1S} = 0, V_{DS} = 0)	I_{G2SS}	—	—	20	nAdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 200 μAdc)	$V_{G1S(off)}$	—	—	−4.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 200 μAdc)	$V_{G2S(off)}$	—	—	−4.0	Vdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current (V_{DS} = 15 Vdc, V_{G2S} = 0, V_{G2S} = 4.0 Vdc)	I_{DSS}	3.0	10	30	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (Gate 1 connected to Drain) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	10	—	20	mmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, = 1.0 MHz)	C_{rss}	—	0.023	0.05	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	—	2.5	4.0	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (Figure 8) (See Test Circuit in Figure 11)	NF	—	2.5	3.5	dB
Common Source Power Gain (Figure 7) (See Test Circuit in Figure 11)	G_{ps}	20	23	—	dB
Level of Unwanted Signal for 1.0% Cross Modulation (Figure 10) (See Test Circuit in Figure 11)	—	—	45	—	mV

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ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Common-Source Conversion Power Gain (Gate 1 or Gate 2 Injection, Figure 12) (See Test Circuit in Figure 13) (Signal Frequency = 100 MHz, Local Oscillator Frequency = 110.7 MHz)	G_c	15	18.5	—	dB
1/2 I.F. Rejection (See Test Circuit in Figure 13)	1/2 I_{FREJ}	—	50	—	dB

COMMON-SOURCE ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 6.0 mAdc)

FIGURE 1 – INPUT ADMITTANCE

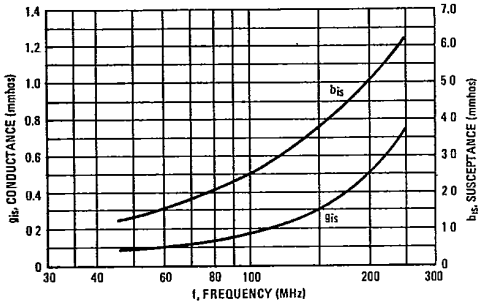


FIGURE 2 – REVERSE TRANSFER ADMITTANCE

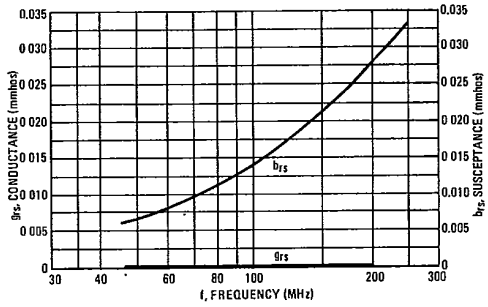


FIGURE 3 – FORWARD TRANSFER ADMITTANCE

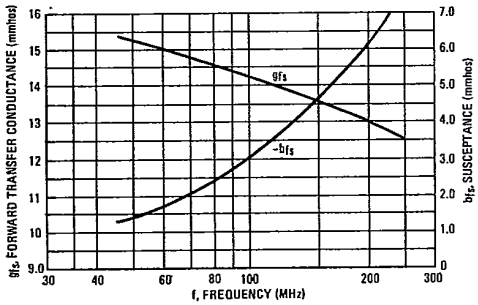
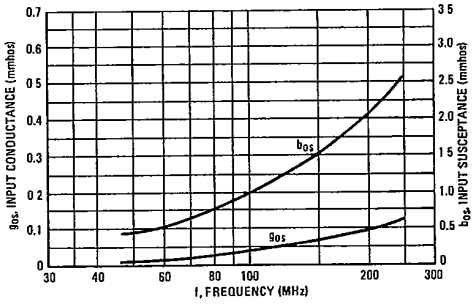


FIGURE 4 – OUTPUT ADMITTANCE



FORWARD TRANSFER ADMITTANCE

(V_{DS} = 15 Vdc, f = 1.0 kHz)

FIGURE 5 – GATE 1

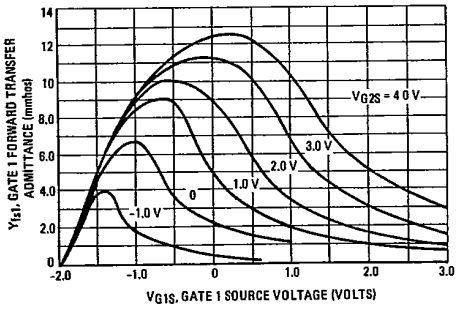


FIGURE 6 – GATE 2

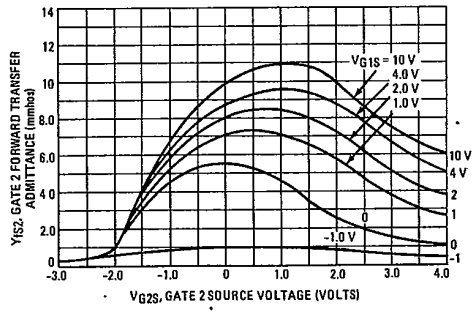


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FIGURE 7 – POWER GAIN

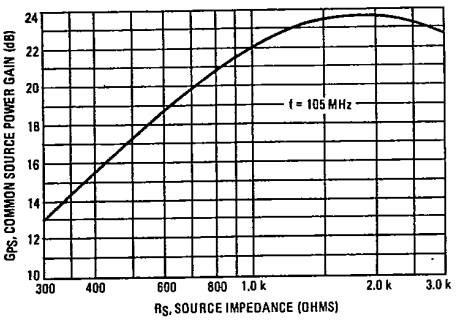


FIGURE 8 – NOISE FIGURE

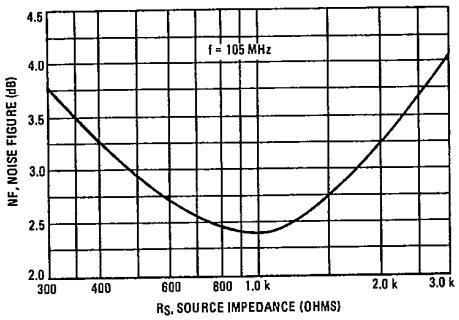


FIGURE 9 – GAIN REDUCTION

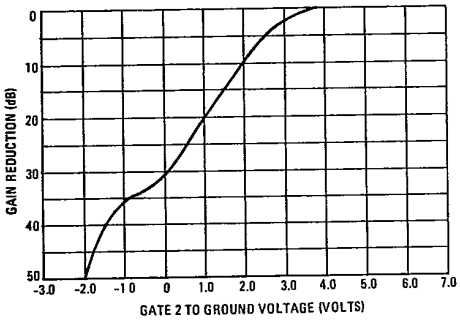


FIGURE 10 – CROSS MODULATION

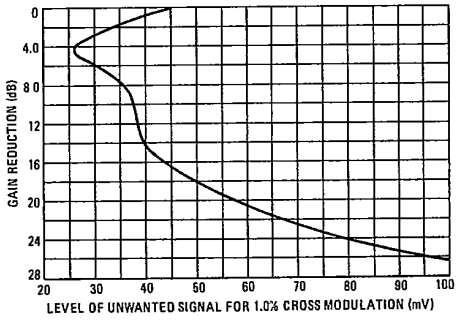
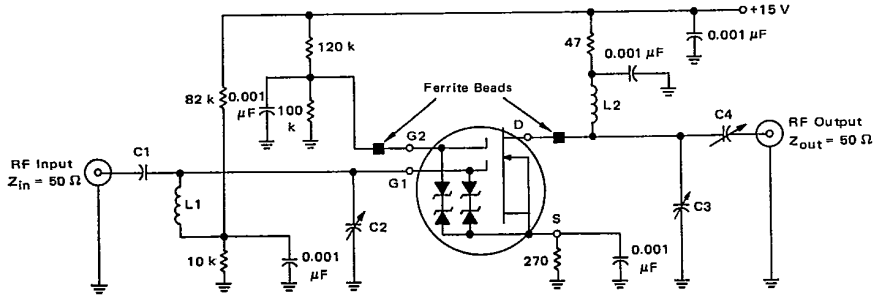


FIGURE 11 – 105 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



The following component values are for a stern stability factor = 2.0.
L1,L2 126 nH PAUL SMITH CO. SK-138-1
4-½ Turns (yellow)
C1 Nominal 7.0 pF Adjusted for source impedance of approximately 1000 Ω, JOHANSON JMC2951
C2 Nominal 4.0 pF ARCO 402
C3 Nominal 13.73 pF ARCO 403
C4 Nominal 4.36 pF JOHANSON JMC2951
All Decoupling Capacitors are Ceramic Discs.

FIGURE 12 – CONVERSION GAIN

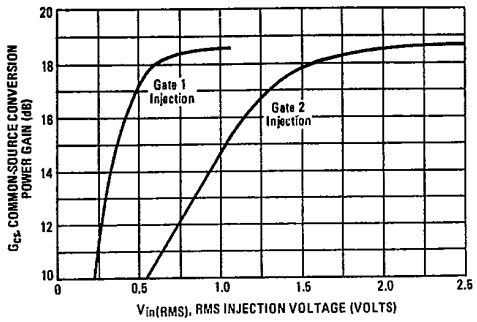


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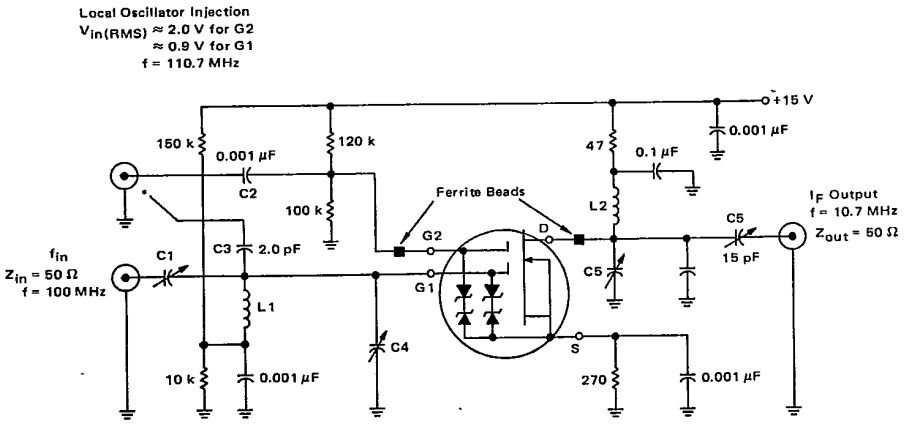
FIGURE 13 – CONVERSION GAIN TEST CIRCUIT



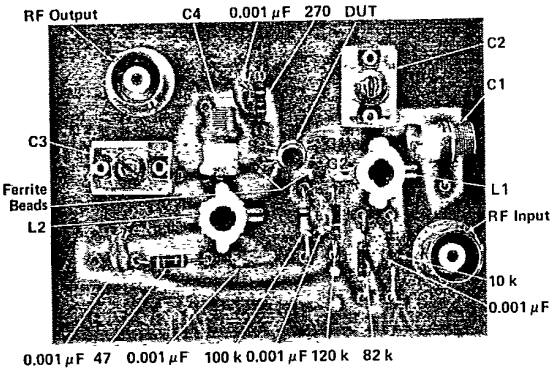
L1 126 nH PAUL SMITH CO. SK-138-1
4-½ Turns (yellow)
L2 2.73 µH High Unloaded Q
C1 JOHANSON JMC2951
C4,C5,C6 ARCO 402

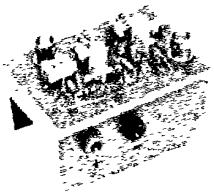
*For G1 injection, C2 is changed to bypass G2 to ground and C3 is added to connect G1 to the injection input.

PRINTED CIRCUIT BOARD LAYOUT INFORMATION

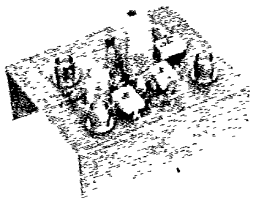
FIGURE 14 – TEST FIXTURES

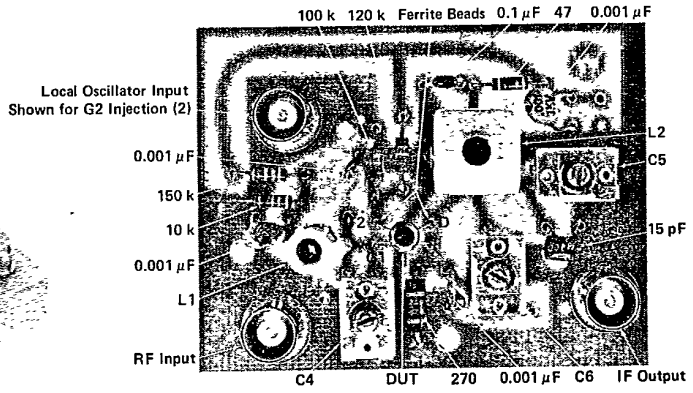
105 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT





100 MHz to 10.7 MHz CONVERSION GAIN TEST CIRCUIT





Notes:
1. C1 is on the bottom side of the board.
2. For G1 injection, C2 is changed to bypass G2 to ground and C3 is added to connect G1 to the injection input. See Figure 13.