TC74HC4514AP
TC74HC4515AP

TC74HC4514AP 4-TO-16 LINE DECODER/LATCH
TC74HC4515AP 4-TO-16 LINE DECODER/LATCH(INV.)

The TC74HC4514A/TC74HC4515A are high speed CMOS 4-LINE TO 16-LINE DECODER WITH LATCHED INPUTs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

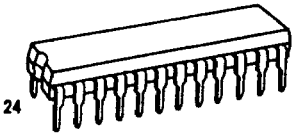
The selected output is enabled by a low on the inhibit input (INHIBIT). A binary code stored in the four input latches (A thru D) is decided and provides a high level (HC4514A) or a low level (HC4515A) at the corresponding one of sixteen outputs. When the INHIBIT is held low, all outputs are kept low (HC4514A) or high (HC4515A), however, the latch function is available.

The data applied to the data inputs are transferred to the outputs of latches when the strobe input is held high. When the strobe input is taken low, the data is retained at the output of the latches.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =18ns(typ.)at V_{CC} =5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 4514B/4515B



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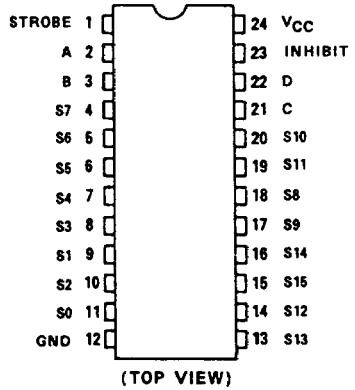
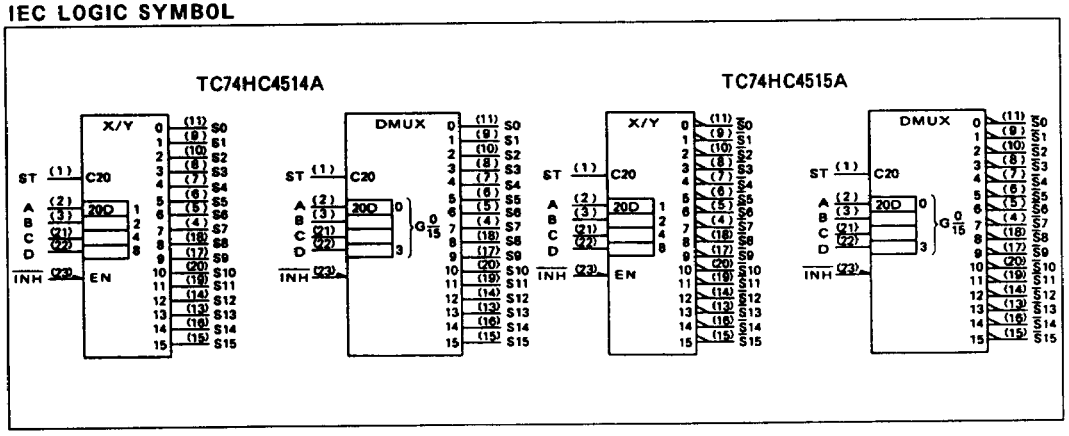
PIN ASSIGNMENT



(TOP VIEW)

NOTE: In case of TC74HC4515A $\overline{S0}$~$\overline{S15}$

IEC LOGIC SYMBOL



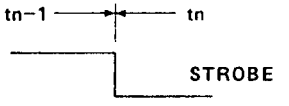
TRUTH TABLE

INPUTS					SELECTED OUTPUTS	
INHIBIT	A	B	C	D	TC74HC4514A-"H"	TC74HC4515A-"L"
L	L	L	L	L	S_0	$\overline{S_0}$
L	H	L	L	L	S_1	$\overline{S_1}$
L	L	H	L	L	S_2	$\overline{S_2}$
L	H	H	L	L	S_3	$\overline{S_3}$
L	L	L	H	L	S_4	$\overline{S_4}$
L	H	L	H	L	S_5	$\overline{S_5}$
L	L	H	H	L	S_6	$\overline{S_6}$
L	H	H	H	L	S_7	$\overline{S_7}$
L	L	L	L	H	S_8	$\overline{S_8}$
L	H	L	L	H	S_9	$\overline{S_9}$
L	L	H	L	H	S_{10}	$\overline{S_{10}}$
L	H	H	L	H	S_{11}	$\overline{S_{11}}$
L	L	L	H	H	S_{12}	$\overline{S_{12}}$
L	H	L	H	H	S_{13}	$\overline{S_{13}}$
L	L	H	H	H	S_{14}	$\overline{S_{14}}$
L	H	H	H	H	S_{15}	$\overline{S_{15}}$
H	X	X	X	X	ALL OUTPUT"L"	ALL OUTPUT"H"

○ X : Don't Care

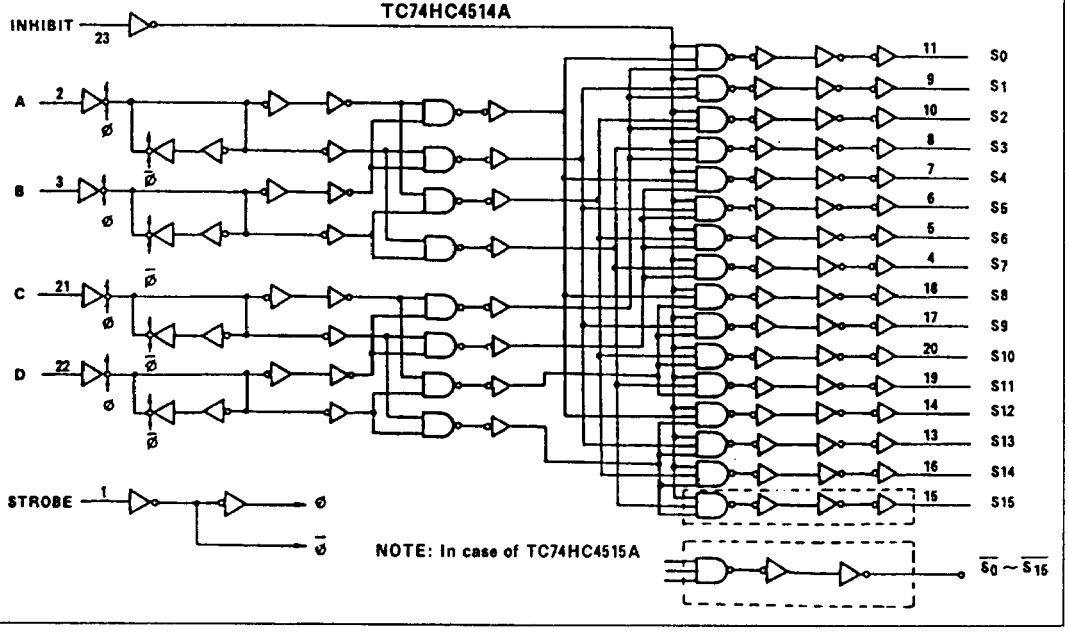
○ STROBE="H"; REFER TO TRUTH TABLE

○ STROBE="H"



Data at the negative going transition of strobe shall be provided on each output while strobe is held low.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (STROBE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (DATA)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (DATA)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		−	18	30	
Propagation Delay Time (STROBE−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		−	20	30	
Propagation Delay Time (INHIBIT−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		−	16	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	ns
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		50	2.0	−	65	175	−	220	
				4.5	−	22	35	−	44	
				6.0	−	19	30	−	37	
Propagation Delay Time (STROBE−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		50	2.0	−	75	175	−	220	
				4.5	−	24	35	−	44	
				6.0	−	20	30	−	37	
Propagation Delay Time (INHIBIT−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		50	2.0	−	60	175	−	220	
				4.5	−	20	35	−	44	
				6.0	−	17	30	−	37	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)				−	61	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$