PLESSEY
Semiconductors

T-73-53

SP9685AC

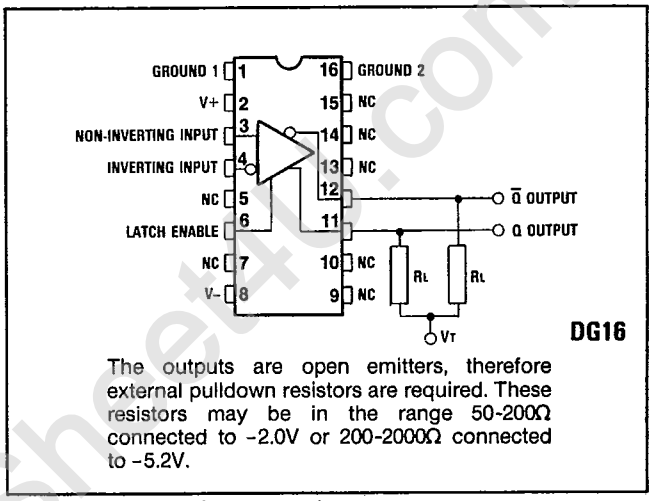
ULTRA FAST COMPARATOR

(CONFORMS TO MIL-STD-883C CLASS B)

The SP9685 is an ultra fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch function enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and -5.2V rails. It is pin and voltage compatible with AD9685 (but faster).



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range 50-200Ω connected to -2.0V or 200-2000Ω connected to -5.2V.

Fig.1 DIL pin connections (top view) and function diagram

FEATURES

- MIL-M-38510 Change Notification Observed
- Full Quality Conformance Inspection
- Propagation Delay 2.2ns Typ.
- Latch Set Up Time 1ns
- Complementary ECL Outputs
- Supply +5V, -5.2V (±0.25V)
- 50 Ohm Line Driving Capability
- Excellent Common Mode Rejection
- Operating Temperature Range: -55°C to +125°C
- Pin Compatible with AD9685
- Pin Compatible with AM685 — But Faster

APPLICATIONS

- Ultra High Speed A/D Converters
- Ultra High Speed Line Receivers
- Peak Detectors
- Threshold Detectors

CHANGE NOTIFICATION

The change notification requirements of MIL-M-38510 will be implemented on this device type. Known customers will be notified of any changes since last buy when ordering further parts if significant changes have been made.

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage:	-6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Power dissipation	350mW
Storage temperature range	-55°C to +150°C
Operating junction temperature	<175°C
Lead temperature (soldering 60 sec)	300°C
Vibration	196m/s²
Shock	14700m/s² peak 0.5ms duration

THERMAL CHARACTERISTICS

θ_{JA} = 120°C/W
θ_{JC} = 35°C/W

Rev.	A	B	C
Date	19 Jan 87	5 Mar 87	15 May 87

ELECTRICAL CHARACTERISTICS

The characteristics apply over the ambient temperature range of -55°C to +125°C
V_{CC} = 5V ± 0.25V : V_{EE} = -5.2V ± 0.25V:
Load resistor R_L = 50Ω to -2.0V dc.

Parameter	Symbol	Value		Sub group	Notes	Method/Conditions/Temp.
		Min.	Max.			
Input offset voltage	V_{OFF}	-5mV	+5mV	1		R_{SOURCE} < 100Ω
Input offset voltage	V_{OFF}	-8mV	+8mV	2,3		R_{SOURCE} < 100Ω
Input bias current	I_B		20μA	1		
Input bias current	I_B		40μA	2,3		
Input offset current	I_{OFF}	-5μA	+5μA	1		
Input offset current	I_{OFF}	-12μA	+12μA	2,3		
Supply current	I_{EE}	-34mA		1		
Supply current	I_{EE}	-37mA		2,3		
Supply current	I_{CC}		23mA	1		
Supply current	I_{CC}		25mA	2,3		
Common mode range	V_{CM}	-2.5V	+2.5V	7,8		Tested by function
ECL output logic level high	V_{OH}	-0.960V	-0.810V	1		Measured at V_{CC} = 5V, V_{EE} = -5.2V
ECL output logic level high	V_{OH}	-0.880V	-0.690V	2		
ECL output logic level high	V_{OH}	-1.060V	-0.890V	3		
ECL output logic level low	V_{OL}	-1.850V	-1.650V	1		
ECL output logic level low	V_{OL}	-1.820V	-1.550V	2		
ECL output logic level low	V_{OL}	-1.900V	-1.650V	3		
Input to output delay	t_{pd}		3ns	9	Note 1	
Input to output delay	t_{pd}		4ns	10,11	Note 1	

NOTES
1. 100mV pulse and +10mV overdrive referred to inverting input.
2. Sub groups 4, 5, 6 are not required.

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested.

Parameter	Symbol	Value		Notes	Method/Conditions/Temp.
		Min.	Max.		
Input capacitance	C_{IN}		3pF		
Latch set-up time	ts		1ns	Note 1	25°C (Q and $\overline{Q}$)
Latch set-up time	ts		2.5ns	Note 1	-55°C to +125°C (Q and $\overline{Q}$)
Latch to output delay	t_{pd} ± (E)		3ns	Note 1	25°C (Q and $\overline{Q}$)
Latch to output delay	t_{pd} ± (E)		5ns	Note 1	-55°C to +125°C (Q and $\overline{Q}$)
Minimum latch pulse width	t_{pw} (E)		3ns	Note 1	25°C
Minimum hold time	th		1ns	Note 1	25°C

NOTES
1. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Device characteristics plus a full conformance testing of other dynamic characteristics guarantees these parameters.

OPERATING NOTES

Timing diagram

The timing diagram, Fig.2, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdirve pulse, switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse with $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Measurement of propagation and latch delays

A simple test circuit is shown in Fig.3. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

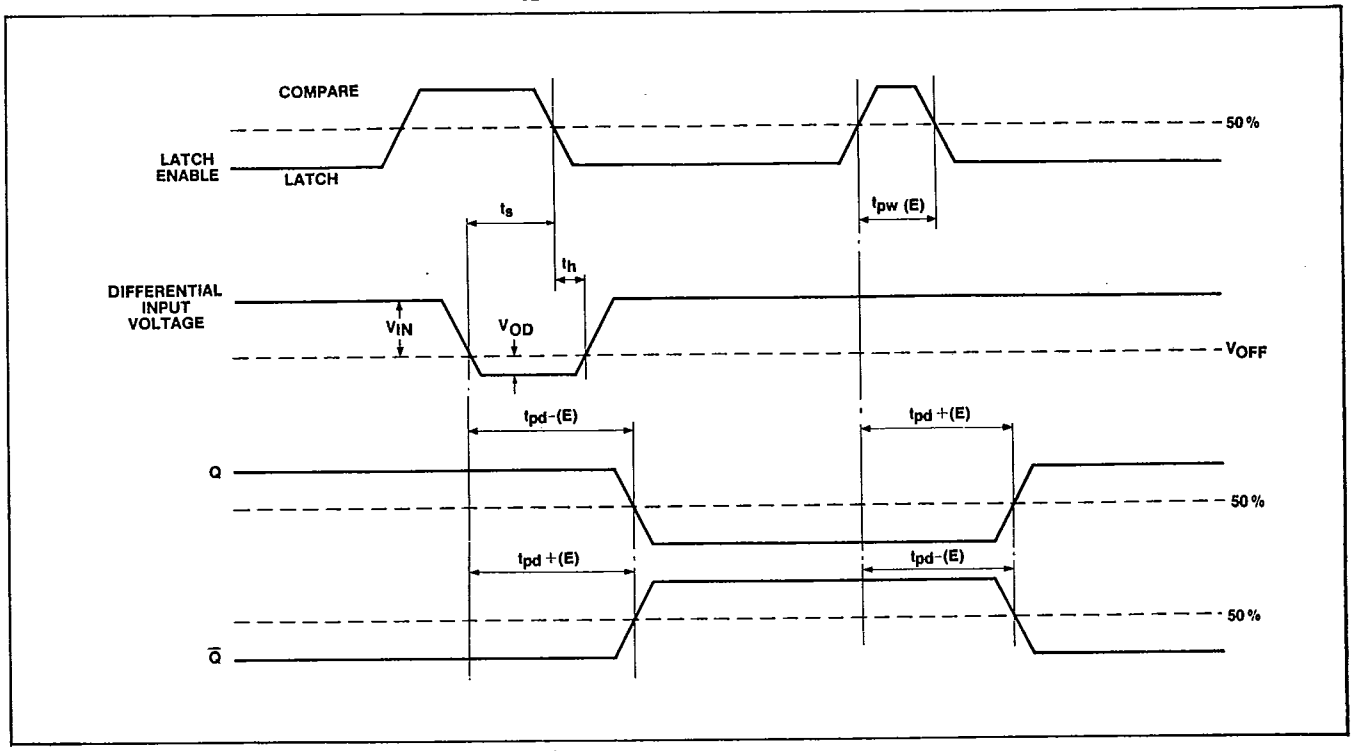
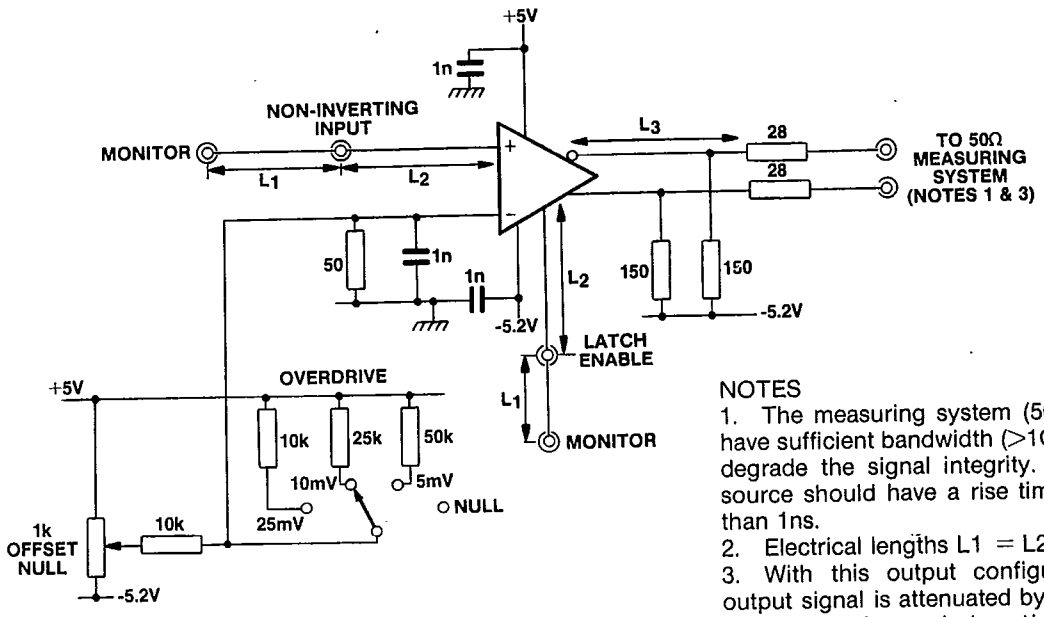


Fig.2 Timing diagram SP9685AC



NOTES
1. The measuring system (50Ω) should have sufficient bandwidth (>1GHz) not to degrade the signal integrity. The signal source should have a rise time of better than 1ns.
2. Electrical lengths L1 = L2 + L3.
3. With this output configuration the output signal is attenuated by the 28Ω to 50Ω pad formed by the system termination.

Fig.3 Test circuit SP9685AC

Latched and unlatched gain

The gain of a high speed, high gain comparator is difficult to measure, because of input noise and the possibility of oscillations when in the linear region. For a full ECL output level swing, the unlatched input shift required is approximately 1mV. In the latched mode, the feedback action in effect enhances the gain and the limitation in the noise/oscillation level; under these conditions the usable resolution is 100μV, although this is only achieved by careful circuit design and layout.

DEFINITION OF TERMS

V_{OFF} Input offset voltage - the potential difference required between the input terminals to cause the output to change state.

I_{OFF} Input offset current - the difference between the currents into the inputs when a potential difference of ±100mV is applied.

Switching terms (Refer to Fig.4)

t_{pd+} Input to output high delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to output low delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ Latch enable to output high delay - The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ Latch enable to output low delay - The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_s Minimum set-up time - The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h The minimum time after the negtive transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ Minimum latch enable pulse width - The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

V_{CM} Input voltage range - The range of input voltages for which the offset and propagation delay specifications are valid.

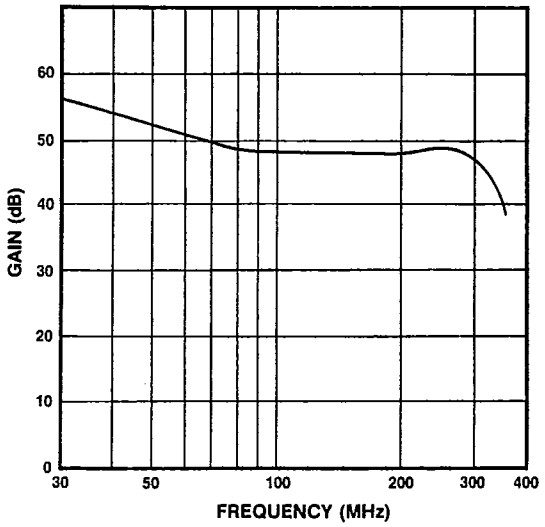


Fig.4 Open loop gain as a function of frequency

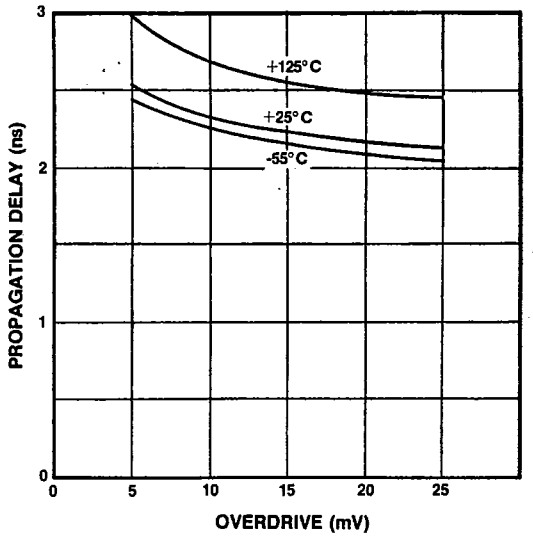


Fig.5 Propagation delay, latch to output as a function of overdrive

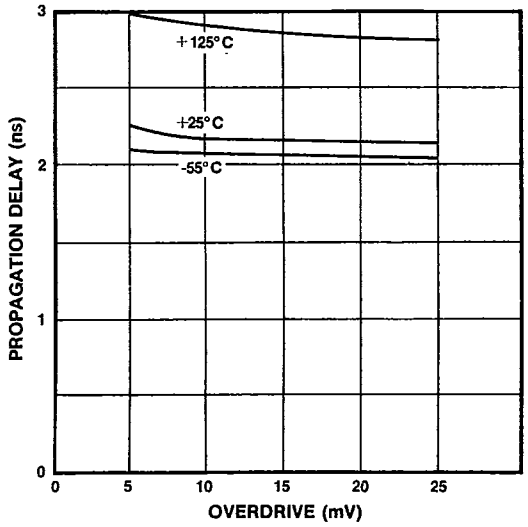


Fig.6 Propagation delay, input to output as a function of overdrive

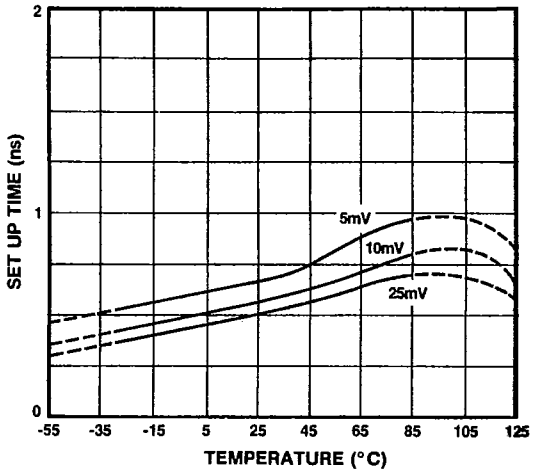


Fig.7 Set-up time as a function of temperature

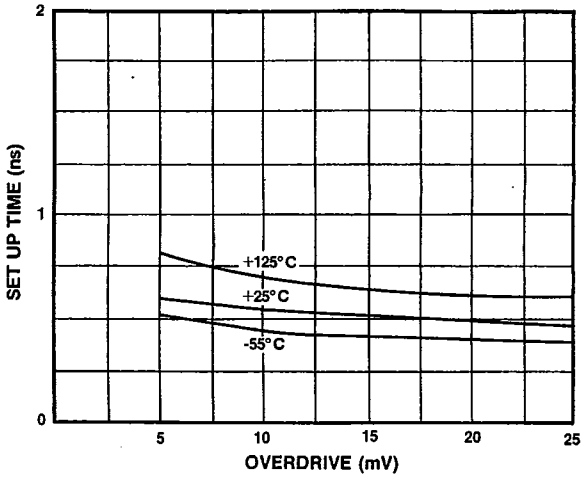


Fig.8 Set-up time as a function of input overdrive

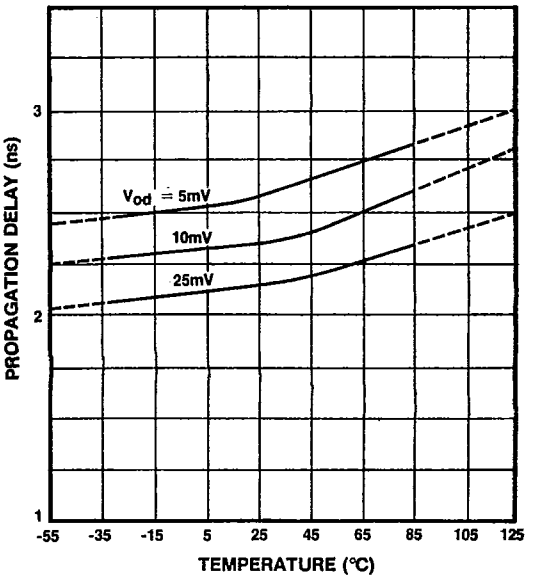


Fig.9 Propagation delay, input to output as a function of temperature

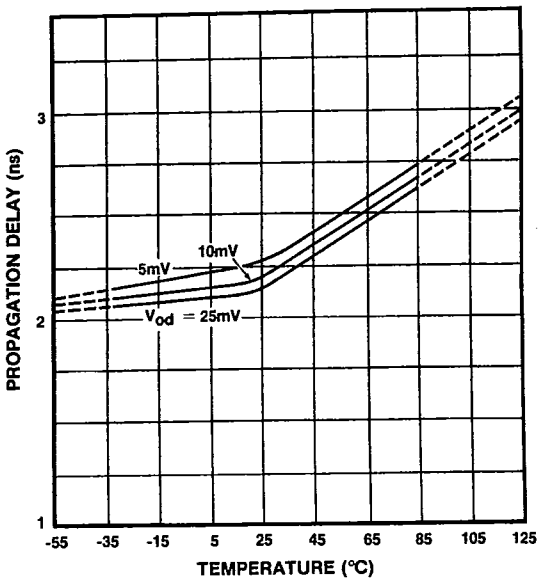


Fig.10 Propagation delay, latch to output as a function of temperature

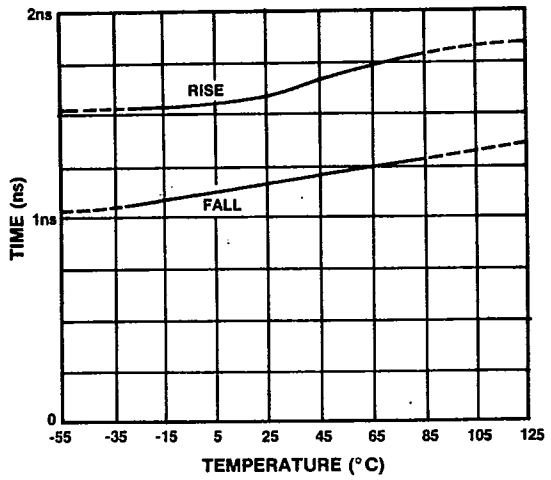


Fig.11 Output rise and fall times as a function of temperature

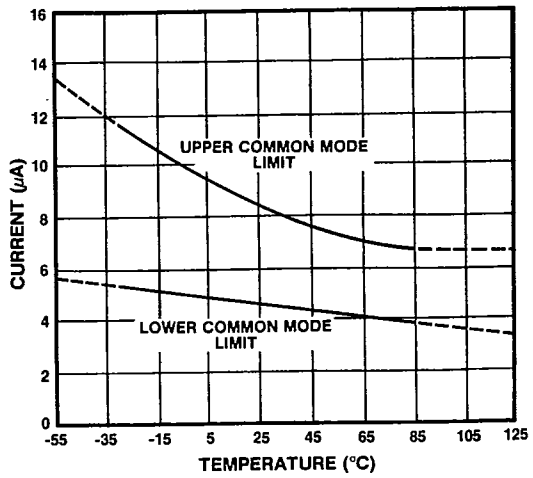


Fig.12 Input bias currents as a function of temperature

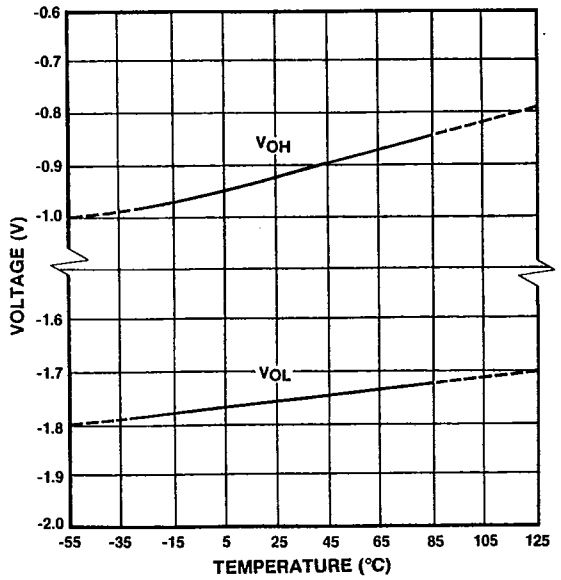


Fig.13 Output levels as a function of temperature

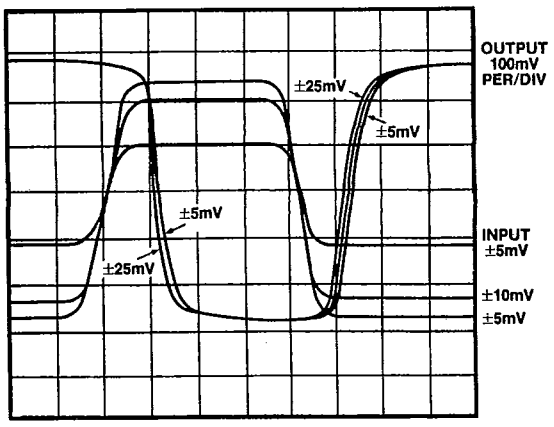


Fig.14 Response to various input signal levels

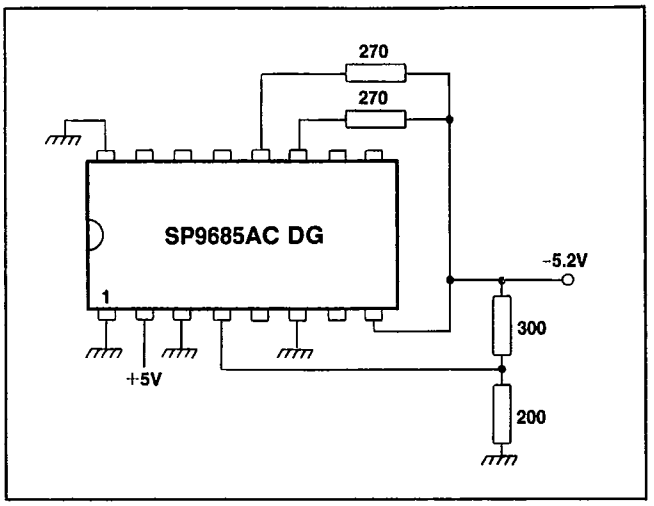
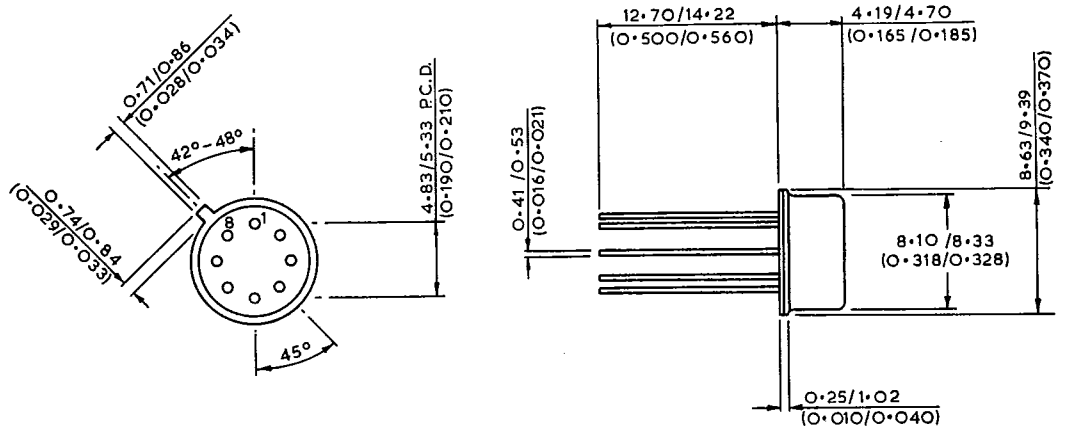
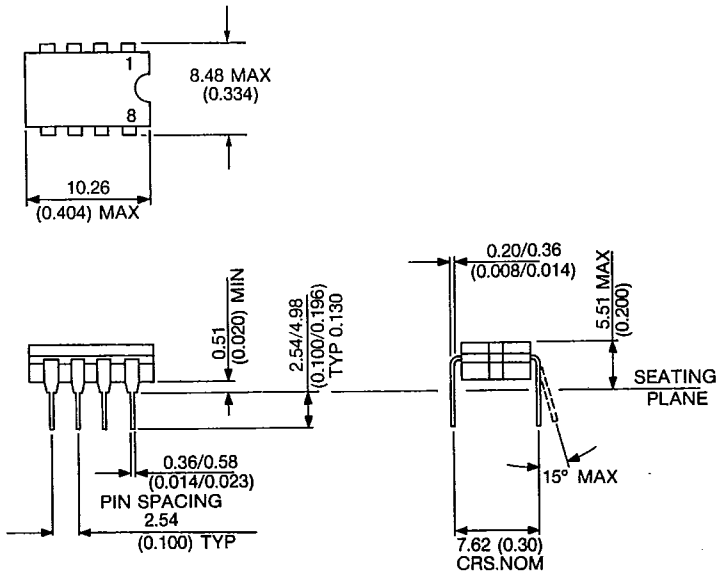


Fig.15 Burn-in/life test circuit
NOTES: (1) PDA is 5% and based on sub groups 1 and 7.
(2) Burn-in temperture is +125°C



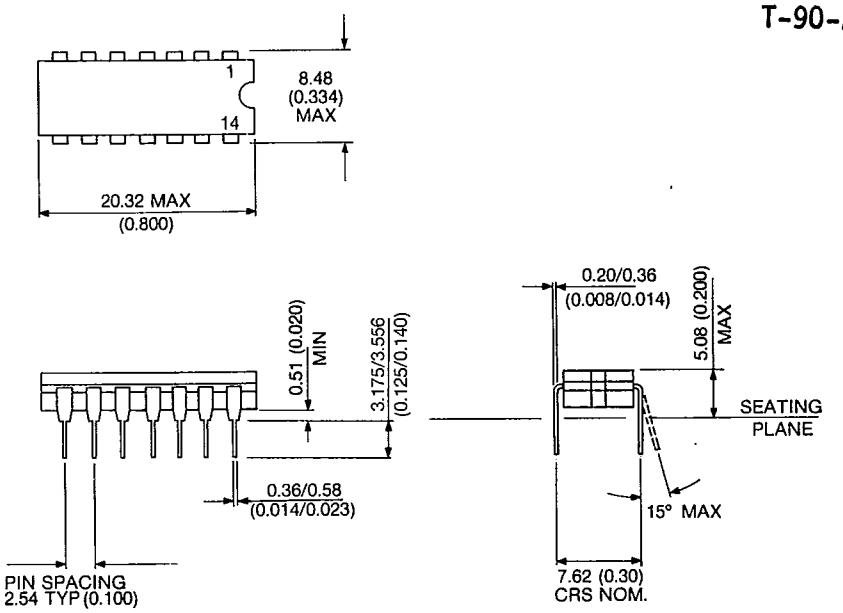
NOTE: This package does not have 'standoff' and therefore does not conform fully to MIL-M-38510F case outline A-1.

8-LEAD METAL CAN

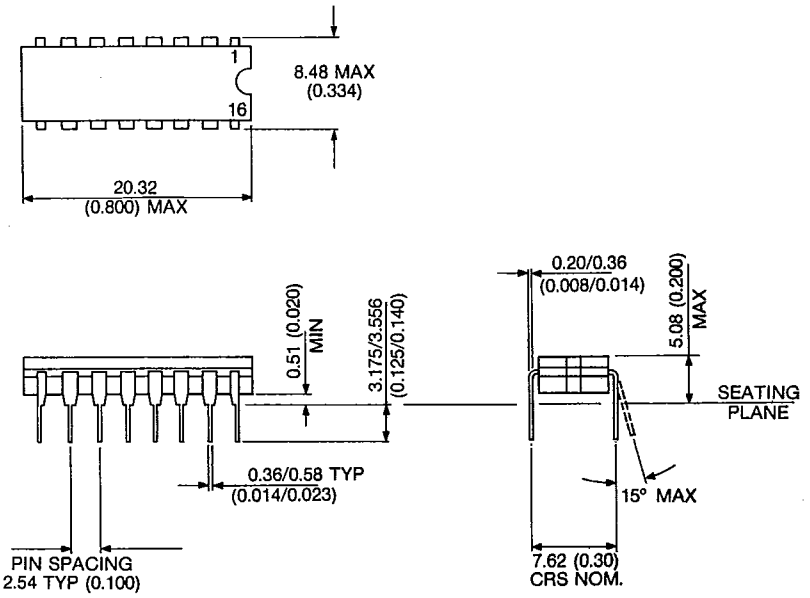


8 LEAD CERAMIC DIL CERDIP - DG8

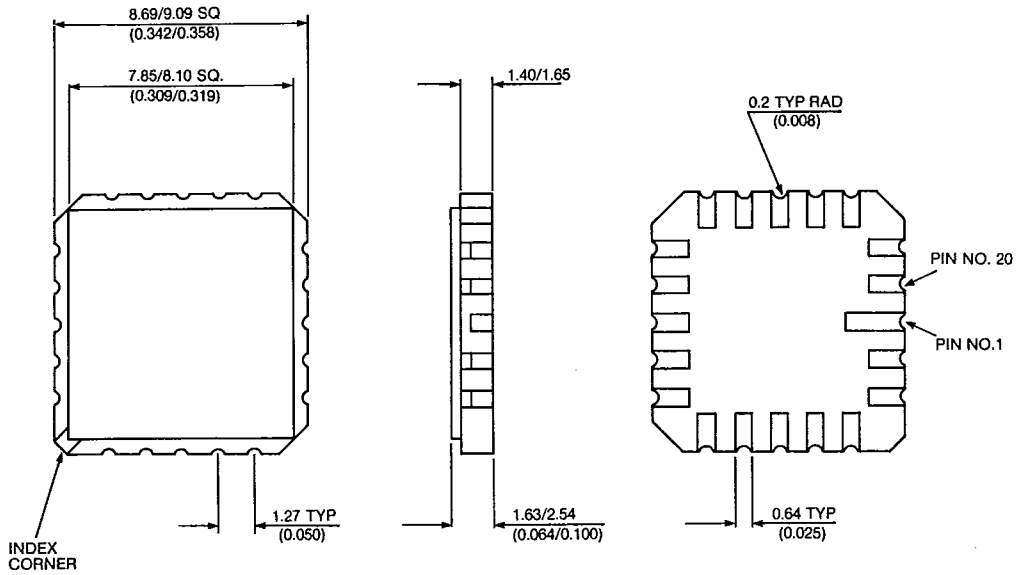
T-90-20



14 LEAD CERAMIC DIL CERDIP - DG14



16 LEAD CERAMIC DIL CERDIP - DG16



20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)