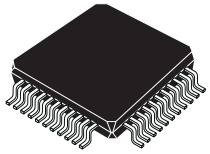
ST7538Q

FSK power line transceiver

General features

- Half duplex frequency shift keying (FSK) transceiver
- Integrated power line driver with programmable voltage and current control
- Programmable interface:
  - Synchronous
  - Asynchronous
- Single supply voltage (from 7.5 up to 12.5V)
- Very low power consumption (Iq = 5mA)
- Integrated 5V voltage regulator (up to 50mA) with short circuit protection
- Integrated 3.3V voltage regulator (up to 50mA) with short circuit protection
- 3.3V or 5V digital supply
- 8 programmable transmission frequencies
- Programmable baud rate up to 4800BPS
- Receiving sensitivity up to 250µVrms
- Suitable to application in accordance with EN 50065 CENELEC specifications
- Carrier or preamble detection
- Band in use detection
- Programmable 24 or 48 bit register with security checksum
- Mains zero crossing detection and synchronization
- Watchdog timer
- Output voltage freeze
- 8 or 16 bit header recognition
- UART/SPI host interface
- ST7537 compatible



TQFP44 Slug Down

Description

The ST7538Q is a Half Duplex synchronous/asynchronous FSK Modem designed for power line communication network applications. It operates from a single supply voltage and integrates a line driver and two linear regulators for 5V and 3.3V. The device operation is controlled by means of an internal register, programmable through the synchronous serial interface. Additional functions as watchdog, clock output, output voltage and current control, preamble detection, time-out, band in use are included. Realized in Multipower BCD5 technology that allows to integrate DMOS, Bipolar and CMOS structures in the same chip.

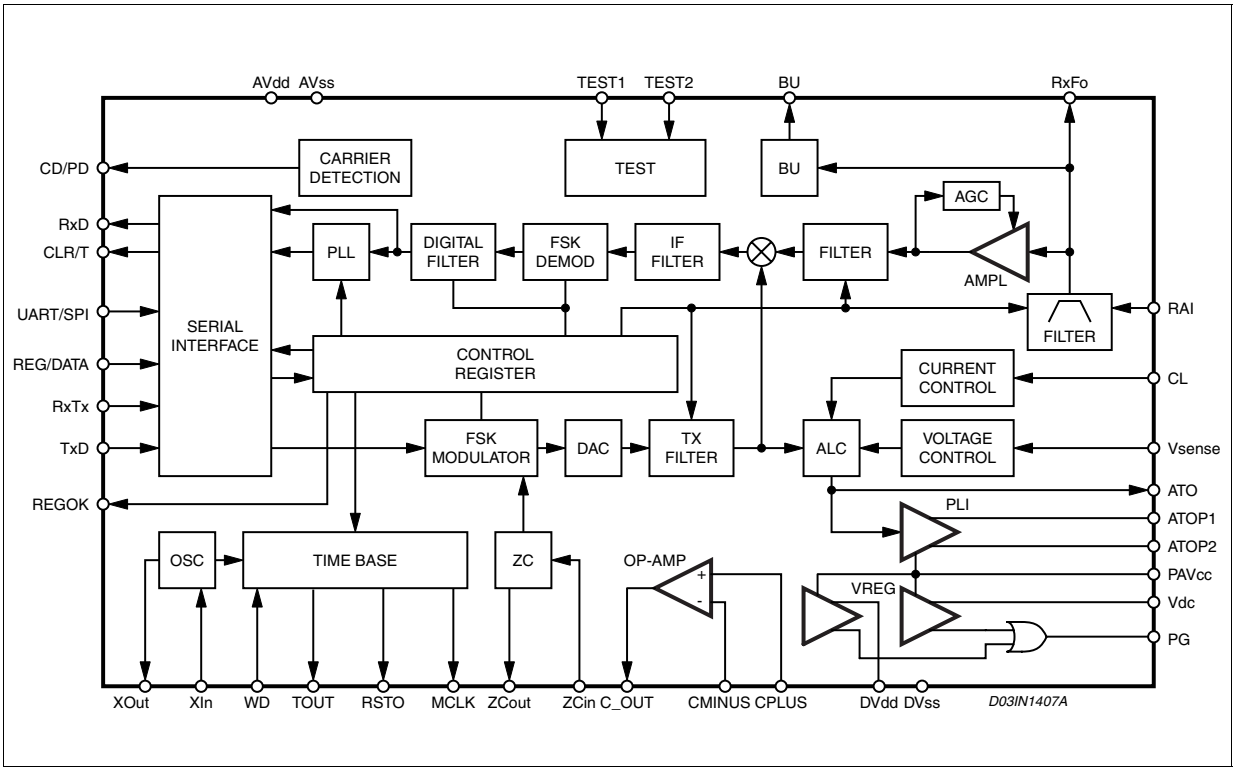
Order codes

Part number	Package	Packaging
ST7538Q	TQFP44 Slug Down	Tube
ST7538QTR	TQFP44 Slug Down	Tape and reel

Contents

1 Block diagram

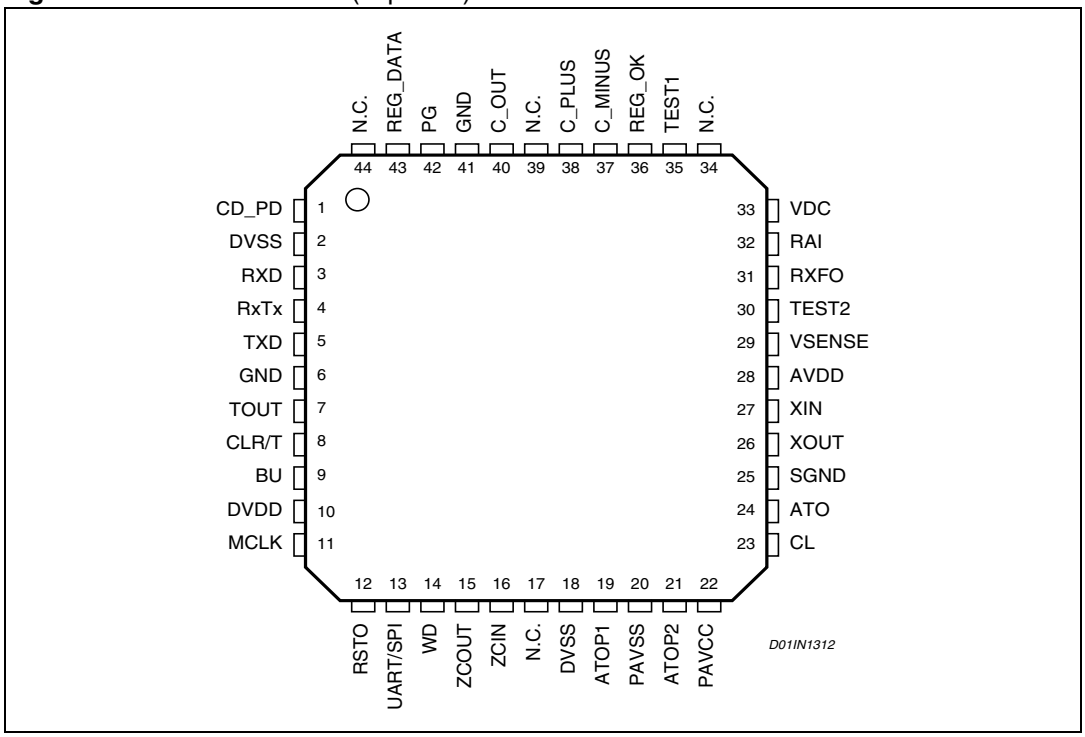
Figure 1. Block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin Connection (Top view)



2.2 Pin description

Table 1. Pin description

Pin N°	Name	Type	Description
1	CD_PD	Digital/Output	Carrier, Preamble or Frame Header Detect Output. "1" No Carrier, Preamble or Frame Header Detected "0" Carrier, Preamble or Frame Header Detected
2	DVss	Supply	Digital Ground
3	RxD	Digital/Output	RX Data Output.
4	RxTx	Digital/Input with internal pull-up	Rx or Tx mode selection input. "1" - RX Session "0" - TX Session
5	TxD	Digital/Input with internal pull-down	TX Data Input.
6	GND	Supply	Substrate Ground (same function as PIN 41)
7	TOUT	Digital/Output	TX Time Out Event Detection "1" - Time Out Event Occurred "0" - No Time-out Event Occurred
8	CLR/T	Digital/Output	Synchronous Mains Access Clock or Control Register Access Clock
9	BU	Digital/Output	Band in use Output. "1" Signal within the Programmed Band "0" No Signal within the Programmed Band
10	DVdd	Supply	Digital Supply Voltage or 3.3V Voltage Regulator Output
11	MCLK	Digital/Output	Master Clock Output
12	RSTO	Digital/Output	Power On or Watchdog Reset Output
13	UART/SPI	Digital/Input with internal pull-down	Interface type: “0” - Serial Peripheral Interface “1” - UART Interface
14	WD	Digital/Input with internal pull-up	Watchdog input. The Internal Watchdog Counter is cleared on the falling edges.
15	ZCOUT	Digital/Output	Zero Crossing Detection Output
16	ZCIN(1)	Analog/Input	Zero Crossing AC Input.
17	NC	Floating	Must be connected to DVss.
18	DVss	Supply	Digital Ground
19	ATOP1	Power/Output	Power Line Driver Output
20	PAVss	Supply	Power Analog Ground
21	ATOP2	Power/Output	Power Line Driver Output
22	PAV_{CC}	Supply	Power Supply Voltage
23	CL(2)	Analog/Input	Current Limiting Feedback. A resistor between CL and AVss sets the PLI Current Limiting Value An integrated 80pF filtering input capacitance is present on this pin
24	ATO	Analog/Output	Small Signal Analog Transmit Output

Table 1. Pin description (continued)

Pin N°	Name	Type	Description
25	SGND	Supply	Analog Signal Ground
26	XOUT	Analog Output	Crystal Output
27	XIN	Analog Input	Crystal Oscillator Input - External Clock Input
28	AVdd	Supply	Analog Power supply.
29	Vsense(3)	Analog/Input	Output Voltage Sensing input for the voltage control loop
30	TEST2	Analog/Input	Test Input must be connected SGND
31	RxFO	Analog/Output	Receiving Filter Output
32	RAI	Analog/Input	Receiving Analog Input
33	VDC	Power	5V Voltage Regulator Output
34	NC	floating	Must Be connected to DVss.
35	TEST1	Digital/Input with internal pull-down	Test input. Must Be connected to DVss.
36	REGOK	Digital/Output	Security checksum logic output "1" - Stored data Corrupted "0" - Stored data OK
37	C_MINUS(4)	Analog/Input	Op-amp Inverting Input.
38	C_PLUS(5)	Analog/Input	Op-amp Not Inverting Input.
39	NC	floating	Must Be connected to DVss
40	C_OUT	Analog/Output	Op-amp Output
41	GND	Supply	Substrate Ground (same function as PIN 6)
42	PG	Digital/Output	Power Good logic Output "1" - VDC is above 4.5V and DVdd is above 3.125V "0" - VDC is below 4.25V or DVdd is below 2.875V
43	REG_DATA	Digital/Input with internal pull-down	Mains or Control Register Access Selector "1" - Control Register Access "0" - Mains Access
44	NC	floating	Must be connected to DVss.

1. If not used this pin must be connected to VDC
2. Cannot be left floating
3. Cannot be left floating
4. If not used this pin must be connected to VDC
5. If not used this pin must be tied low (SGND or PAVss or DVss)

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PAV_{CC}	Power Supply Voltage	-0.3 to +14	V
AV_{dd}	Analog Supply Voltage	-0.3 to +5.5	V
DV_{dd}	Digital Supply Voltage	-0.3 to +5.5	V
AV_{ss}/DV_{ss}	Voltage between AV_{ss} and DV_{ss}	-0.3 to +0.3	V
V_I	Digital input Voltage	DV_{ss} - 0.3 to DV_{dd} +0.3	V
V_O	Digital output Voltage	DV_{ss} - 0.3 to DV_{dd} +0.3	V
I_O	Digital Output Current	-2 to +2	mA
V_{sense}, XIN, C_MINUS ,C_PLUS, CL	Voltage Range at Vsense, XIN, C_MINUS, C_PLUS, CL Inputs	AV_{ss} - 0.3 to AV_{dd}+0.3	V
RAI, ZCIN	Voltage Range at RAI, ZCIN Inputs	$-AV_{dd}$ - 0.3 to AV_{dd} +0.3	V
ATO, RxFO, C_OUT, XOUT	Voltage range at ATO, RxFO, C_OUT, XOUT Outputs	AV_{ss} - 0.3 to AV_{dd} +0.3	V
ATOP1,2	Voltage range at Powered ATO Output	AV_{ss} - 0.3 to $+PAV_{cc}$ +0.3	V
ATOP	Powered ATO Output Current (1)	400	mArms
T_{amb}	Operating ambient Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-50 to 150	°C
CD_PD Pin	Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002- “Human Body Model” Acceptance Criteria: “Normal Performance”	±1500	V
Other pins		±2000	V

1. This current is intended as not repetitive pulse current

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	TQFP44 with slug	Unit
R_{thJA1}	Maximum Thermal Resistance Junction-Ambient Steady state (1)	35	°C/W
R_{thJA2}	Maximum Thermal Resistance Junction-Ambient Steady state (2)	50	°C/W

1. Mounted on Multilayer PCB with a dissipating surface on the bottom side of the PCB
2. It's the same condition of the point above, without any heatsinking surface on the board.

4 Electrical characteristics

Table 4. Electrical characteristics
(AVdd = DVdd = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V, -40°C ≤T_A ≤85°C, T_J < 125 °C, fc = 86kHz, other control register parameters as default value, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
AV_{dd}, DV_{dd}	Supply voltages		4.75	5	5.25	V
PAV_{dd} - DV_{dd}	PAV_{CC} and DV_{dd} Relation during Power-Up Sequence	DV_{dd} < 4.75V with 5V Digital supply provided externally	0.1		1.2	V
PAV_{CC} - AV_{dd}	PAV_{CC} and AV_{dd} Relation during Power-Up Sequence	AV_{dd} < 4.75V	0.1		1.2	V
PAV_{cc}	Power Supply Voltage		7.5		12.5	V
	Max allowed slope during Power-Up				100	V/ms
AI_{dd} + DI_{dd}	Input Supply Current	Transmission & Receiving mode		5	7	mA
I PAV_{CC}	Powered Analog Supply Current	TX mode (no load)		30	50	mArms
		RX mode		500	1000	µA
		Maximum total current			370	mArms
UVLO	Input Under Voltage Lock Out Threshold on PAVcc		3.7	3.9	4.1	V
$UVLO_{HYS}$	UVLO Hysteresis			340		mV
Digital I/O						
R_{down}	Pull Down Resistor			100		kΩ
R_{up}	Pull up Resistor			100		kΩ

Table 4. Electrical characteristics (continued)
(AVdd = DVdd = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V, -40°C ≤T_A ≤85°C, T_J < 125 °C, fc = 86kHz, other control register parameters as default value, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Digital I/O 5V digital supply						
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level input Voltage				1.2	V
V_{OH}	High Logic Level Output Voltage	I_{OH}= -2mA	DVdd -0.75			V
V_{OL}	Low Logic Level Output Voltage	I_{OL}= 2mA			DVss + 0.3	V
Digital I/O 3.3V digital supply						
V_{IH}	High Logic Level Input Voltage		1.4			V
V_{IL}	Low Logic Level input Voltage				0.8	V
V_{OH}	High Logic Level Output Voltage	I_{OH}= -2mA	DVdd -0.75			V
V_{OL}	Low Logic Level Output Voltage	I_{OL}= 2mA			DVss + 0.4	V
Oscillator						
XIN_{SWING}	XIN Input Voltage swing	External Clock. *Figure 19*		5		V
XIN_{OFFSET}	XIN Input Voltage offset	External Clock. *Figure 19*		2.5		V
DC	XTAL Clock Duty Cycle	External Clock. *Figure 19*	40		60	%
Xtal	Crystal Oscillator frequency	Fundamental	16			MHz
Tclock	Oscillator Period (1/Xtal)		62.5			ns
$Xtal_{ESR}$	External Oscillator Esr Resistance				40	Ω
$Xtal_{CL}$	External Oscillator Stabilization Capacitance				16	pF
Transmitter						
IATO	Output Transmitting Current on ATO				1	mArms
V_{ATO}	Max Carrier Output AC Voltage	R_{CL} = 1.75kΩ $Vsense_{(AC)}$ = 0V	1.75	2.3	3.5	V_{PP}
V_{ATODC}	Output DC Voltage on ATO		1.7	2.1	2.5	V

Table 4. Electrical characteristics (continued)
(AVdd = DVdd = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V, -40°C ≤T_A ≤85°C, T_J < 125 °C, fc = 86kHz, other control register parameters as default value, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$HD2_{ATO}$	Second Harmonic Distortion on ATO	V_{ATO} = $2V_{PP}$		-55	-42	dB_c
$HD3_{ATO}$	Third Harmonic Distortion on ATO			-52	-49	dB_c
IATOP	Output Transmitting Current in programmable current limiting	Rcl = 1.85kΩ; R_{LOAD} = 1Ω (as in *Figure 14*)	250	310	370	mArms
$V_{ATOP(AC)}$	Max Carrier Output AC Voltage for each ATOP1 and ATOP2 pins	R_{CL} = 1.t5kΩ Vsense(AC) = 0V $PAVcc \geq \frac{VATOP(AC)}{2} + 7.5V$	3.5	4.6	6	V_{pp}
$V_{ATOP(DC)}$	Output DC Voltage on ATOP1 and ATOP2 pins		3.5	4.2	5	V
$HD2_{ATOP}$	Second Harmonic Distortion on each ATOP1 and ATOP2 pins	V_{ATOP} = $4V_{PP}$, PAVCC = 10V No Load		-55	-42	dB_c
		V_{ATOP} = $4V_{PP}$, PAVCC = 10V R_{LOAD} =50Ω (Differential) Carrier Frequency: 132.5KHz		-65	-53	dB_c
$HD3_{ATOP}$	Third Harmonic Distortion on each ATOP1 and ATOP2 pins	V_{ATOP} = $4V_{PP}$, PAVCC = 10V No Load.		-56	-49	dB_c
		V_{ATOP} = $4V_{PP}$, PAVCC = 10V R_{LOAD} =50Ω (Differential) Carrier Frequency: 132.5KHz		-65	-52	dB_c
VATOP	Accuracy with Voltage Control Loop Active	R_{CL} = 1.75Ω; Vsense(AC) = 0V	-1		+1	GST
GST	ALC Gain Step Control loop gain step		0.6	1	1.4	dB
DRNG	ALC Dynamic Range			30		dB
$Vsense_{TH}$	Voltage control loop reference threshold on V_{sense} pin	*Figure 14*	160	180	200	mV_{PK}
$Vsense_{HYS}$	Hysteresis on Voltage loop reference threshold	*Figure 14*		±18		mV
$V_{SENSE(DC)}$	Output DC Voltage on VSENSE			1.865		V
V_{SENSE}	VSENSE Input Impedance			36		kΩ

Table 4. Electrical characteristics (continued)
(AVdd = DVdd = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V, -40°C ≤T_A ≤85°C, T_J < 125 °C, fc = 86kHz, other control register parameters as default value, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
C_{CL}	Input capacitance on CL pin			80		pF
CCL_{TH}	Current control loop reference threshold on C_L pin	*Figure 14*	1.80	1.90	2.00	V
CCL_{HYST}	Hysteresis on Current loop reference threshold	*Figure 14*	210	250	290	mV
T_{RxTx}	Carrier Activation Time	*Figure 17* - 600 Baud Xtal=16MHz	0.01		1.6	ms
		Figure 17- 1200 Baud Xtal=16MHz	0.01		800	µs
		Figure 17- 2400 Baud Xtal=16MHz	0.01		400	µs
		Figure 17- 4800 Baud Xtal=16MHz	0.01		200	µs
TALC	Carrier Stabilization Time From STEP 16 to zero or From step 16 to step 31,	*Figure 17* Xtal =16MHz			3.2	ms
T_{ST}	Tstep	*Figure 17* Xtal =16MHz			200	µs
Receiver						
V_{IN}	Input Sensitivity (Normal Mode)			0.5	2	mV_{rms}
	Input Sensitivity (High Sens.)			250		$µV_{rms}$
V_{IN}	Maximum Input Signal				2	V_{rms}
R_{IN}	Input Impedance		80	100	140	kΩ
V_{CD}	Carrier detection sensitivity (Normal Mode)			0.5	2	mV_{rms}
	Carrier detection sensitivity (High Sensitivity Mode)			250		$µV_{rms}$
	Carrier detection sensitivity (TxD line forced to “1”)	UART/SPI pin forced to “1”		V_{BU}		dB/ µVrms
V_{BU}	Band in Use Detection Level			77	85	dB/ µVrms

Table 4. Electrical characteristics (continued)
(AVdd = DVdd = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V, -40°C ≤T_A ≤85°C, T_J < 125 °C, fc = 86kHz, other control register parameters as default value, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
5V voltage regulator						
VDC	Linear regulator output voltage	0 < Io < 50mA 7.5V < PAVcc < 12.5V	-5%	5.05	+5%	V
PG_{VDC}	Power Good Output Voltage Threshold on VDC pin		4.3	4.5	4.7	V
$PG_{VDC(HYS)}$	PG on VDC pin Hysteresis			250		mV
3.3V voltage regulator						
DVdd	Linear Regulator Output Voltage	0 < Io < 50mA 7.5V < PAVcc < 12.5V	-5%	3.3	+5%	V
PG_{DVdd}	Power Good Output Voltage Threshold on DVdd pin			3.125		V
$PG_{DVdd(HYS)}$	PG on DVdd pin Hysteresis			250		mV
Other functions						
T_{RSTO}	Reset Time	See *Figure 21*; Xtal = 16MHz	50			ms
T_{WD}	Watch-dog Pulse Width	See *Figure 21*	3.5			ms
T_{WM}	Watch-dog Pulse Period	See *Figure 21*	T_{WD} + 3.5		1490	ms
T_{WO}	Watch-dog Time Out	See *Figure 21*			1.5	s
T_{OUT}	TX TIME OUT	Control Register Bit 7 and Bit 8 See *Figure 20*		1 3		s
T_{OFF}	Time Out OFF Time	See *Figure 20*	125			ms
T_{OFFD}	RxTx 0->1 vs. TOUT Delay	See *Figure 20*			20	µs
T_{CD}	Carrier Detection Time selectable by register	Control Register bit 9 and bit10 *Figure 11*		500 1 3 5		µs ms ms ms
T_{DCD}	CD_PD Propagation Delay	*Figure 11*		300	500	µs
M_{CLK}	Master Clock Output Selectable by register	Control Register bit 15 and bit 16 see *Table 11*		fclock fclock/2 fclock/4 off		MHz
B_{AUD}	Baud rate	Control Register bit 3 and bit 4 see *Table 11*		600 1200 2400 4800		Baud

Table 4. Electrical characteristics (continued)
(AVdd = DVdd = +5V, PAVcc =+9 V, PAVss, SGND = DVss = 0V, -40°C ≤T_A ≤85°C, T_J < 125 °C, fc = 86kHz, other control register parameters as default value, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_B	Baud rate Bit Time (=1/$_{BAUD}$)	Control Register bit 3 and bit 4 see *Table 11*		1667 833 417 208		µs
Zero crossing detection						
ZC_{DEL}	Zero Crossing Detection delay (delay between the ZCIN and ZCOUT signals)	*Figure 22*			1	µs
$ZC_{(LOW)}$	Zero Crossing Detection Low Threshold		-45		-5	mV
$ZC_{(HIGH)}$	Zero Crossing Detection High Threshold		5		+45	mV
$ZC_{(OFFSET)}$	Zero Crossing Offset		-20		+20	mV
Operational amplifier						
$C_{OUT(Sync)}$	Max Sync Current		15	28	45	mA
$C_{OUT(Source)}$	Max Source Current		-30	-20	-10	mA
$C_{IN(Offset)}$	Input Terminals OFFSET		-38		+38	mV
GBWP	Gain Bandwidth Product		6	7	9	MHz
Serial interface						
Ts	Setup Time	see *Figure 5*, *6*, *7*, *8* & *9*			5	ns
T_H	Hold Time	see *Figure 5*, *6*, *7*, *8* & *9*			2	ns
T_{CR}	CLR/T vs. REG_DATA or RxTx	see *Figure 5*, *6*, *7*, *8* & *9*			$T_B/4$	
T_{CC}	CLR/T vs. CLR/T	see *Figure 5*, *6*, *7*, *8* & *9*	T_B		$2*T_B$	
T_{DS}	Setup Time	see *Figure 5*, *6*, *7*, *8* & *9*	$T_B/4$		$T_B/2$	
T_{DH}	Hold Time	see *Figure 5*, *6*, *7*, *8* & *9*	$T_B/4$		$T_B/2$	
T_{CRP}			T_H		$T_B/2$	

5 Functional description

5.1 Carrier frequencies

ST7538Q is a multi frequency device: eight programmable Carrier Frequencies are available (see *Table 5*).
Only one Carrier could be used a time. The communication channel could be varied during the normal working Mode to realize a multifrequency communication.
Selecting the desired frequency in the Control Register the Transmission and Reception filters are accordingly tuned.

Table 5. ST7538Q Channels List

FCarrier	F (KHz)
F0	60
F1	66
F2	72
F3	76
F4	82.05
F5	86
F6	110
F7(1)	132.5

5.2 Baud rates

ST7538Q is a multi Baud rate device: four Baud Rate are available (See *Table 6.*).

Table 6. ST7538Q mark and space tones frequency distance vs baud rate and deviation

Baud Rate [Baud]	ΔF (1) (Hz)	Deviation (2)
600	600	1 (3)
1200	600 1200	0.5 1
2400 (4)	1200 (4) 2400	0.5 1
4800	2400 4800	0.5 1

1. Frequency deviation.
2. Deviation = ΔF / (Baud Rate)
3. Deviation 0.5 Not Allowed
4. Default value

5.3 Mark and space frequencies

Mark and space communication frequencies are defined by the following formula:

F ("0") = FCarrier + [Δ**F**]/2

F ("1") = FCarrier - [Δ**F**]/2

Δ**F** is the Frequency Deviation.

With Deviation = “0.5” the difference in terms of frequency between the mark and space tones is half the Baudrate value (Δ**F** = 0.5*BAudrate). When the Deviation = “1” the difference is the Baudrate itself (Δ**F** = Baudrate). The minimal Frequency Deviation is 600Hz.

Table 7. ST7538Q synthesized frequencies

Carrier Frequency (KHz)	Baud Rate	Deviation	Exact Frequency [Hz] (Clock=16MHz)		Carrier Frequency (KHz)	Baud Rate	Deviation	Exact Frequency [Hz] (Clock=16MHz)	
			“1”	“0”				“1”	“0”
60	600	--			82.05	600	--		
		1	59733	60221			1	81706	82357
	1200	0.5	59733	60221		1200	0.5	81706	82357
		1	59408	60547			1	81380	82682
	2400	0.5	59408	60547		2400	0.5	81380	82682
		1	58757	61198			1	80892	83171
	4800	0.5	58757	61198		4800	0.5	80892	83171
		1	57617	62337			1	79590	84473
66	600	--			86	600	--		
		1	65755	66243			1	85775	86263
	1200	0.5	65755	66243		1200	0.5	85775	86263
		1	65430	66569			1	85449	86589
	2400	0.5	65430	66569		2400	0.5	85449	86589
		1	64779	67220			1	84798	87240
	4800	0.5	64779	67220		4800	0.5	84798	87240
		1	63639	68359			1	83659	88379

Table 7. ST7538Q synthesized frequencies

Carrier Frequency (KHz)	Baud Rate	Deviation	Exact Frequency [Hz] (Clock=16MHz)		Carrier Frequency (KHz)	Baud Rate	Deviation	Exact Frequency [Hz] (Clock=16MHz)	
			"1"	"0"				"1"	"0"
72	600	--			110	600	--		
		1	71777	72266			1	109701	110352
	1200	0.5	71777	72266		1200	0.5	109701	110352
		1	71452	72591			1	109375	110677
	2400	0.5	71452	72591		2400	0.5	109375	110677
		1	70801	73242			1	108724	111165
	4800	0.5	70801	73242		4800	0.5	108724	111165
		1	69661	74382			1	107585	112467
76	600	--			132.5	600	--		
		1	75684	76335			1	132161	132813
	1200	0.5	75684	76335		1200	0.5	132161	132813
		1	75358	76660			1	131836	133138
	2400	0.5	75358	76660		2400	0.5	131836	133138
		1	74870	77148			1	131348	133626
	4800	0.5	74870	77148		4800	0.5	131348	133626
		1	73568	78451			1	130046	134928

5.4 ST7538Q mains access

ST7538Q can access the Mains in two different ways:

- Synchronous access
- Asynchronous access

The choice between the two types of access can be performed by means of Control Register bit 14 (see *Table 11*) and affects the ST7538Q data flow in Transmission Mode as in Reception Mode (for how to set the communication Mode, see *Section 5.5 on page 18*).

In Data Transmission Mode:

– Synchronous Mains access: on clock signal provided by ST7538Q (CLR/T line) rising edge, data transmission line (TxD line) value is read and sent to the FSK Modulator. ST7538Q manages the Transmission timing according to the BaudRate Selected.

– Asynchronous Mains access: data transmission line (TxD line) value enters directly to the FSK Modulator. The Host Controller manages the Transmission timing (CLR/T line should be neglected).

In Data Reception Mode:

- Synchronous Mains access: on clock signal recovered by a PLL from ST7538Q (CLR/T line) rising edge, value on FSK Demodulator is read and put to the data reception line (RxD line). ST7538Q recovers the bit timing according to the BaudRate Selected.
- Asynchronous Mains access: Value on FSK Demodulator is sent directly to the data reception line (RxD line). The Host Controller recovers the communication timing (CLR/T line should be neglected).

5.5 Host processor interface

ST7538Q exchanges data with the host processor through a serial interface.

The data transfer is managed by REG_DATA and RxTx Lines, while data are exchanged using RxD, TxD and CLR/T lines.

Four are the ST7538Q working modes:

- Data Reception
- Data Transmission
- Control Register Read
- Control Register Write

REG_DATA and RxTx lines are level sensitive inputs.

Table 8. Data and control register access bits configuration

	REG_DATA	RxTx
Data Transmission	0	0
Data Reception	0	1
Control Register Read	1	1
Control Register Write	1	0

ST7538Q features two type of Host Communication Interfaces:

- SPI
- UART

The selection can be done through the UART/SPI pin. If UART/SPI pin is forced to “0” SPI interface is selected while if UART/SPI pin is forced to “1” UART interface is selected [(a)]. The type of interface affects the Data Reception by setting the idle state of RxD line. When ST7538Q is in Receiving mode (REG_DATA=”0” and RxTx =“1”) and no data are available on mains (or RxD is forced to an idle state, i.e. with a conditioned Detection Method), the RxD line is forced to “0” when UART/SPI pin is forced to ”0” or to “1” when UART/SPI pin is forced to ”1”.

a. UART Interface Mode modifies also Control Register Functions and provides one more level of Rx sensitivity (see par. 5.11)

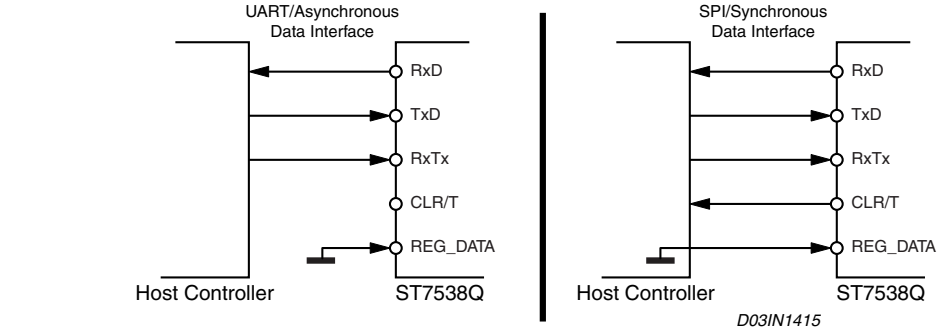
The UART interface allows to connect an UART compatible device instead SPI interface allows to connect an SPI compatible device. The allowed combinations of Host Interface/ST7538Q Mains Access are:

Table 9. Host Interface / ST7538Q mains access combinations

Host Device interface type	UART/SPI pin	Communication mode	Mains access	
			Asynchronous	Synchronous
UART	“1”	Transmission	X	
UART	“1”	Reception	X	X(1)
SPI	“0”	Transmission		X
SPI	“0”	Reception		X

1. Received Data more stable than in Asynchronous Mains Access

Figure 3. Synchronous and asynchronous ST7538Q/Host controller interfaces



ST7538Q allows to interface the Host Controller using a five line interface (RxD,TxD,RxTx, CLR/T, & REG_DATA) in case of Synchronous mains access or using a 3 line interface (RxD,TxD & RxTx) in Asynchronous mains access. Since Control Register is not accessible in Asynchronous mode, in this case REG_DATA pin can be tied to GND.

5.5.1 Communication between host and ST7538Q

The Host can achieve the Mains access by selecting REG_DATA = ”0” and the choice between Data Transmission or Data Reception is performed by selecting RxTx line (if RxTx =“1” ST7538Q receives data from mains, if RxTx = ”0” ST7538Q transmits data over the mains).

Communication between Host and ST7538Q is different in Asynchronous and Synchronous mode:

- **Asynchronous mode**

  In Asynchronous Mode, data are exchanged without any data Clock reference. The host controller has to recover the clock reference in receiving Mode and control the Bit time in transmission mode.

  If RxTx line is set to “1” & REG_DATA = ”0” (Data Reception), ST7538Q enters in an Idle State. After Tcc time the modem starts providing received data on RxD line.

  If RxTx line is set to “0” & REG_DATA=”0” (Data Transmission), ST7538Q enters in an Idle State and transmission circuitry is switched on. After Tcc time the modem starts transmitting data present on TxD line.

- **Synchronous mode**

  In Synchronous Mode ST7538Q is always the master of the communication and provides the clock reference on CLR/T line.
  When ST7538Q is in receiving mode an internal PLL recovers the clock reference. Data on RxD line are stable on CLR/T rising Edge.

  When ST7538Q is in transmitting mode the clock reference is internally generated and TxD line is sampled on CLR/T rising Edge.

  If RxTx line is set to “1” & REG_DATA=”0” (Data Reception), ST7538Q enters in an Idle State and CLR/T line is forced Low. After Tcc time the modem starts providing received data on RxD line.

  If RxTx line is set to “0” & REG_DATA=”0” (Data Transmission), ST7538Q enters in an Idle State and transmission circuitry is switched on. After Tcc time the modem starts transmitting data present on TxD line (*Figure 5*) .

Figure 4. Receiving and transmitting data/recovered clock timing

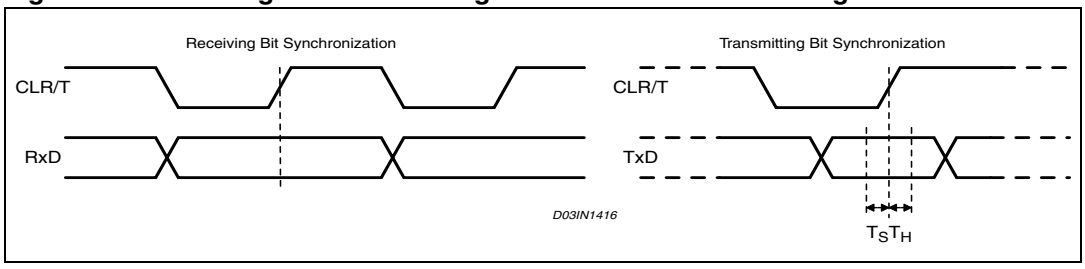
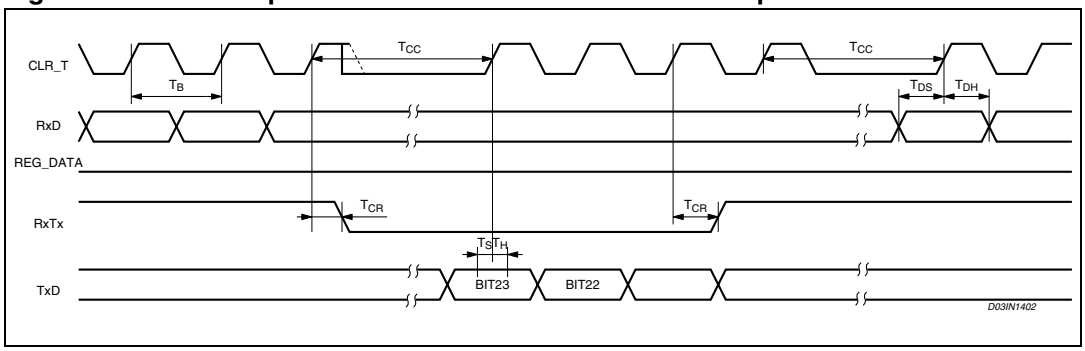


Figure 5. Data reception -> data transmission -> data reception



5.6 Control register access

The communication with ST7538Q Control Register is always synchronous. The access is achieved using the same lines of the Mains interface (RxD, TxD, RxTx and CLR/T) plus REG_DATA Line.

With REG_DATA = 1 and RxTx = 0, the data present on TxD are loaded into the Control Register MSB first. The ST7538Q samples the TxD line on CLR/T rising edges. The control Register content is updated at the end of the register access section (REG_DATA falling edge).

In Normal Control Register mode (Control Register bit 21=”0”, see *Table 11*) if more than 24 bits are transferred to ST7538Q only latest 24 bits are stored inside the Control Register. If less than 24 bits are transferred to ST7538Q the Control Register writing is aborted (in this case if at least 16 bits are provided REGOK line will be activated).

In order to avoid undesired Control Register writings caused by REG_DATA line fluctuations (for example because of surge or burst on mains), in Extended Control Register mode (Control Register bit 21=”1” see *Table 11*) exactly 24 or 48 bits must be transferred to ST7538Q in order to properly write the Control Register, otherwise writing is aborted and if at least 16 bits are provided REGOK line will be activated. If 24 bits are transferred, only the first 24 Control Register bits (from 23 to 0) are written.

With REG_DATA = 1 and RxTx = 1, the content of the Control Register is sent on RxD port. The Data on RxD are stable on CLR/T rising edges MSB First. In Normal Control Register mode 24 bits are transferred from ST7538Q to the Host. In Extended Control Register mode 24 or 48 bits are transferred from ST7538Q to the Host depending on content of Control Register bit 18 (with bit 18 = ”0” the first 24 bits are transferred, otherwise all 48 bits are transferred, see *Table 11*).

Figure 6. Data reception -> control register read -> data reception timing diagram

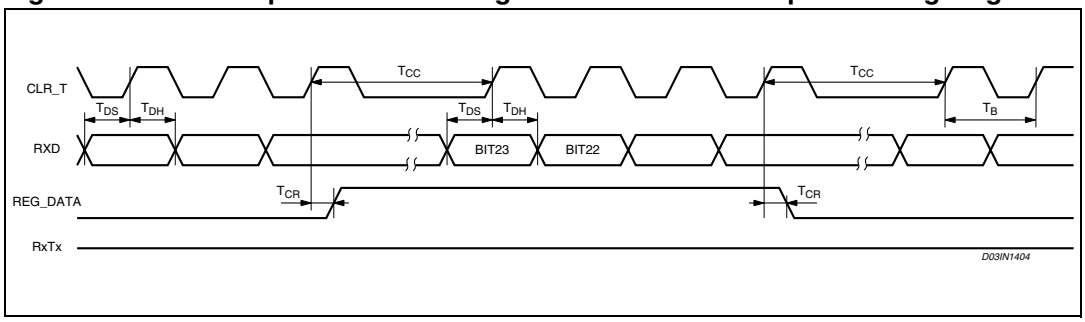


Figure 7. Data reception -> control register write -> data reception timing diagram

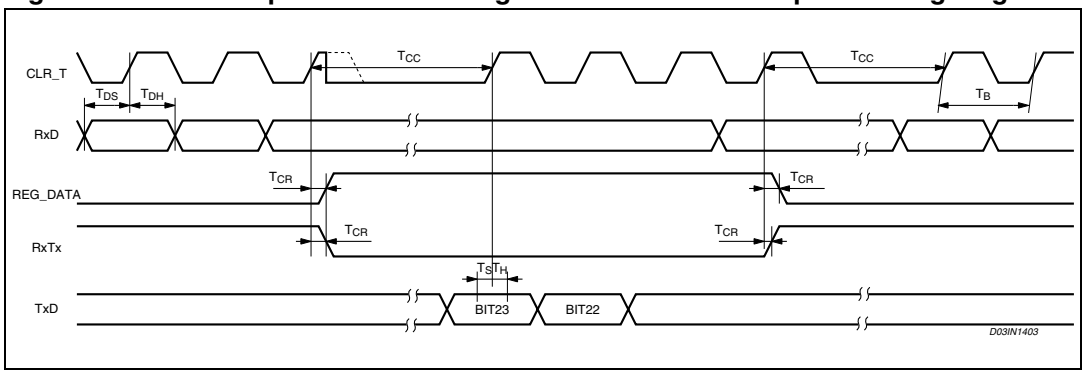


Figure 8. Data transmission -> control reg. read data -> reception timing diagram

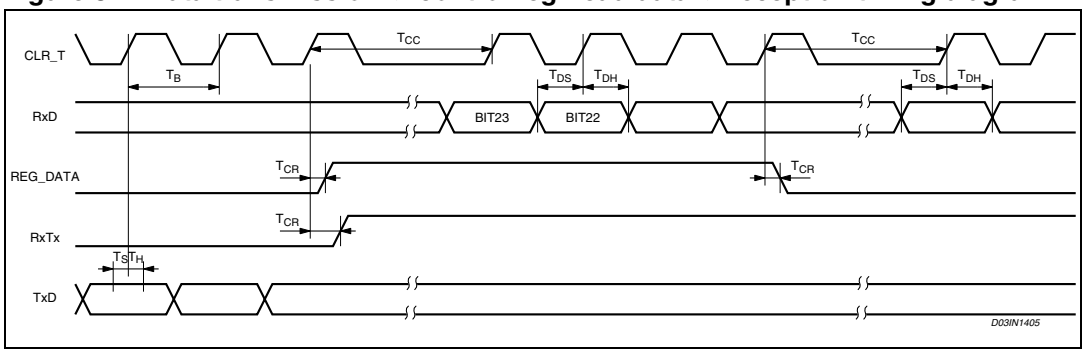
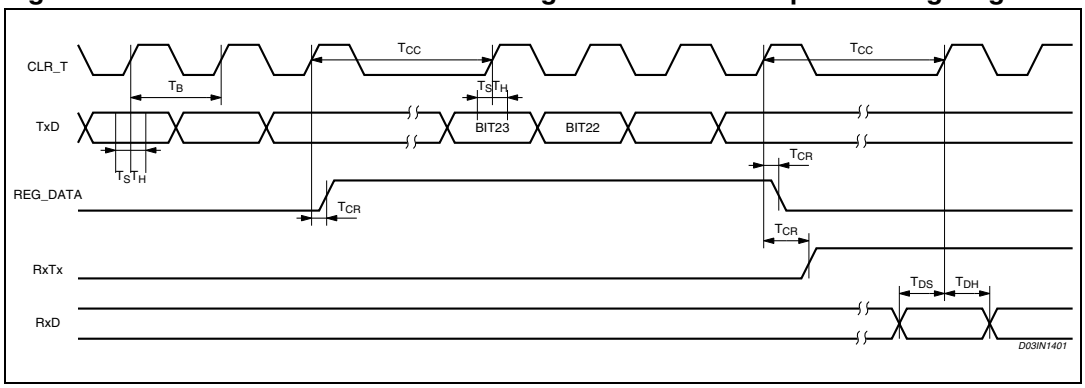


Figure 9. Data transmission -> control reg. write -> data reception timing diagram



5.7 Receiving mode

The receive section is active when RxTx Pin = ”1” and REG_DATA = 0.
The input signal is read on RAI Pin using SGND as ground reference and then pre-filtered by a Band pass Filter (62kHz max bandwidth at -3dB). The Pre-Filter can be inserted setting one bit in the Control Register. The Input Stage features a wide dynamic range to receive Signal with a Very Low Signal to Noise Ratio. The Amplitude of the applied waveform is automatically adapted by an Automatic Gain Control block (AGC) and then filtered by a Narrow Band Band-Pass Filter centered around the Selected Channel Frequency (14kHz max at -3dB). The resulting signal is down-converted by a mixer using a sinewave generated by the FSK Modulator. Finally an Intermediate Frequency Band Pass-Filter (IF Filter) improves the Signal to Noise ration before sending the signal to the FSK demodulator. The FSK demodulator then send the signal to the RX Logic for final digital filtering. Digital filtering Removes Noise spikes far from the BAUD rate frequency and Reduces the Signal Jitter. RxD Line is forced at logic level “0” or “1” (according the UART/SPI pin level) when neither mark or space frequencies are detected on RAI Pin.
Mark and Space Frequency in Receiving Mode must be distant at least BaudRate/2 to have a correct demodulation.
While ST7538Q is in Receiving Mode (RxTx pin = ”1”), the transmit circuitry, Power Line Interface included, is turned off. This allows the device to achieve a very low current consumption (5mA typ). In Receiving mode ATOP2 pin is internally connected to PAVSS.

5.7.1 High sensitivity mode

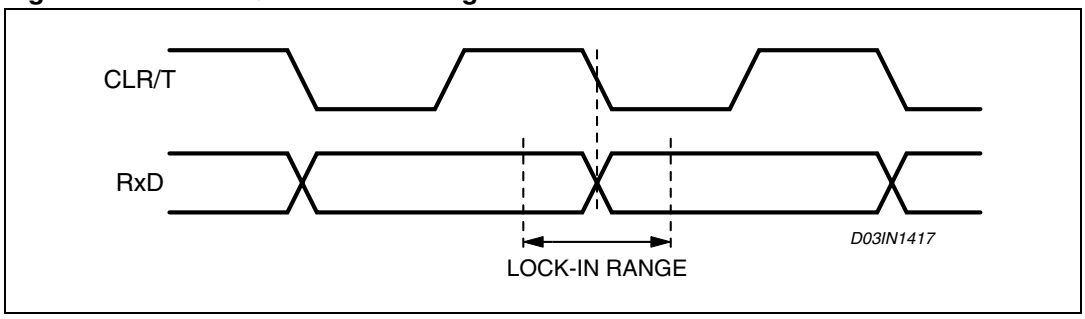
It is possible to increase the ST7538Q Receiving Sensitivity setting to ‘1’ the High Sensitivity Bit of Control Register [(b)]. This function allows to increase the communication reliability when the ST7538Q sensitivity is the limiting factor.

5.7.2 Synchronization recovery system (PLL)

ST7538Q embeds a Clock Recovery System to feature a Synchronous data exchange with the Host Controller.
The clock recovery system is realized by means of a second order PLL. Data on the data line (RxD) are stable on CLR/T line rising edge (CLR/T Falling edge synchronized to RxD line transitions ± LOCK-IN Range).
The PLL Lock-in and Lock-out Range is $\pm\pi/2$. When the PLL is in the unlock condition, CLR/T and RxD lines are forced to a low logic level.
When PLL is in unlock condition it is sensitive to RxD Rising and Falling Edges. The maximum number of transition required to reach the lock-in condition is 5. When in lock-in condition the PLL is sensitive only to RxD rising Edges to reduce the CLR/T Jitter.
ST7538Q PLL is forced in the un-lock condition, when more than 32 equal symbols are received.
Due to the fact that the PLL, in lock-in condition, is sensitive only to RxD rising edge, sequences equal or longer than 15 equal symbols can put the PLL into the un-lock condition.

b. A third level of Rx sensitivity can be selected in UART Interface Mode (see par. 5.11)

Figure 10. ST7538Q PLL lock-in range



5.7.3 Carrier/preamble detection

The Carrier/Preamble Block is a digital Frequency detector Circuit.
It can be used to manage the MAINS access and to detect an incoming signal.
Two are the possible setting:

- **Carrier detection**: The Carrier/Preamble detection Block notifies to the host controller the presence of a Carrier when it detects on the RAI Input a signal with an harmonic component close to the programmed Carrier Frequency. The CD_PD signal sensitivity is identical to the data reception sensitivity (0.5mVrms Typ. in Normal Sensitivity Mode).
  The CD_PD line is forced to a logic level low when a Carrier is detected.
- **Preamble_detection**: The Carrier/Preamble detection Block notifies to the host controller the presence of a Carrier modulated at the Programmed Baud Rate for at least 4 Consecutive Symbols (“1010” or “0101” are the symbols sequences detected). CD_PD line is forced low till a Carrier signal is detected and PLL is in the lock-in range. To reinforce the effectiveness of the information given by CD_PD Block, a digital filtering is applied on Carrier or Preamble notification signal (See Control Register Paragraph). The Detection Time Bits in the Control Register define the filter performance. Increasing the Detection Time reduces the false notifications caused by noise on main line. The Digital filter adds a delay to CD_PD notification equal to the programmed Detection Time. When the carrier frequency disappears, CD_PD line is held low for a period equal to the detection time and then forced high. During this time the some spurious data caused by noise can be demodulated.

5.7.4 Header recognition

In Extended Control Register Mode (Control Register bit 21 = ”1”, see *Table 11*) the CD_PD line can be used to recognize if an header has been sent during the transmission. With Header Recognition function enable (Control Register bit 18 = ”1”, see *Table 11*), CD_PD line is forced low when a Frame Header is detected. If Frame Length Count function is enabled, CD_PD is held low and a number of 16 bit word equal to the Frame Length selected is sent to the host controller. In this case, CLR/T is forced to “0” and RxD is forced to “0” or “1” (according the UART/SPI pin level) when Header has not been detected or after the Frame Length has been reached.
If Frame Length Count function is disabled, an header recognition is signaled by forcing CD_PD low for one period of CLR/T line. In this case, CLR/T and RxD signal are always present, even if no header has been recognized.

Figure 11. CD_PD timing during RX

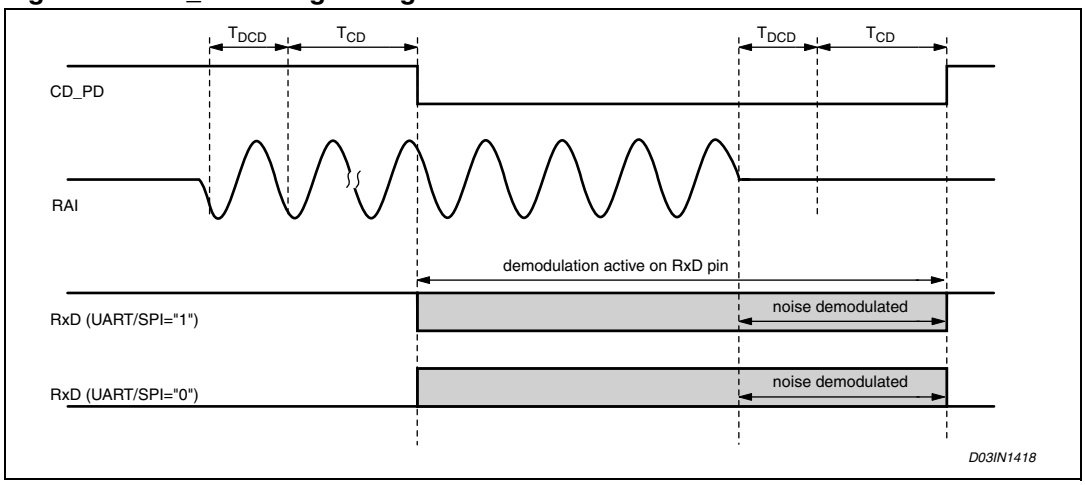
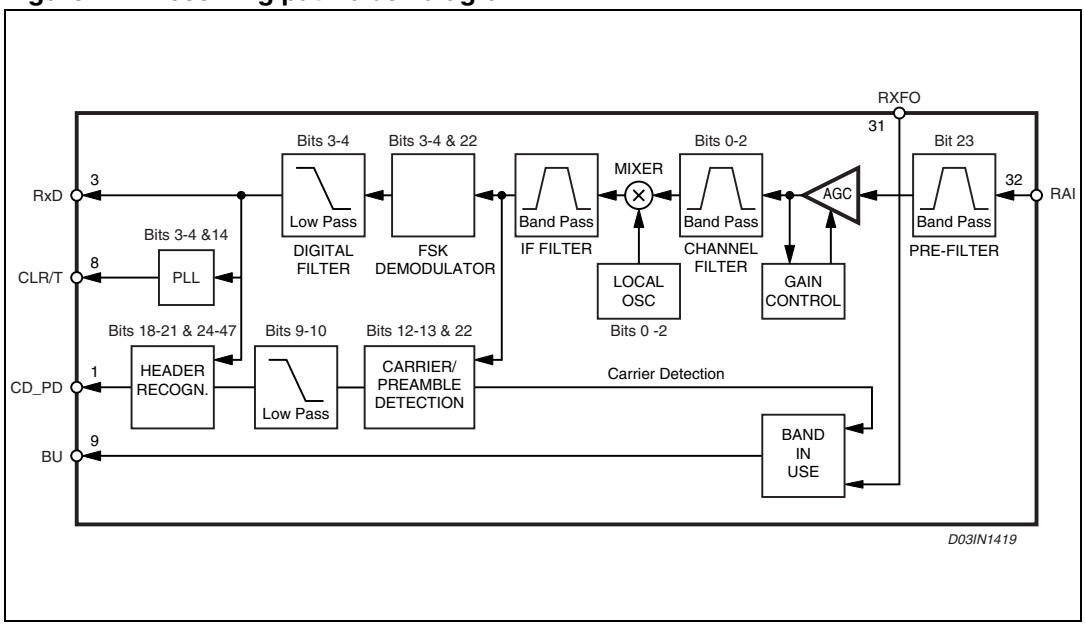


Figure 12. Receiving path block diagram



5.8 Transmission mode

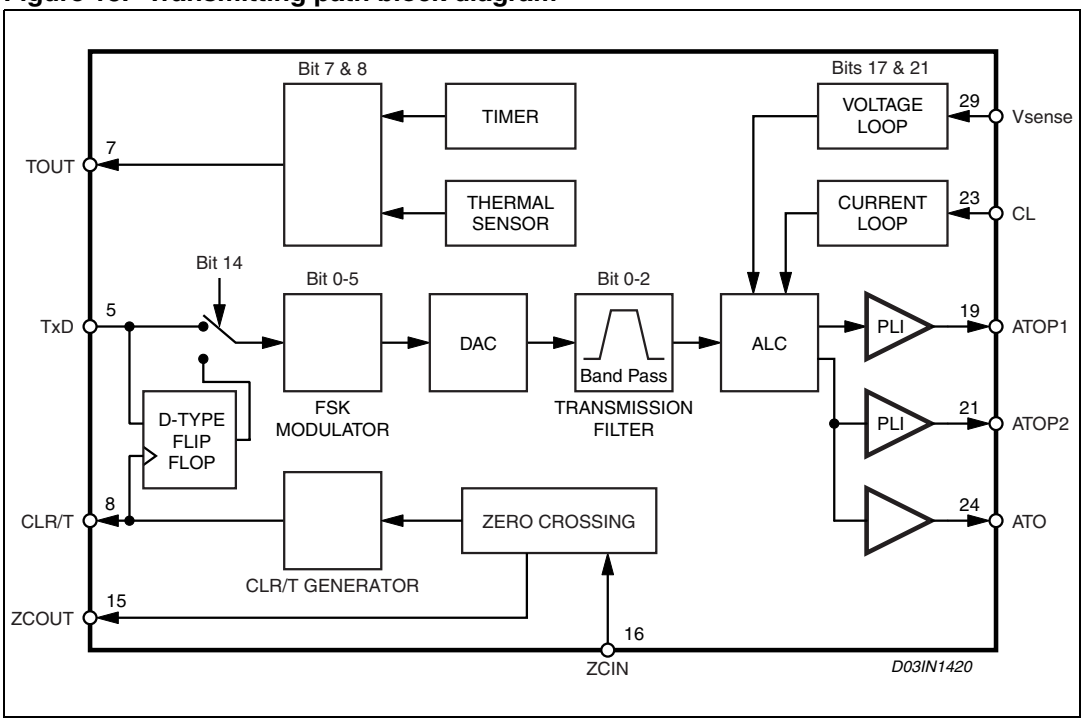
The transmit mode is set when RxTx Pin = ”0” and REG_DATA Pin = ”0”. In transmitting mode the FSK Modulator and the Power Line Interface are turned ON. The transmit Data (TXD) enter synchronously or asynchronously to the FSK modulator.

- Host Controller Synchronous Communication Mode: on CLR/T rising edge, TXD Line Value is read and sent to the FSK Modulator. ST7538Q Manages the Transmission timing according to the BaudRate Selected
- Host Controller Asynchronous Communication Mode: TXD data enter directly to the FSK Modulator.The Host Controller Manages the Transmission timing

In both conditions no Protocol Bits are added by ST7538Q.

The FSK frequencies are synthesized in the FSK modulator from a 16MHz crystal oscillator by direct digital synthesis technique. The frequencies Table in different Configuration is reported in *Table 7*. The frequencies precision is same as external crystal one’s.
In the analog domain, the signal is filtered in order to reduce the output signal spectrum and to reduce the harmonic distortion. The transition between a symbol and the following is done at the end of the on-going half FSK sinewave cycle.

Figure 13. Transmitting path block diagram



5.8.1 Automatic Level Control (ALC)

The Automatic Level Control Block (ALC) is a variable gain amplifier (with 32 non linear discrete steps) controlled by two analog feed backs acting at the same time. The ALC gain range is 0dB to 30 dB and the gain change is clocked at 5KHz. Each step increases or reduces the voltage of 1dB (Typ).
Two are the control loops acting to define the ALC gain:

- **The Voltage control loop** acts to keep the Peak-to-Peak Voltage constant on Vsense. The gain adjustment is related to the result of a peak detection between the Voltage waveform on Vsense and two internal Voltage references. It is possible to protect the Voltage Control Loop against noise by freezing the output level (see *Section 6.6: Output voltage level freeze on page 38*).

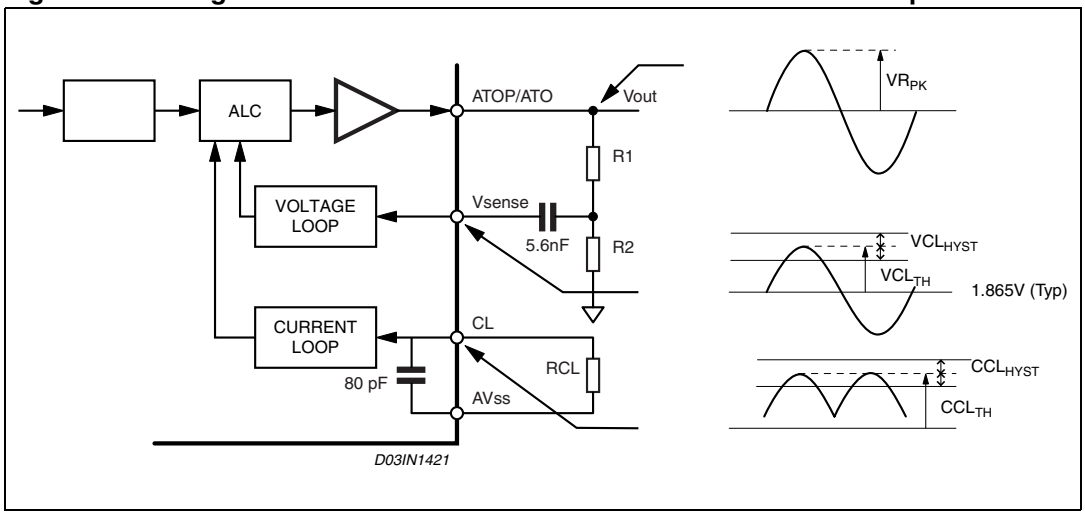
If Vsense < VCL_{TH} - VCL_{HYST} The next gain level is increased by 1 step
If VCL_{TH} - VCL_{HYST} < Vsense < VCL_{TH} + VCL_{HYST} No Gain Change
If Vsense > VCL_{TH} + VLC_{HYST} The next gain level is decreased by 1 step

- **The Current control loop** acts to limit the maximum Peak Output current inside ATOP1 and ATOP2.
  The current control loop acts through the voltage control loop decreasing the Output Peak-to-Peak Amplitude to reduce the Current inside the Power Line Interface.
  The current sensing is done by mirroring the current in the High side MOS of the Power Amplifier (not dissipating current Sensing). The Output Current Limit (up to 400mApeak), is set by means of an external resistor (R_{CL}) connected between CL and PAVss. The resistor converts the current sensed into a voltage signal. The Peak current sensing block works as the Output Voltage sensing Block:

If V(CL) < CCL_{TH} - CCL_{HYST} Voltage Control Loop Acting
If CCL_{TH} - CCL_{HYST} < V(CL) < CCL_{TH} + CCL_{HYST} No Gain Change
If V(CL) > CCL_{TH} + CLC_{HYST} The next gain level is decreased by 1 step

Figure 14 shows the typical connection of Current an Voltage control loops.

Figure 14. Voltage and current feedback external interconnection example



Voltage control loop formula

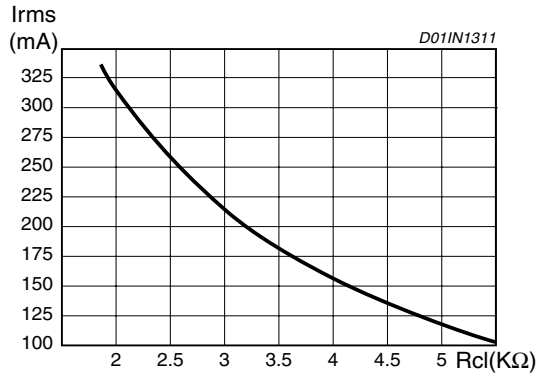
$$VR_{PK} \cong \frac{R_1 + R_2}{R_2} \cdot (VCL_{TH} \pm VCL_{HYST})$$

Table 10. Vout vs R1 & R2 resistors value

Vout (Vrms)	Vout (dBμV)	(R1+R2)/R2	R2 (KΩ)	R1 (KΩ)
0.150	103.5	1.1	7.5	1.0
0.250	108.0	1.9	5.1	3.9
0.350	110.9	2.7	3.6	5.6
0.500	114.0	3.7	3.3	8.2
0.625	115.9	4.7	3.3	11.0
0.750	117.5	5.8	2.7	12.0
0.875	118.8	6.6	2.0	11.0
1.000	120.0	7.6	1.6	10.0
1.250	121.9	9.5	1.6	13.0
1.500	123.5	10.8	1.6	15.0

Note: The rate of R2 takes in account the input resistance on the SENSE pin (36 KΩ). 5.6nF capacitor effect has been neglected.

Figure 15. Typical output current vs rcl



- **Integrated Power Line Interface (PLI)**
  The Power Line Interface (PLI) is a double CMOS AB Class Power Amplifier with the two outputs (ATOP1 and ATOP2) in opposition of phase.
  Two are the possible configuration:
  - Single Ended Output (ATOP1).
  - Bridge Connection
  The Bridge connection guarantee a Differential Output Voltage to the load with twice the swing of each individual Output. This topology virtually eliminates the even harmonics generation.
  The PLI requires, to ensure a proper operation, a regulated and well filtered Supply Voltage. PAVcc Voltage must fulfil the following formula to work without clipping phenomena:

$$PAVcc \geq \frac{VATOP(AC)}{2} + 7.5V$$

  To allow the driving of an external Power Line Interface, the output of the ALC is available even on ATO pin. ATO output has a current capability much lower than ATOP1 and ATOP2.

Figure 16. PLI bridge topology

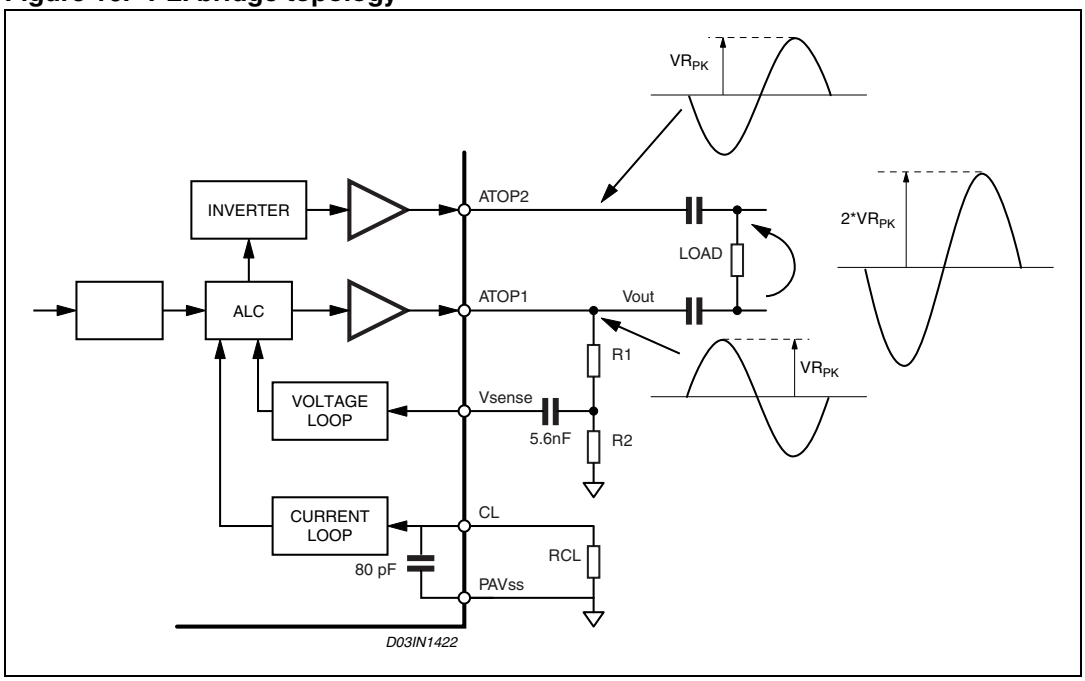
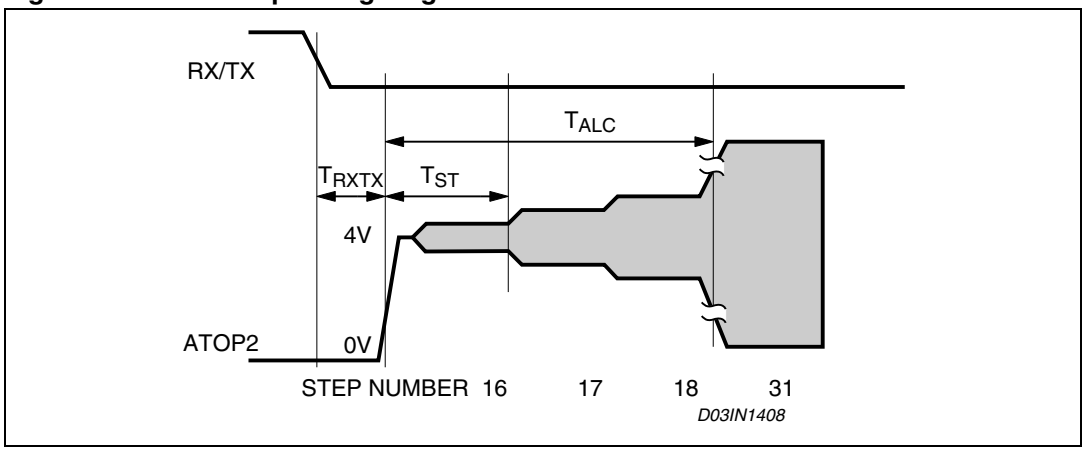


Figure 17. PLI startup timing diagram

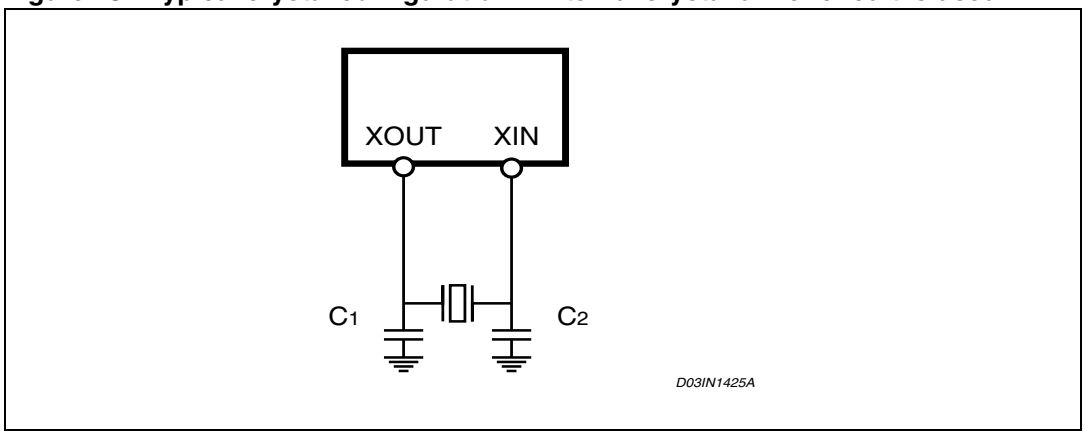


5.9 Crystal oscillator

ST7538Q integrates a inverter driver circuit to realize a 16MHz crystal oscillator.

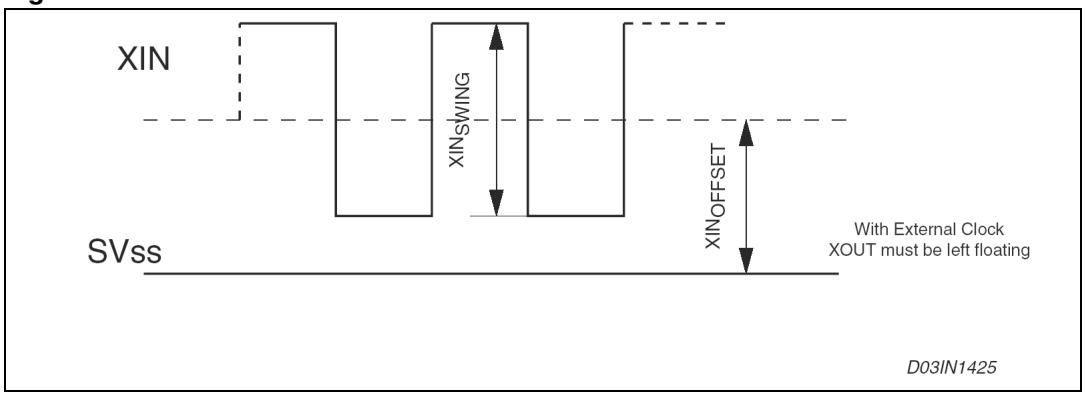
This circuit is able to drive a maximum load capacitance of 16pF with typical quartz ESR of 40Ω
If the internal driver circuit is used, only one external crystal quartz and two external load capacitors (C_1 and C_2) are needed to realize the oscillator function (*Figure 18*).

Figure 18. Typical crystal configuration if internal crystal driver circuit is used



If an external oscillator is used, XOUT must be disconnected, while XIN must satisfies the specifications given in *Table 4* (see *Figure 19*).

Figure 19. XIN waveform if an external oscillator is used



5.10 Control register

The ST7538Q is a multi-channel and multifunction transceiver. An internal 24 or 48 Bits (in Extended mode) Control Register allows to manage all the programmable parameters (*Table 11*).
The programmable functions are:

- Channel Frequency
- Baud Rate
- Deviation
- Watchdog
- Transmission Timeout
- Frequency Detection Time
- Detection Method
- Mains Interfacing Mode
- Output Clock
- Sensitivity Mode
- Input Pre-Filter

In addition to these functions the Extended mode provides 24 additional bits and others functions:

- Output Level Freeze
- Frame Header Recognizer (one 16 bits header of or two 8 bits headers) with support to Frame Length Bit count

Table 11. Control register functions

Bits	Function	Value	Selection			Note	Default
0 to 2	Frequencies	60 KHz 66 KHz 72 KHz 76 KHz 82.05 KHz 86 KHz 110 KHz 132.5 KHz	Bit2 0 0 0 0 1 1 1 1	Bit1 0 0 1 1 0 0 1 1	Bit0 0 1 0 1 0 1 0 1		132.5 kHz
3 to 4	Baud Rate	600 1,200 2,400 4,800	Bit 4 0 0 1 1	Bit 3 0 1 0 1			2400
5	Deviation	0.5 1	Bit 5 0 1				0.5
6	Watchdog	Disabled Enabled (1.5 s)	Bit 6 0 1				Enabled
7 to 8	Transmission Time Out	Disabled 1 s 3 s Not Used	Bit 8 0 0 1 1	Bit 7 0 1 0 1			1 sec
9 to 10	Frequency detection time	500 µs 1 ms 3 ms 5 ms	Bit 10 0 0 1 1	Bit 9 0 1 0 1			1 ms
11	Zero Crossing Synchronization	Disabled Enabled	Bit 11 0 1				Disabled

Table 11. Control register functions (continued)

	Function	Value	Selection		Note	Default
12 to 13	Detection Method(1)	Carrier detection without conditioning	Bit 13: 0	Bit 12: 0	Carrier Detection Notification on CD_PD Line CLR/T and RxD signal always Present	Preamble detection without conditioning
		Carrier detection with conditioning	0	1	CLR/T and RxD lines are forced to “0” when Carrier is not detected	
		Preamble detection without conditioning	1	0	Preamble Detection Notification on CD_PD Line CLR/T and RxD signal always Present	
		Preamble detection with conditioning	1	1	Preamble Detection Notification on CD_PD Line CLR/T and RxD lines are forced to “0” when Preamble has not been detected or PLL is in Unlock condition	
14	Mains Interfacing Mode	Synchronous Asynchronous	Bit 14: 0 1			Asynchronous
15 to 16	Output Clock	16 MHz 8 MHz 4 MHz Clock OFF	Bit 16: 0 0 1 1	Bit 15: 0 1 0 1		4 MHz
17	Output Voltage Level Freeze	Enabled Disabled	Bit 17: 0 1		Active only if Extended Control Register is enable (Bit 21=”1”)	Disabled
18	Header Recognition	Disabled Enabled	Bit 18: 0 1		Active only if Extended Control Register is enable (Bit 21=”1”)	Disabled
19	Frame Length Count	Disabled Enabled	Bit 19: 0 1		Active only if Header Recognition Function (Bit 18=”1”) and Extended Control Register (Bit 21=”1”) are enable	Disabled

Table 11. Control register functions (continued)

	Function	Value	Selection	Note	Default
20	Header Length	8 bits 16 bits	Bit 20 0 1	Active only if Extended Control Register is enable (Bit 21=”1”)	16 bits
21	Extended Register	Disable (24 bits) Enabled (48 bits)	Bit 21 0 1	Extended Register enables Functions on Bit 17, 18,19 and 20	Disabled (24 bits)
22	Sensitivity Mode	Normal Sensitivity High Sensitivity	Bit 22 0 1		Normal
23	Input Filter	Disabled Enabled	Bit 23 0 1		Disabled
24 to 39	Frame Header	from 0000h to FFFFh		One 16 bits Header or two 8 bits Headers (MSB first) depending on Bit 17	9B58h
40 to 47	Frame Length	from 01h to FFh		Number of 16 bits words expected	08h

1. The Detection method bit meaning differs depending on UART/SPI pin value. In this table is listed the SPI mode (UART/SPI=”0”). For Detection method bit meaning in UART mode (UART/SPI=”1”) please see *Table 12*.

5.11 Detection method and Rx Sensitivity in UART mode

When ST7538Q is running in UART mode (by forcing UART/SPI pin to “1”) the Control Register Function “Detection method” differs from SPI mode as indicated in the *Table 12*:

Table 12. Control register functions in UART mode

	Function	Value	Selection		Note	Default
			Bit 13	Bit 12		
12 to 13	Detection Method	Not Allowed	0	0	This configuration should be avoided because it could cause an unpredictable behavior of the device	Carrier detection without conditioning
		Not Allowed	0	1	This configuration should be avoided because it could cause an unpredictable behavior of the device	
		Carrier detection without conditioning	1	0	Carrier Detection Notification on CD_PD Line CLR/T and RxD signal always Present	
		Carrier detection with conditioning	1	1	Carrier Detection Notification on CD_PD Line CLR/T Line is forced to “0” and RxD Line is forced to “0” or “1” (according the UART/SPI pin level) when Carrier is not detected	

UART mode provides also a third level of Receiving sensitivity in addition to two levels select able by Control Register (see *Table 11*). By setting to “1” the TxD pin during a receiving session the sensitivity is forced to BU threshold (this condition suppresses the Control Register setting).

6 Auxiliary analog and digital functions

6.1 Band in use

The Band in Use Block has a Carrier Detection like function but with a different Input Sensibility (77dBµV Typ.)
and with a different BandPass filter Selectivity (40dB/Dec).

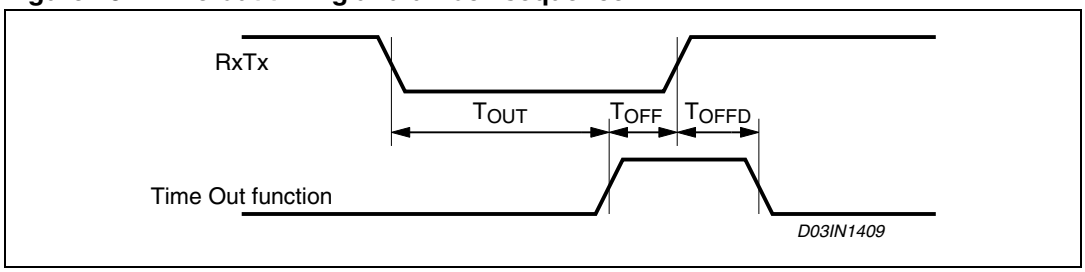
BU line is forced High when a signal in band is detected.
To prevent BU line false transition, BU signal is conditioned to Carrier Detection Internal Signal.

6.2 Time out

Time Out Function is a protection against a too long data transmission. When Time Out function is enabled after 1 or 3 second of continuos transmission the transceiver is forced in receiving mode. This function allows ST7538Q to automatically manage the CENELEC Medium Access specification. When a time-out event occur, TOUT is forced high, and is held high for at least 125 ms. To Unlock the Time Out condition RxTx should be forced High. During the time out period only register access or reception mode are enabled.

During Reset sequence if RxTx line =”0” & REG_DATA line =”0”, TIMEOUT protection is suddendly enabled and ST7538Q must be configured in data reception after the reset event before starting a new data transmission.
Time Out time is programmable using Control Register bits 7 and 8 (*Table 11*).

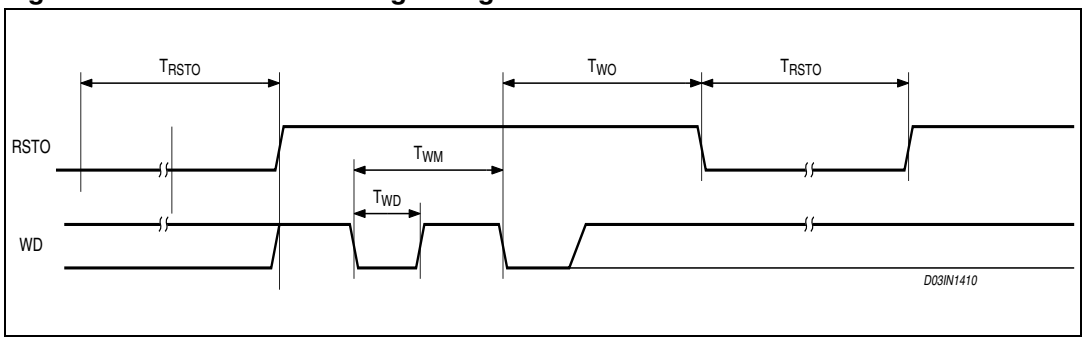
Figure 20. Time-out timing and unlock sequence



6.3 Reset & watchdog

RSTO Output is a reset generator for the application circuitry. During the ST7538Q startup sequence is forced low. RSTO becomes high after a T_{RSTO} delay from the end of oscillator startup sequence.
Inside ST7538Q is also embedded a watchdog function. The watchdog function is used to detect the occurrence of a software fault of the Host Controller. The watchdog circuitry generates an internal and external reset (RSTO low for T_{RSTO} time) on expiry of the internal watchdog timer. The watchdog timer reset can be achieved applying a negative pulse on WD pin (*Figure 21*).

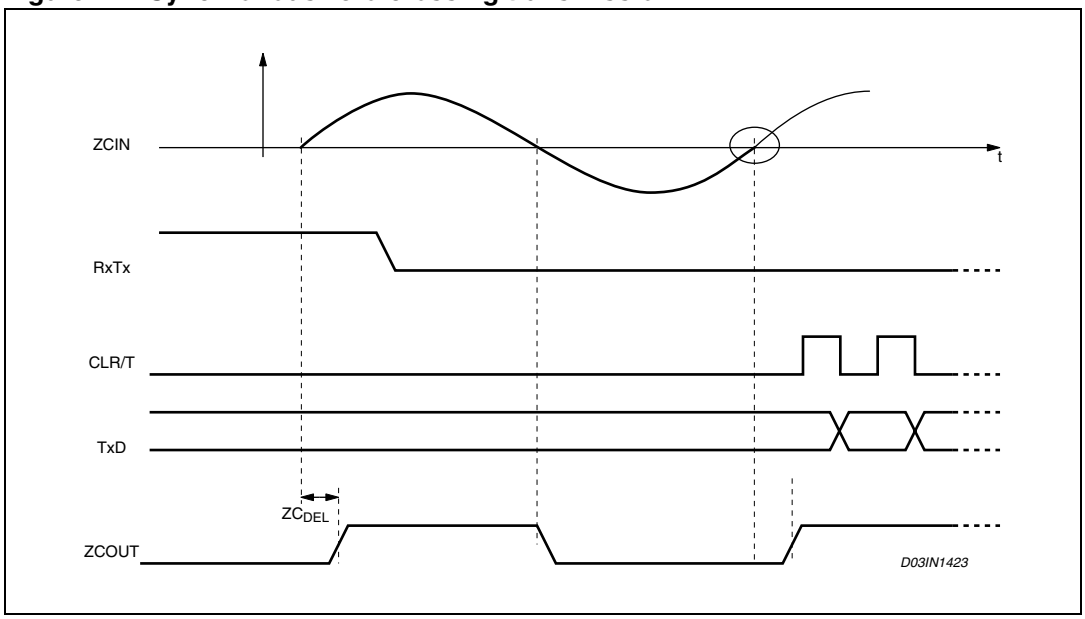
Figure 21. Reset and watchdog timing



6.4 Zero crossing detection

The Mains Voltage Zero Crossing can be detected, through a proper connection of ZCIN to the Mains. ZCIN comparator has a threshold fixed at SGND. ZCOUT is a TTL Output forced High after a positive zero-crossing transition, and low after a negative one.
Setting the Bit 11 inside the Control Register to “1” the transmission is automatically synchronized to the mains positive zero-crossing transition. This function is achieved turning on the PLI when RX/TX is low and delaying the CLR/T first transition until the first zero-crossing event. The automatic synchronization procedure can work only if the synchronous interface is programmed. If asynchronous interface is in use the Zero Crossing synchronization can be achieved managing the ZCOUT line.

Figure 22. Synchronous zero-crossing transmission



6.5 Output clock

MCLK is the master clock output. The clock frequency sourced can be programed through the control register to be a ratio of the crystal oscillator frequency (Fosc, Fosc/2 Fosc/4) or can be disabled (off). The transition between one frequency and another is done only at the end of the ongoing cycle.

6.6 Output voltage level freeze

The Output Level Freeze function, when enabled, turns off the Voltage Control Loop once the ALC stays in a stable condition for about 3 periods of control loop, and maintains a constant gain until the end of transmission. Output Level Freeze can be enabled using Control Register bit 17 (*Table 11*). This function is available only using the Extended Control Register (Control Register bit 21 = ”1”).

6.7 Extended control register

When Extended Control Register function is enabled, all the 48 bits of Control Register are programmable. Otherwise, only the first 24 bits of Control Register are programmable. The functions Header Recognition, Frame Bit Count and Output Voltage Freeze are available only if Extended Control Register function is enabled. Extended Control Register can be enabled setting the Control Register bit 21(*Table 11*).

6.8 Reg OK

REGOK allows to detect an incomplete writing of the Control Register content (see *Section 5.6: Control register access on page 21*) or an accidental corruption of the Control Register content. In these cases REGOK goes to “1” until a new Control Register writing session is performed.

6.9 Under voltage lock out

The UVLO function turns off the device if the PAVcc voltage falls under 4V. Hysteresis is 340mV typically.

6.10 Thermal shutdown

The ST7538Q is provided of a thermal protection which turn off the PLI when the junction temperature exceeds 170°C ± 10% . Hysteresis is around 30°C.

When shutdown threshold is overcome, PLI interface is switched OFF.

Thermal Shutdown event is notified to the HOST controller using TIMEOUT line. When TIMEOUT line is High, ST7538Q junction temperature exceed the shutdown threshold (Not Leached).

6.11 5V and 3.3V voltage regulators and power good function

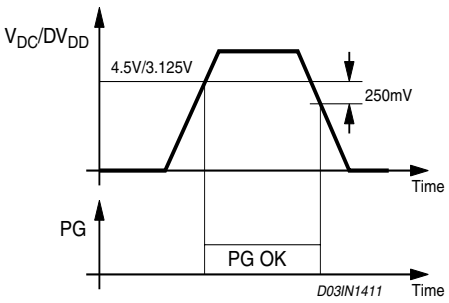
ST7538Q has an embedded 5V linear regulator externally available to supply the application circuitry.
The linear regulator has a very low quiescent current (50µA) and a current capability of 50mA. The regulator is protected against short circuitry events.

The DVdd pin can act either as 3.3V Voltage Output or as Input Digital Supply. When the DVdd pin is externally forced to 5V all the Digital I/Os operate at 5V, otherwise all the Digital I/Os are internally supplied at 3.3V. The DVdd pin can also source 3.3V voltage to supply external components. The 3.3V linear regulator has a very low quiescent current (50µA) and a current capability of 50mA. The regulator is protected against short circuitry events.

If AVdd and DVdd pins are connected to VDC pin, the 5V regulator maximum current capability rises to 100mA

When the regulator Voltages are above of the power good thresholds V_{PG} (see *Table 4*), Power Good line is forced high, while is forced low at startup and when VDC or DVdd falls below V_{PG} - V_{PGHYS} Voltage.

Figure 23. Power good function



6.12 Power-up procedure

To ensure ST7538Q proper power-Up sequence, PAVcc, AVdd and DVdd Supply has to fulfil the following rules:

PAVcc rising slope must not exceed 100V/ms.

When DVdd is below 5V/3.3V and AVdd is below 5V: 100mV < PAVcc-AVdd , PAVcc-DVdd < 1.2V.

When AVdd and DVdd supplies are connected to VDC the above mentioned relation is guarantied if VDC load < 100mA and if the filtering capacitor on VDC < 100uF.

If DVdd is not forced to 5V, the Digital I/Os are internally supplied at 3.3 V and if DVdd load < 50mA and the filtering capacitor on DVdd < 100uF the second relation can be ignored .

Figure 24. Power-UP sequence

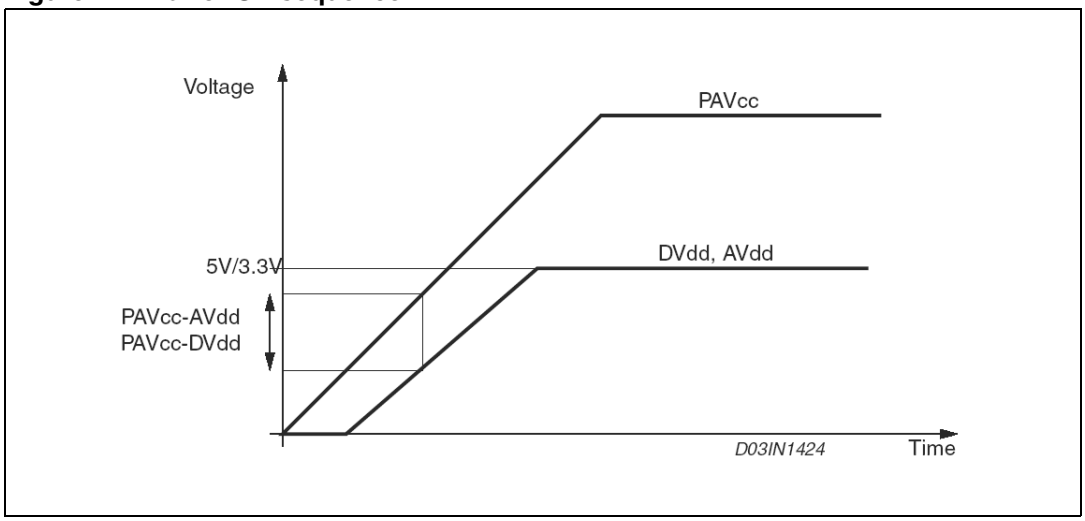
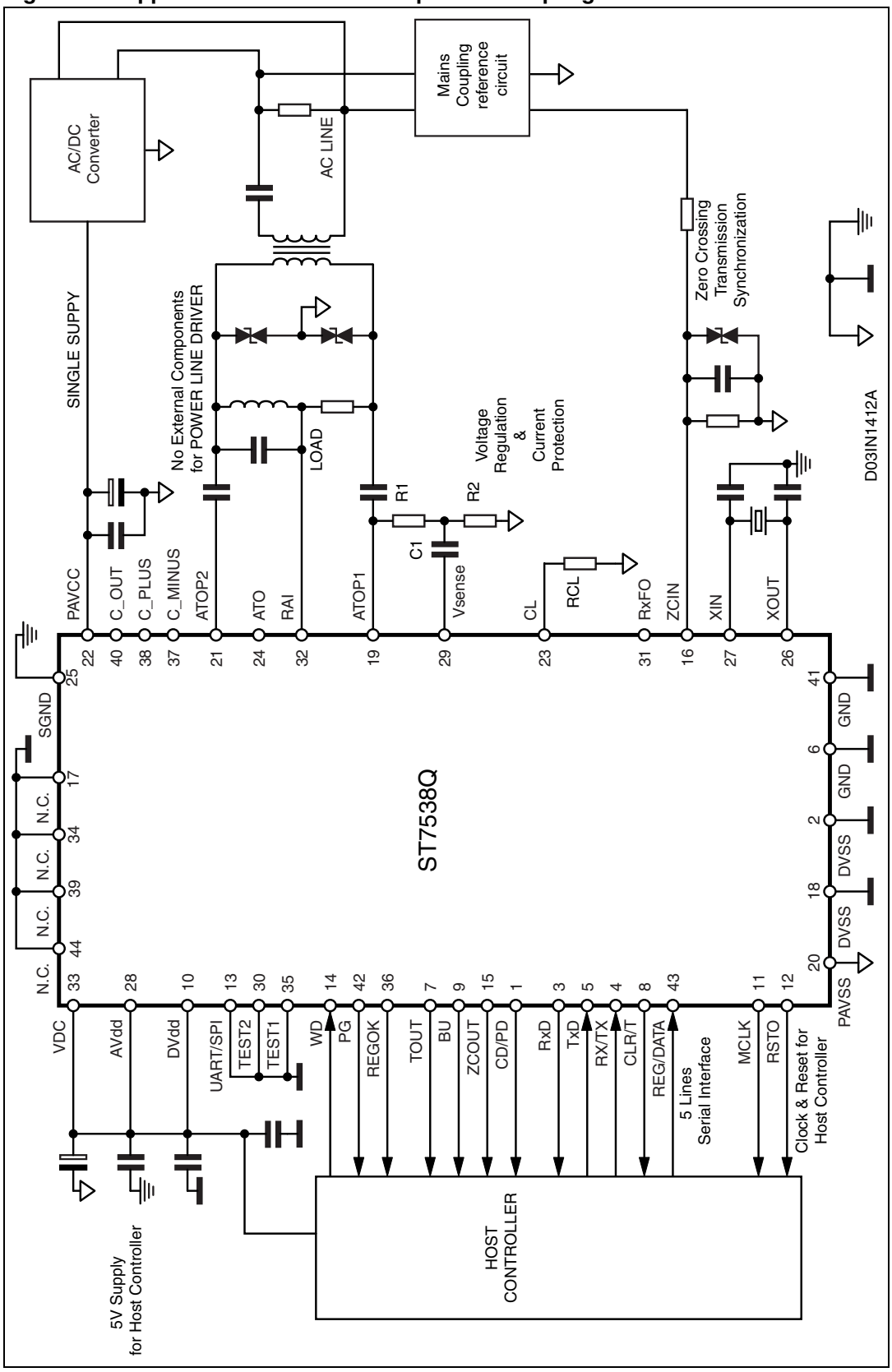


Figure 25. Application schematic example with coupling tranformer.



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Best thermal performance is achieved when slug is soldered to PCB.
It is recommended to have five solder dots (See *Figure 27*) without resist to connect the Copper slug to the ground layer on the soldering side. Moreover it is recommitted to connect the ground layer on the soldering side to another ground layer on the opposite side with 15 to 20 vias.

It is suggested to not use the PCB surface below the slug area to interconnect any pin except ground pins.

Figure 26. ST7538Q slug drawing

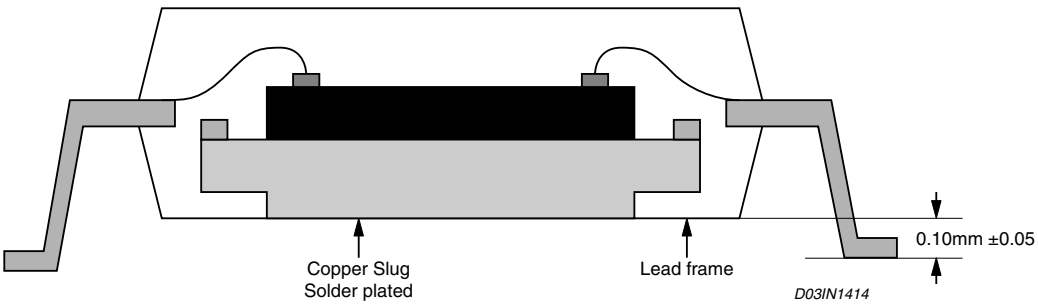
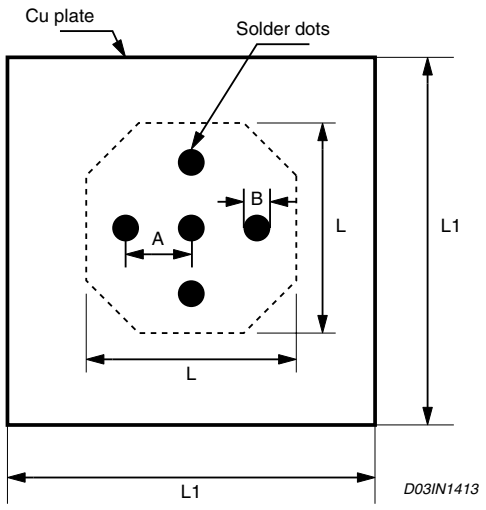


Figure 27. Soldering information



Package Sizes	10x10x1.4mm
A	2.00 mm
B	1.00 mm
L	6.00 mm
L1 (Copper plate)	10.00 mm

If PCB with ground layer, connect copper plate with 15 to 20 vias

8 Revision history

Table 13. Revision history

Date	Revision	Changes
12-Jul-2006	1	Initial release.

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