

## DM93L28 Dual 8-Bit Shift Register

### General Description

The DM93L28 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

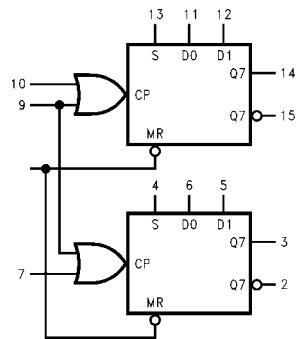
### Features

- 2-input multiplexer provided at data input of each register
- Gated clock input circuitry
- Both true and complementary outputs provided from last bit of each register
- Asynchronous master reset common to both registers

### Ordering Code:

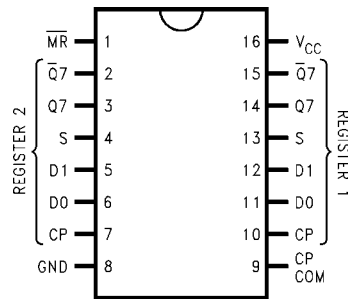
Order Number	Package Number	Package Description
DM93L28N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

### Logic Symbol



V<sub>CC</sub> = Pin 16      GND = Pin 8

### Connection Diagram



### Pin Descriptions

Pin Names	Description
S	Data Select Input
D0, D1	Data Inputs
CP	Clock Pulse Input (Active HIGH) Common (Pin 9) Separate (Pins 7 and 10)
$\overline{\text{MR}}$	Master Reset Input (Active LOW)
Q7	Last Stage Output
$\overline{\text{Q7}}$	Complementary Output

## Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a

logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

$$\text{Serial data in: } S_D = S D_0 + S D_1$$

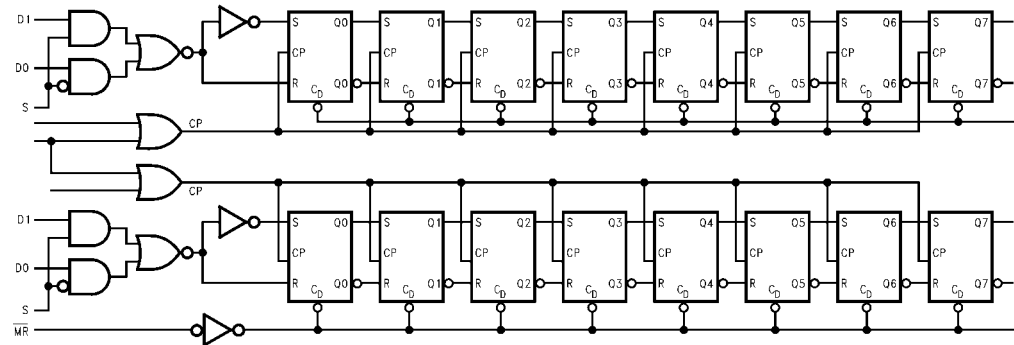
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

### Shift Select Table

Inputs			Output
S	D0	D1	Q7 (t <sub>n+8</sub> )
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 n+8 = Indicates state after eight clock pulse

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.7	V
I <sub>OH</sub>	HIGH Level Output Current			-400	μA
I <sub>OL</sub>	LOW Level Output Current			4.8	mA
T <sub>A</sub>	Free Air Operating Temperature	0		+7°	°C
t <sub>s</sub> (H)	Setup Time HIGH or LOW	30			ns
t <sub>s</sub> (L)	D <sub>n</sub> to CP	30			ns
t <sub>h</sub> (H)	Hold Time HIGH or LOW	0			ns
t <sub>h</sub> (L)	D <sub>n</sub> to CP	0			ns
t <sub>w</sub> (H)	Clock Pulse Width	55			ns
t <sub>w</sub> (L)	HIGH or LOW	55			ns
t <sub>w</sub> (L)	MR Pulse Width with CP HIGH	60			ns
t <sub>w</sub> (L)	MR Pulse Width with CP LOW	70			ns

**Electrical Characteristics**

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -10 mA		-1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min, V <sub>IL</sub> = Max		0.3	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V		1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V	MR, Dx	20	μA
			CP (7, 10)	30	
			S	40	
			CP Com	60	
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.3V	MR, Dx	-400	μA
			CP (7, 10)	-600	
			S	-800	
			CP Com	-1200	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	-2.5	-25	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max		25.3	mA

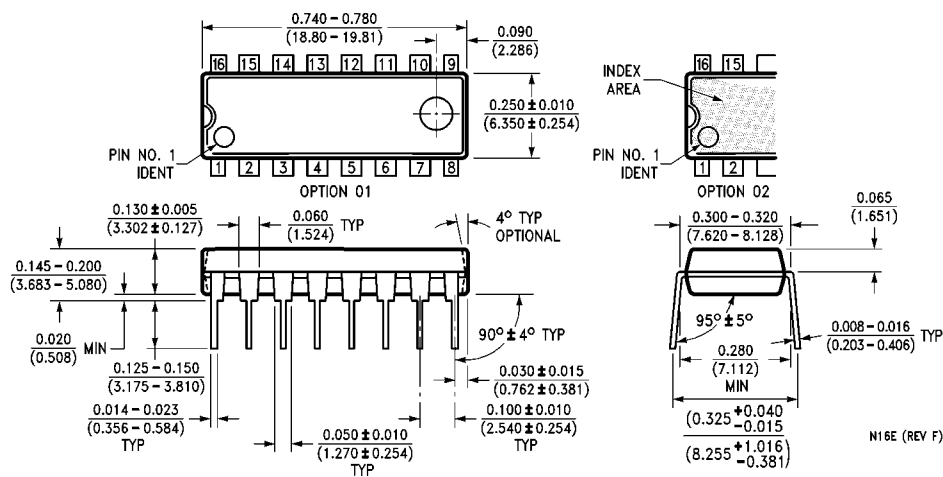
**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

$V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$

Symbol	Parameter	$C_L = 15 \text{ pF}$		Units
		Min	Max	
$f_{MAX}$	Maximum Shift Right Frequency	5.0		MHz
$t_{PLH}$	Propagation Delay		45	ns
$t_{PHL}$	CP to $Q_7$ or $\overline{Q}_7$		80	ns
$t_{PHL}$	Propagation Delay $\overline{MR}$ to $Q_7$		110	ns

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16EUnits**

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