# 32 Mbit Concurrent SuperFlash + 4/8 Mbit (P)SRAM ComboMemory
## SST34HF3242C / SST34HF3244C
## SST34HF3282 / SST34HF3284

***Advance Information***

## FEATURES:

- **Flash Organization: 2M x16 or 4M x8**
- **Dual-Bank Architecture for Concurrent Read/Write Operation**
  - 32 Mbit Top Sector Protection
  - SST34HF32x4x: 8 Mbit + 24Mbit
  - SST34HF32x2x: 4 Mbit + 28 Mbit
- **(P)SRAM Organization:**
  - 4 Mbit: 256K x16
  - 8 Mbit: 512K x16
- **Single 2.7-3.3V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 25 mA (typical)
  - Standby Current: 20 µA (typical)
- **Hardware Sector Protection (WP#)**
  - Protects 8 KWord in the smaller bank by holding WP# low and unprotects by holding WP# high
- **Hardware Reset Pin (RST#)**
  - Resets the internal state machine to reading data array
- **Byte Selection for Flash (CIOF pin)**
  - Selects 8-bit or 16-bit mode
- **Sector-Erase Capability**
  - Uniform 2 KWord sectors
- **Flash Chip-Erase Capability**
- **Block-Erase Capability**
  - Uniform 32 KWord blocks
- **Erase-Suspend / Erase-Resume Capabilities**
- **Read Access Time**
  - Flash: 70 ns
  - (P)SRAM: 70 ns
- **Security ID Feature**
  - SST: 128 bits
  - User: 256 bits
- **Latched Address and Data**
- **Fast Erase and Program (typical):**
  - Sector-Erase Time: 18 ms
  - Block-Erase Time: 18 ms
  - Chip-Erase Time: 35 ms
  - Program Time: 7 µs
- **Automatic Write Timing**
  - Internal $V_{PP}$ Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
  - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
  - 56-ball LFBGA (8mm x 10mm)
  - 62-ball LFBGA (8mm x 10mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

## PRODUCT DESCRIPTION

The SST34HF32x2xC/32x4x ComboMemory devices integrate either a 2M x16 or 4M x8 CMOS flash memory bank with either a 256K x16 or 512K x16 CMOS SRAM or pseudo SRAM (PSRAM) memory bank in a multi-chip package (MCP). These devices are fabricated using SST's proprietary, high-performance CMOS SuperFlash technology incorporating the split-gate cell design and thick-oxide tunneling injector to attain better reliability and manufacturability compared with alternate approaches. The SST34HF32x2xC/32x4x devices are ideal for applications such as cellular phones, GPS devices, PDAs, and other portable electronic devices in a low power and small form factor system.

The SST34HF32x2xC/32x4x feature dual flash memory bank architecture allowing for concurrent operations between the two flash memory banks and the (P)SRAM. The devices can read data from either bank while an Erase or Program operation is in progress in the opposite bank. The two flash memory banks are partitioned into 4 Mbit + 28 Mbit or 8 Mbit + 24 Mbit with top sector protection options for storing boot code, program code, configuration/parameter data and user data.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. The SST34HF32x2xC/32x4x devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years. With high-performance Program operations, the flash memory banks provide a typical Program time of 7 µsec. The entire flash memory bank can be erased and programmed word-by-word in typically 4 seconds for the SST34HF32x2xC/32x4x, when using interface features such as Toggle Bit, Data# Polling,

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or RY/BY# to indicate the completion of Program operation. To protect against inadvertent flash write, the SST34HF32x2xC/32x4x devices contain on-chip hardware and software data protection schemes.

The flash and (P)SRAM operate as two independent memory banks with respective bank enable signals. The memory bank selection is done by two bank enable signals. The (P)SRAM bank enable signals, BES1# and BES2, select the (P)SRAM bank. The flash memory bank enable signal, BEF#, has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The memory banks are superimposed in the same memory address space where they share common address lines, data lines, WE# and OE# which minimize power consumption and area.

Designed, manufactured, and tested for applications requiring low power and small form factor, the SST34HF32x2xC/32x4x are offered in both commercial and extended temperatures and a small footprint package to meet board space constraint requirements. See Figure 1 for pin assignments.

## Device Operation

The SST34HF32x2xC/32x4x uses BES1#, BES2 and BEF# to control operation of either the flash or the (P)SRAM memory bank. When BEF# is low, the flash bank is activated for Read, Program or Erase operation. When BES1# is low, and BES2 is high the (P)SRAM is activated for Read and Write operation. BEF# and BES1# cannot be at low level, and BES2 cannot be at high level at the same time. **If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage.** All address, data, and control lines are shared by flash and (P)SRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# and BES1# bank enables are raised to $V_{IHC}$ (Logic High) or when BEF# is high and BES2 is low.

## Concurrent Read/Write Operation

Dual bank architecture of SST34HF32x2xC/32x4x devices allows the Concurrent Read/Write operation whereby the user can read from one bank while programming or erasing in the other bank. This operation can be used when the user needs to read system code in one bank while updating data in the other bank. See Table 3 for dual-bank memory organization.

**CONCURRENT READ/WRITE STATES**

| Flash | | |
|---|---|---|
| **Bank 1** | **Bank 2** | **(P)SRAM** |
| Read | Write | No Operation |
| Write | Read | No Operation |
| Write | No Operation | Read |
| No Operation | Write | Read |
| Write | No Operation | Write |
| No Operation | Write | Write |

**Note:** For the purposes of this table, write means to perform Block-/Sector-Erase or Program operations as applicable to the appropriate bank.

## Flash Read Operation

The Read operation of the SST34HF32x2xC/32x4x is controlled by BEF# and OE#, both have to be low for the system to obtain data from the outputs. BEF# is used for device selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either BEF# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 6).

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## Flash Program Operation

These devices are programmed on a word-by-word or byte-by-byte basis depending on the state of the CIOF pin. Before programming, one must ensure that the sector being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Software Data Protection is initiated using the three-byte load sequence.
2. Address and data are loaded.

   During the Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first.
3. The internal Program operation is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed typically within 7 µs.

See Figures 7 and 8 for WE# and BEF# controlled Program operation timing diagrams and Figure 21 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.

## Flash Sector- /Block-Erase Operation

These devices offer both Sector-Erase and Block-Erase operations. These operations allow the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on a uniform sector size of 2 KWord. The Block-Erase mode is based on a uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. Any commands issued during the Block- or Sector-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 12 and 13 for timing waveforms.

## Flash Chip-Erase Operation

The SST34HF32x2xC/32x4x provide a Chip-Erase operation, which allows the user to erase all flash sectors/blocks to the “1” state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bits or Data# Polling. See Table 6 for the command sequence, Figure 11 for timing diagram, and Figure 25 for the flowchart. Any commands issued during the Chip-Erase operation are ignored. When WP# is low, any attempt to Chip-Erase will be ignored.

## Flash Erase-Suspend/-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode no more than 10 µs after the Erase-Suspend command had been issued. ($T_{ES}$ maximum latency equals 10 µs.) Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output $DQ_2$ toggling and $DQ_6$ at “1”. While in Erase-Suspend mode, a Program operation is allowed except for the sector or block selected for Erase-Suspend. To resume Sector-Erase or Block-Erase operation which has been suspended, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the one-byte sequence.

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## Flash Write Operation Status Detection

The SST34HF32x2xC/32x4x provide one hardware and two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) pin. The software detection includes two status bits: Data# Polling ($DQ_7$) and Toggle Bit ($DQ_6$). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), Data# Polling ($DQ_7$) or Toggle Bit ($DQ_6$) read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either $DQ_7$ or $DQ_6$. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

## Ready/Busy# (RY/BY#)

The SST34HF32x2xC/32x4x include a Ready/Busy# (RY/BY#) output signal. RY/BY# is an open drain output pin that indicates whether an Erase or Program operation is in progress. Since RY/BY# is an open drain output, it allows several devices to be tied in parallel to $V_{DD}$ via an external pull-up resistor. After the rising edge of the final WE# pulse in the command sequence, the RY/BY# status is valid. When RY/BY# is actively pulled low, it indicates that an Erase or Program operation is in progress. When RY/BY# is high (Ready), the devices may be read or left in standby mode.

## Byte/Word (CIOF)

The device includes a CIOF pin to control whether the device data I/O pins operate x8 or x16. If the CIOF pin is at logic “1” ($V_{IH}$) the device is in x16 data configuration: all data I/0 pins $DQ_0$-$DQ_{15}$ are active and controlled by BEF# and OE#.

If the CIOF pin is at logic “0”, the device is in x8 data configuration: only data I/O pins $DQ_0$-$DQ_7$ are active and controlled by BEF# and OE#. The remaining data pins $DQ_8$-$DQ_{14}$ are at Hi-Z, while pin $DQ_{15}$ is used as the address input $A_{-1}$ for the Least Significant Bit of the address bus.

## Flash Data# Polling ($DQ_7$)

When the devices are in an internal Program operation, any attempt to read $DQ_7$ will produce the complement of the true data. Once the Program operation is completed, $DQ_7$ will produce true data. During internal Erase operation, any attempt to read $DQ_7$ will produce a ‘0’. Once the internal Erase operation is completed, $DQ_7$ will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or BEF#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or BEF#) pulse. See Figure 9 for Data# Polling ($DQ_7$) timing diagram and Figure 22 for a flowchart.

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## Toggle Bits ($DQ_6$ and $DQ_2$)

During the internal Program or Erase operation, any consecutive attempts to read $DQ_6$ will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the $DQ_6$ bit will stop toggling. The device is then ready for the next operation. The toggle bit is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operations. For Sector-, Block-, or Chip-Erase, the toggle bit ($DQ_6$) is valid after the rising edge of sixth WE# (or BEF#) pulse. $DQ_6$ will be set to "1" if a Read operation is attempted on an Erase-suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, $DQ_6$ will toggle.

An additional Toggle Bit is available on $DQ_2$, which can be used in conjunction with $DQ_6$ to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bit information. The Toggle Bit ($DQ_2$) is valid after the rising edge of the last WE# (or BEF#) pulse of a Write operation. See Figure 10 for Toggle Bit timing diagram and Figure 22 for a flowchart.

**TABLE 1: WRITE OPERATION STATUS**

| Status | | $DQ_7$ | $DQ_6$ | $DQ_2$ | RY/BY# |
|---|---|---|---|---|---|
| Normal Operation | Standard Program | DQ7# | Toggle | No Toggle | 0 |
| | Standard Erase | 0 | Toggle | Toggle | 0 |
| Erase-Suspend Mode | Read From Erase Suspended Sector/Block | 1 | 1 | Toggle | 1 |
| | Read From Non-Erase Suspended Sector/Block | Data | Data | Data | 1 |
| | Program | DQ7# | Toggle | No Toggle | 0 |

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**Note:** $DQ_7$, $DQ_6$, and $DQ_2$ require a valid address when reading status information. The address must be in the bank where the operation is in progress in order to read the operation status. If the address is pointing to a different bank (not busy), the device will output array data.

## Data Protection

The SST34HF32x2xC/32x4x provide both hardware and software features to protect nonvolatile data from inadvertent writes.

## Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

## Hardware Block Protection

The SST34HF32x2xC/32x4x provide a hardware block protection which protects the outermost 8 KWord/16 KByte in Bank 1. The block is protected when WP# is held low. When WP# is held low and a Block-Erase command is issued to the protected block, the data in the outermost 8 KWord/16 KByte section will be protected. The rest of the block will be erased. See Table 3 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

## Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least $T_{RP}$, any in-progress operation will terminate and return to Read mode (see Figure 18). When no internal Program/Erase operation is in progress, a minimum period of $T_{RHR}$ is required after RST# is driven high before a valid Read can take place (see Figure 17).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity. See Figures 17 and 18 for timing diagrams.

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## Software Data Protection (SDP)

The SST34HF32x2xC/32x4x provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HF32x2xC/32x4x are shipped with the Software Data Protection permanently enabled. See Table 6 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within $T_{RC.}$ The contents of $DQ_{15}$-$DQ_8$ are "Don't Care" during any SDP command sequence.

## Common Flash Memory Interface (CFI)

These devices also contain the CFI information to describe the characteristics of the devices. In order to enter the CFI Query mode, the system must write the three-byte sequence, same as the Software ID Entry command with 98H (CFI Query command) to address $BK_X$555H in the last byte sequence. In order to enter the CFI Query mode, the system can also use the one-byte sequence with $BK_X$55H on Address and 98H on Data Bus. See Figure 15 for CFI Entry and Read timing diagram. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 7 through 9. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

## Security ID

The SST34HF32x2xC/32x4x devices offer a 136-bit Security ID space. The Secure ID space is divided into two segments—one 128-bit factory programmed segment and one 128-word (256-byte) user-programmed segment. The first segment is programmed and locked at SST with a unique, 128-bit number. The user segment is left un-programmed for the customer to program as desired.

To program the user segment of the Security ID, the user must use the Security ID Program command. End-of-Write status is checked by reading the toggle bits. Data# Polling is not used for Security ID End-of-Write detection. Once programming is complete, the Sec ID should be locked using the User-Sec-ID-Program-Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased. The Secure ID space can be queried by executing a three-byte command sequence with Query-Sec-ID command (88H) at address 555H in the last byte sequence. To exit this mode, the Exit-Sec-ID command should be executed. Refer to Table 6 for more details.

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## Product Identification

The Product Identification mode identifies the device as either SST34HF32x2x or SST34HF32x4x and manufacturer as SST. This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers cannot be used on this device because of the shared lines between flash and (P)SRAM in the multi-chip package. Therefore, application of high voltage to pin $A_9$ may damage this device. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 5 and 6 for software operation, Figure 14 for the Software ID Entry and Read timing diagram and Figure 23 for the ID Entry command sequence flowchart.

**TABLE 2: PRODUCT IDENTIFICATION**

| | ADDRESS | DATA |
|---|---|---|
| Manufacturer's ID | BK0000H | 00BFH |
| Device ID | | |
| SST34HF3242C/3282 | BK0001H | 7351H |
| SST34HF3244C/3284 | BK0001H | 7353H |

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**Note:** BK = Bank Address ($A_{20}$-$A_{18}$)

## Product Identification Mode Exit/ CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 6 for software command codes, Figure 16 for timing waveform and Figure 23 for a flowchart.

## (P)SRAM Operation

With BES1# low, BES2 and BEF# high, the SST34HF32x2xC/32x4x operate as either 256K x16 or 512K x16 CMOS (P)SRAM, with fully static operation requiring no external clocks or timing strobes. The SST34HF32x2xC/32x4x (P)SRAM is mapped into the first 512 KWord address space. When BES1#, BEF# are high and BES2 is low, all memory banks are deselected and the device enters standby. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte. See Table 5 for x16 (P)SRAM Read and Write data byte control modes of operation.

## (P)SRAM Read

The (P)SRAM Read operation of the SST34HF32x2xC/ 32x4x is controlled by OE# and BES1#, both have to be low with WE# and BES2 high for the system to obtain data from the outputs. BES1# and BES2 are used for (P)SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 3, for further details.

## (P)SRAM Write

The (P)SRAM Write operation of the SST34HF32x2xC/ 32x4x is controlled by WE# and BES1#, both have to be low, BES2 must be high for the system to write to the (P)SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES1#, WE#, or the falling edge of BES2 whichever occurs first. The write time is measured from the last falling edge of BES#1 or WE# or the rising edge of BES2 to the first rising edge of BES1#, or WE# or the falling edge of BES2. Refer to the Write cycle timing diagrams, Figures 4 and 5, for further details.

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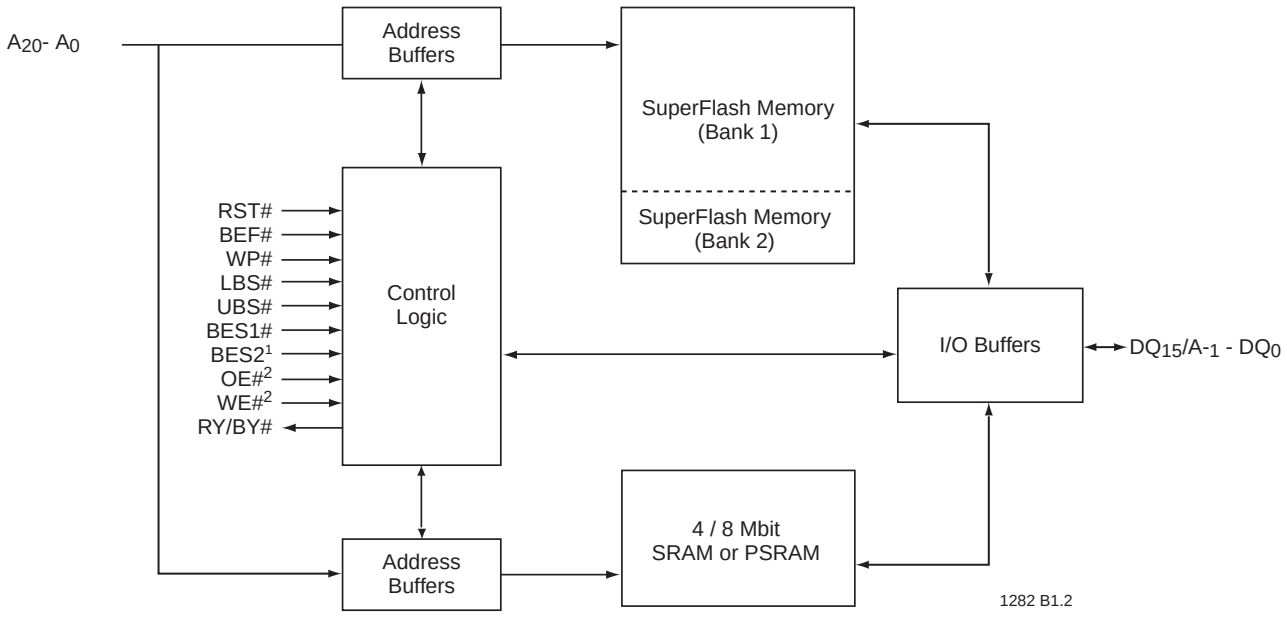
## FUNCTIONAL BLOCK DIAGRAM




Notes: 1. BES2 applies only to the SST34HF32x2x/32x4x devices
2. For LS package only: WE# = WEF# and/or WES#
OE# = OEF# and/or OES#

**TABLE 3: DUAL-BANK MEMORY ORGANIZATION (1 OF 2)**

| SST34HF3242C/3282 | SST34HF3244C/3284 | Block | Block Size | Address Range x8 | Address Range x16 |
|---|---|---|---|---|---|
| Bank 1 | Bank 1 | BA63 | 8 KW / 16 KB | 3FC000H–3FFFFFH | 1FE000H–1FFFFFH |
| | | | 24 KW / 48 KB | 3F0000H–3FBFFFH | 1F8000H–1FDFFFH |
| | | BA62 | 32 KW / 64 KB | 3E0000H–3EFFFFH | 1F0000H–1F7FFFH |
| | | BA61 | 32 KW / 64 KB | 3D0000H–3DFFFFH | 1E8000H–1EFFFFH |
| | | BA60 | 32 KW / 64 KB | 3C0000H–3CFFFFH | 1E0000H–1E7FFFH |
| | | BA59 | 32 KW / 64 KB | 3B0000H–3BFFFFH | 1D8000H–1DFFFFH |
| | | BA58 | 32 KW / 64 KB | 3A0000H–3AFFFFH | 1D0000H–1D7FFFH |
| | | BA57 | 32 KW / 64 KB | 390000H–39FFFFH | 1C8000H–1CFFFFH |
| | | BA56 | 32 KW / 64 KB | 380000H–38FFFFH | 1C0000H–1C7FFFH |
| Bank 2 | | BA55 | 32 KW / 64 KB | 370000H–37FFFFH | 1B8000H–1BFFFFH |
| | | BA54 | 32 KW / 64 KB | 360000H–36FFFFH | 1B0000H–1B7FFFH |
| | | BA53 | 32 KW / 64 KB | 350000H–35FFFFH | 1A8000H–1AFFFFH |
| | | BA52 | 32 KW / 64 KB | 340000H–34FFFFH | 1A0000H–1A7FFFH |
| | | BA51 | 32 KW / 64 KB | 330000H–33FFFFH | 198000H–19FFFFH |
| | | BA50 | 32 KW / 64 KB | 320000H–32FFFFH | 190000H–197FFFH |
| | | BA49 | 32 KW / 64 KB | 310000H–31FFFFH | 188000H–18FFFFH |
| | | BA48 | 32 KW / 64 KB | 300000H–30FFFFH | 180000H–187FFFH |
| | Bank 2 | BA47 | 32 KW / 64 KB | 2F0000H–2FFFFFH | 178000H–17FFFFH |
| | | BA46 | 32 KW / 64 KB | 2E0000H–2EFFFFH | 170000H–177FFFH |
| | | BA45 | 32 KW / 64 KB | 2D0000H–2DFFFFH | 168000H–16FFFFH |
| | | BA44 | 32 KW / 64 KB | 2C0000H–2CFFFFH | 160000H–167FFFH |
| | | BA43 | 32 KW / 64 KB | 2B0000H–2BFFFFH | 158000H–15FFFFH |
| | | BA42 | 32 KW / 64 KB | 2A0000H—2AFFFFH | 150000H–157FFFH |
| | | BA41 | 32 KW / 64 KB | 290000H—29FFFFH | 148000H–14FFFFH |
| | | BA40 | 32 KW / 64 KB | 280000H—28FFFFH | 140000H–147FFFH |
| | | BA39 | 32 KW / 64 KB | 270000H—27FFFFH | 138000H–13FFFFH |
| | | BA38 | 32 KW / 64 KB | 260000H—26FFFFH | 130000H–137FFFH |
| | | BA37 | 32 KW / 64 KB | 250000H—25FFFFH | 128000H–12FFFFH |
| | | BA36 | 32 KW / 64 KB | 240000H—24FFFFH | 120000H–127FFFH |
| | | BA35 | 32 KW / 64 KB | 230000H—23FFFFH | 118000H–11FFFFH |
| | | BA34 | 32 KW / 64 KB | 220000H—22FFFFH | 110000H–117FFFH |
| | | BA33 | 32 KW / 64 KB | 210000H—21FFFFH | 108000H–10FFFFH |
| | | BA32 | 32 KW / 64 KB | 200000H—20FFFFH | 100000H–107FFFH |
| | | BA31 | 32 KW / 64 KB | 1F0000H—1FFFFFH | 0F8000H–0FFFFFH |
| | | BA30 | 32 KW / 64 KB | 1E0000H—1EFFFFH | 0F0000H–0F7FFFH |
| | | BA29 | 32 KW / 64 KB | 1D0000H—1DFFFFH | 0E8000H–0EFFFFH |
| | | BA28 | 32 KW / 64 KB | 1C0000H—1CFFFFH | 0E0000H–0E7FFFH |
| | | BA27 | 32 KW / 64 KB | 1B0000H—1BFFFFH | 0D8000H–0DFFFFH |
| | | BA26 | 32 KW / 64 KB | 1A0000H—1AFFFFH | 0D0000H–0D7FFFH |
| | | BA25 | 32 KW / 64 KB | 190000H—19FFFFH | 0C8000H–0CFFFFH |
| | | BA24 | 32 KW / 64 KB | 180000H—18FFFFH | 0C0000H–0C7FFFH |
| | | BA23 | 32 KW / 64 KB | 170000H—17FFFFH | 0B8000H–0BFFFFH |
| | | BA22 | 32 KW / 64 KB | 160000H—16FFFFH | 0B0000H–0B7FFFH |

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**TABLE 3: DUAL-BANK MEMORY ORGANIZATION (CONTINUED) (2 OF 2)**

| SST34HF3242C/3282 | SST34HF3244C/3284 | Block | Block Size | Address Range x8 | Address Range x16 |
|---|---|---|---|---|---|
| Bank 2 | Bank 2 | BA21 | 32 KW / 64 KB | 150000H—15FFFFH | 0A8000H–0AFFFFH |
| | | BA20 | 32 KW / 64 KB | 140000H—14FFFFH | 0A0000H–0A7FFFH |
| | | BA19 | 32 KW / 64 KB | 130000H—13FFFFH | 098000H–09FFFFH |
| | | BA18 | 32 KW / 64 KB | 120000H—12FFFFH | 090000H–097FFFH |
| | | BA17 | 32 KW / 64 KB | 110000H—11FFFFH | 088000H–08FFFFH |
| | | BA16 | 32 KW / 64 KB | 100000H—10FFFFH | 080000H–087FFFH |
| | | BA15 | 32 KW / 64 KB | 0F0000H—0FFFFFH | 078000H–07FFFFH |
| | | BA14 | 32 KW / 64 KB | 0E0000H—0EFFFFH | 070000H–077FFFH |
| | | BA13 | 32 KW / 64 KB | 0D0000H—0DFFFFH | 068000H–06FFFFH |
| | | BA12 | 32 KW / 64 KB | 0C0000H—0CFFFFH | 060000H–067FFFH |
| | | BA11 | 32 KW / 64 KB | 0B0000H—0BFFFFH | 058000H–05FFFFH |
| | | BA10 | 32 KW / 64 KB | 0A0000H—0AFFFFH | 050000H–057FFFH |
| | | BA9 | 32 KW / 64 KB | 090000H—09FFFFH | 048000H–04FFFFH |
| | | BA8 | 32 KW / 64 KB | 080000H—08FFFFH | 040000H–047FFFH |
| | | BA7 | 32 KW / 64 KB | 070000H—07FFFFH | 038000H–03FFFFH |
| | | BA6 | 32 KW / 64 KB | 060000H—06FFFFH | 030000H–037FFFH |
| | | BA5 | 32 KW / 64 KB | 050000H–05FFFFH | 028000H–02FFFFH |
| | | BA4 | 32 KW / 64 KB | 040000H–04FFFFH | 020000H–027FFFH |
| | | BA3 | 32 KW / 64 KB | 030000H–03FFFFH | 018000H–01FFFFH |
| | | BA2 | 32 KW / 64 KB | 020000H–02FFFFH | 010000H–017FFFH |
| | | BA1 | 32 KW / 64 KB | 010000H–01FFFFH | 008000H–00FFFFH |
| | | BA0 | 32 KW / 64 KB | 000000H–00FFFFH | 000000H–007FFFH |

T3.0 1282

## PIN DESCRIPTION

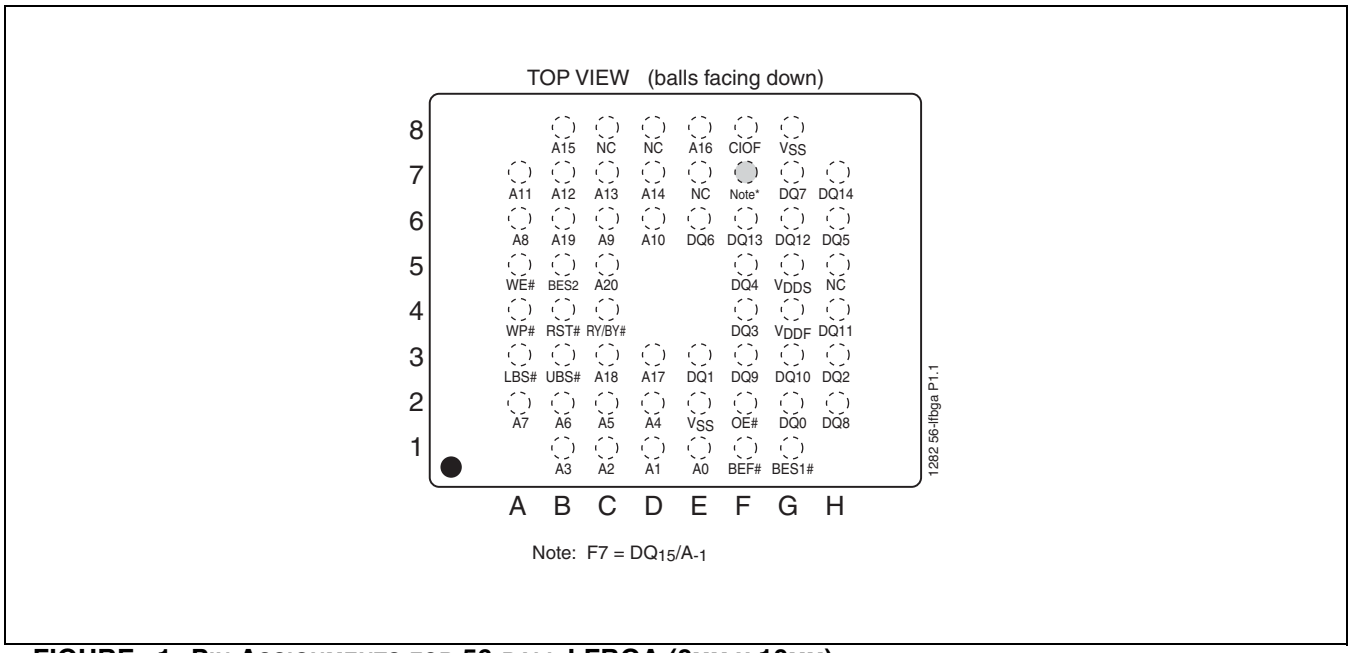


**FIGURE 1: PIN ASSIGNMENTS FOR 56-BALL LFBGA (8MM X 10MM)**

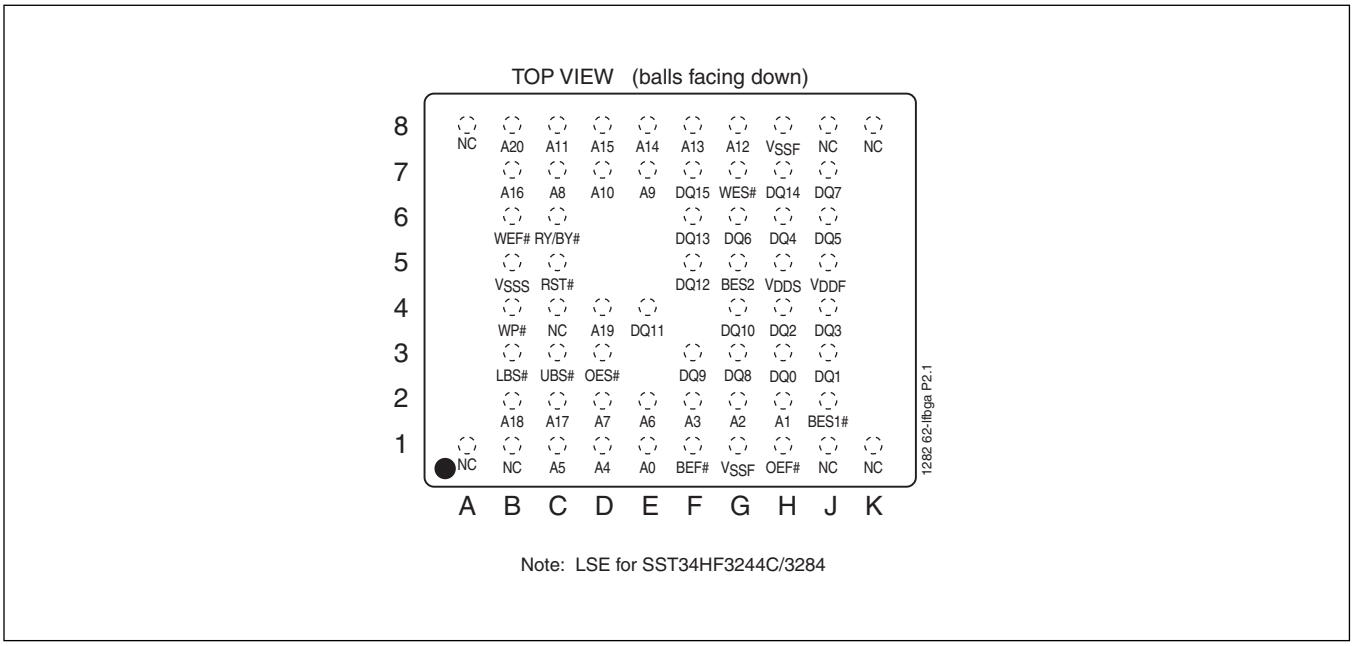


**FIGURE 2: PIN ASSIGNMENTS FOR 62-BALL LFBGA (8MM X 10MM)**

Advance Information

**TABLE 4: PIN DESCRIPTION**

| Symbol | Pin Name | Functions |
|---|---|---|
| $A_{MS}$[1] to $A_0$ | Address Inputs | To provide flash address, $A_{20}$-$A_0$.<br>To provide (P)SRAM address, $A_{MSS}$-$A_0$ |
| $DQ_{14}$-$DQ_0$ | Data Inputs/Outputs | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# is high or BES1# is high or BES2 is low and BEF# is high. |
| $DQ_{15}/A_{-1}$ | Data Input/Output and LBS Address | $DQ_{15}$ is used as data I/O pin when in x16 mode (CIOF = "1")<br>$A_{-1}$ is used as the LBS address pin when in x8 mode (CIOF = "0") |
| BEF# | Flash Memory Bank Enable | To activate the Flash memory bank when BEF# is low |
| BES1# | (P)SRAM Memory Bank Enable | To activate the (P)SRAM memory bank when BES1# is low |
| BES2 | (P)SRAM Memory Bank Enable | To activate the (P)SRAM memory bank when BES2 is high |
| OEF#[2] | Output Enable | To gate the data output buffers for Flash[2] only |
| OES#[2] | Output Enable | To gate the data output buffers for SRAM[2] only |
| WEF#[2] | Write Enable | To control the Write operations for Flash[2] only |
| WES#[2] | Write Enable | To control the Write operations for SRAM[2] only |
| OE# | Output Enable | To gate the data output buffers |
| WE# | Write Enable | To control the Write operations |
| CIOF | Byte Selection for Flash | When low, select Byte mode. When high, select Word mode. |
| UBS# | Upper Byte Control ((P)SRAM) | To enable $DQ_{15}$-$DQ_8$ |
| LBS# | Lower Byte Control ((P)SRAM) | To enable $DQ_7$-$DQ_0$ |
| WP# | Write Protect | To protect and unprotect the bottom 8 KWord (4 sectors) from Erase or Program operation |
| RST# | Reset | To Reset and return the device to Read mode |
| RY/BY# | Ready/Busy# | To output the status of a Program or Erase Operation<br>RY/BY# is a open drain output, so a 10KΩ - 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read. |
| $V_{SSF}$[2] | Ground | Flash[2] only |
| $V_{SSS}$[2] | Ground | SRAM[2] only |
| $V_{SS}$ | Ground | |
| $V_{DDF}$ | Power Supply (Flash) | 2.7-3.3V Power Supply to Flash only |
| $V_{DDS}$ | Power Supply ((P)SRAM) | 2.7-3.3V Power Supply to (P)SRAM only |
| NC | No Connection | Unconnected pins |

T4.0 1282

1. $A_{MSS}$ = Most Significant Address
   $A_{MSS}$ = $A_{17}$ for SST34HF324xC and $A_{18}$ for SST34HF328x
2. LSE package only

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**TABLE 5: OPERATIONAL MODES SELECTION FOR X16 (P)SRAM**

| Mode | BEF#[1] | BES1#[1,2] | BES2[1,2] | OE#[2,3] | WE#[2,3] | LBS#[2] | UBS#[2] | $DQ_{7-0}$ | $DQ_{15-8}$ CIOF = $V_{IH}$ | $DQ_{15-8}$ CIOF = $V_{IL}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Full Standby | $V_{IH}$ | $V_{IH}$ | X | X | X | X | X | HIGH-Z | HIGH-Z | HIGH-Z |
| | | X | $V_{IL}$ | X | X | X | X | | | |
| Output Disable | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | X | HIGH-Z | HIGH-Z | HIGH-Z |
| | | $V_{IL}$ | $V_{IH}$ | X | X | $V_{IH}$ | $V_{IH}$ | | | |
| | $V_{IL}$ | $V_{IH}$ | X | $V_{IH}$ | $V_{IH}$ | X | X | HIGH-Z | HIGH-Z | HIGH-Z |
| | | X | $V_{IL}$ | | | | | | | |
| Flash Read | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | $V_{IH}$ | X | X | $D_{OUT}$ | $D_{OUT}$ | $DQ_{14-8}$ = HIGH-Z<br>$DQ_{15} = A_{-1}$ |
| | | X | $V_{IL}$ | | | | | | | |
| Flash Write | $V_{IL}$ | $V_{IH}$ | X | $V_{IH}$ | $V_{IL}$ | X | X | $D_{IN}$ | $D_{IN}$ | $DQ_{14-8}$ = HIGH-Z<br>$DQ_{15} = A_{-1}$ |
| | | X | $V_{IL}$ | | | | | | | |
| Flash Erase | $V_{IL}$ | $V_{IH}$ | X | $V_{IH}$ | $V_{IL}$ | X | X | X | X | X |
| | | X | $V_{IL}$ | | | | | | | |
| (P)SRAM Read | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $D_{OUT}$ | $D_{OUT}$ | $D_{OUT}$ |
| | | | | | | $V_{IH}$ | $V_{IL}$ | HIGH-Z | $D_{OUT}$ | $D_{OUT}$ |
| | | | | | | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | HIGH-Z | HIGH-Z |
| (P)SRAM Write | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $D_{IN}$ | $D_{IN}$ | $D_{IN}$ |
| | | | | | | $V_{IH}$ | $V_{IL}$ | HIGH-Z | $D_{IN}$ | $D_{IN}$ |
| | | | | | | $V_{IL}$ | $V_{IH}$ | $D_{IN}$ | HIGH-Z | HIGH-Z |
| Product Identification[4] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | Manufacturer's ID[5]<br>Device ID[5] | | |

T5.1 1282

1. Do not apply BEF# = $V_{IL}$, BES1# = $V_{IL}$ and BES2 = $V_{IH}$ at the same time
2. X can be $V_{IL}$ or $V_{IH}$, but no other value.
3. OE# = OEF# and OES#
   WE# = WEF# and WES# for LSE package only
4. Software mode only
5. With $A_{19}$-$A_{18}$ = $V_{IL}$; SST Manufacturer's ID = BFH, is read with $A_0$=0,
   SST34HF32x2x Device ID = 7351H, is read with $A_0$=1
   SST34HF32x4x Device ID = 7353H, is read with $A_0$=1

Advance Information

**TABLE 6: SOFTWARE COMMAND SEQUENCE**

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] | Addr[1] | Data[2] |
| Word-Program | 555H | AAH | 2AAH | 55H | 555H | A0H | WA[3] | Data | | | | |
| Sector-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | $SA_X$[4] | 50H |
| Block-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | $BA_X$[4] | 30H |
| Chip-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| Erase-Suspend | XXXXH | B0H | | | | | | | | | | |
| Erase-Resume | XXXXH | 30H | | | | | | | | | | |
| Query Sec ID[5] | 555H | AAH | 2AAH | 55H | 555H | 88H | | | | | | |
| User-Security-ID-Program | 555H | AAH | 2AAH | 55H | 555H | A5H | SIWA[6] | Data | | | | |
| User-Security-ID-Program-Lock-out[7] | 555H | AAH | 2AAH | 55H | 555H | 85H | XXH | 0000H | | | | |
| Software ID Entry[8] | 555H | AAH | 2AAH | 55H | $BK_X$[9] 555H | 90H | | | | | | |
| CFI Query Entry | 555H | AAH | 2AAH | 55H | $BK_X$[4] 555H | 98H | | | | | | |
| CFI Query Entry | $BK_X$[4] 55H | 98H | | | | | | | | | | |
| Software ID Exit/ CFI Exit/ Sec ID Exit[10,11] | 555H | AAH | 2AAH | 55H | 555H | F0H | | | | | | |
| Software ID Exit/ CFI Exit/ Sec ID Exit[10,11] | XXH | F0H | | | | | | | | | | |

T6.1 1282

1. Address format $A_{10}$-$A_0$ (Hex), Addresses $A_{20}$-$A_{11}$ can be $V_{IL}$ or $V_{IH}$, but no other value, for the command sequence when in x16 mode. When in x8 mode, Addresses $A_{20}$-$A_{12}$, Address $A_{-1}$ and $DQ_{14}$-$DQ_8$ can be $V_{IL}$ or $V_{IH}$, but no other value, for the command sequence.
2. $DQ_{15}$-$DQ_8$ can be $V_{IL}$ or $V_{IH}$, but no other value, for the command sequence
3. WA = Program Word/Byte address
4. $SA_X$ for Sector-Erase; uses $A_{20}$-$A_{11}$ address lines
   $BA_X$ for Block-Erase; uses $A_{20}$-$A_{15}$ address lines
5. For SST34HF32x2xC/32x4x the Security ID Address Range is:
   (x16 mode) = 000000H to 000087H, (x8 mode) = 000000H to 00010FH
   SST ID is read at Address Range (x16 mode) = 000000H to 000007H (x8 mode) = 000000H to 00000FH
   User ID is read at Address Range (x16 mode) = 000008H to 000087H (x8 mode) = 000010H to 00010FH
   Lock Status is read at Address 0000FFH (x16) or 0001FFH (x8). Unlocked: DQ3 = 1 / Locked: DQ3 = 0.
6. SIWA = User Security ID Program Word/Byte address
   For SST34HF32x2xC/32x4x, valid Address Range is
   (x16 mode) = 000008H-000087H (x8 mode) = 000010H-00010FH.
   All 4 cycles of User Security ID Program and Program Lock-out must be completed before going back to Read-Array mode.
7. The User-Security-ID-Program-Lock-out command must be executed in x16 mode. (CIOF = $V_{IH}$)
8. The device does not remain in Software Product Identification mode if powered down.
9. $A_{19}$ and $A_{18}$ = $V_{IL}$
10. Both Software ID Exit operations are equivalent
11. IIf users never lock after programming, User Sec ID can be programmed over the previously unprogrammed bits (data=1) using the User Sec ID mode again (the programmed “0” bits cannot be reversed to “1”).

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**TABLE 7: CFI QUERY IDENTIFICATION STRING[1]**

| Address x16 Mode | Address x8 Mode | Data[2] | Description |
|---|---|---|---|
| 10H | 20H | 0051H | Query Unique ASCII string “QRY” |
| 11H | 22H | 0052H | |
| 12H | 24H | 0059H | |
| 13H | 26H | 0002H | Primary OEM command set |
| 14H | 28H | 0000H | |
| 15H | 2AH | 0000H | Address for Primary Extended Table |
| 16H | 2CH | 0000H | |
| 17H | 2EH | 0000H | Alternate OEM command set (00H = none exists) |
| 18H | 30H | 0000H | |
| 19H | 32H | 0000H | Address for Alternate OEM extended Table (00H = none exits) |
| 1AH | 34H | 0000H | |

T7.1 1282

1. Refer to CFI publication 100 for more details.
2. In x8 mode, only the lower byte of data is output.

**TABLE 8: SYSTEM INTERFACE INFORMATION**

| Address x16 Mode | Address x8 Mode | Data[1] | Description |
|---|---|---|---|
| 1BH | 36H | 0027H | $V_{DD}$ Min (Program/Erase)<br>$DQ_7$-$DQ_4$: Volts, $DQ_3$-$DQ_0$: 100 millivolts |
| 1CH | 38H | 0036H | $V_{DD}$ Max (Program/Erase)<br>$DQ_7$-$DQ_4$: Volts, $DQ_3$-$DQ_0$: 100 millivolts |
| 1DH | 3AH | 0000H | $V_{PP}$ min (00H = no $V_{PP}$ pin) |
| 1EH | 3CH | 0000H | $V_{PP}$ max (00H = no $V_{PP}$ pin) |
| 1FH | 3EH | 0004H | Typical time out for Program $2^N$ µs ($2^4$ = 16 µs) |
| 20H | 40H | 0000H | Typical time out for min size buffer program $2^N$ µs (00H = not supported) |
| 21H | 42H | 0004H | Typical time out for individual Sector/Block-Erase $2^N$ ms ($2^4$ = 16 ms) |
| 22H | 44H | 0006H | Typical time out for Chip-Erase $2^N$ ms ($2^6$ = 64 ms) |
| 23H | 46H | 0001H | Maximum time out for Program $2^N$ times typical ($2^1$ x $2^4$ = 32 µs) |
| 24H | 48H | 0000H | Maximum time out for buffer program $2^N$ times typical |
| 25H | 4AH | 0001H | Maximum time out for individual Sector-/Block-Erase $2^N$ times typical ($2^1$ x $2^4$ = 32 ms) |
| 26H | 4CH | 0001H | Maximum time out for Chip-Erase $2^N$ times typical ($2^1$ x $2^6$ = 128 ms) |

T8.0 1282

1. In x8 mode, only the lower byte of data is output.

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Advance Information

**TABLE 9: DEVICE GEOMETRY INFORMATION**

| Address x16 Mode | Address x8 Mode | Data[1] | Description |
|---|---|---|---|
| 27H | 4EH | 0016H | Device size = $2^N$ Bytes (16H = 22; $2^{22}$ = 4 MByte) |
| 28H | 50H | 0002H | Flash Device Interface description; 0002H = x8/x16 asynchronous interface |
| 29H | 52H | 0000H | |
| 2AH | 54H | 0000H | Maximum number of bytes in multi-byte write = $2^N$ (00H = not supported) |
| 2BH | 56H | 0000H | |
| 2CH | 58H | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH | 5AH | 003FH | Block Information (y + 1 = Number of blocks; z x 256B = block size) |
| 2EH | 5CH | 0000H | y = 63 + 1 = 64 blocks (003FH = 63) |
| 2FH | 5EH | 0000H | |
| 30H | 60H | 0001H | z = 256 x 256 Bytes = 64 KByte/block (0100H = 256) |
| 31H | 62H | 00FFH | Sector Information (y + 1 = Number of sectors; z x 256B = sector size) |
| 32H | 64H | 0003H | y = 1023 + 1 = 1024 sectors (03FFH = 1023) |
| 33H | 66H | 0010H | |
| 34H | 68H | 0000H | z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16) |

T9.2 1282

1. In x8 mode, only the lower byte of data is output.

Advance Information

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +125°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to $V_{DD}$[1]+0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to $V_{DD}$[1]+1.0V
Package Power Dissipation Capability ($T_A$ = 25°C) . . . . . 1.0W
Surface Mount Solder Reflow Temperature[2] . . . . . 260°C for 10 seconds
Output Short Circuit Current[3] . . . . . 50 mA

1. $V_{DD}$ = $V_{DDF}$ and $V_{DDS}$
2. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
3. Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE**

| Range | Ambient Temp | $V_{DD}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 2.7-3.3V |
| Extended | -20°C to +85°C | 2.7-3.3V |

**AC CONDITIONS OF TEST**

| | |
|---|---|
| Input Rise/Fall Time | 5 ns |
| Output Load | $C_L$ = 30 pF |
| See Figures 19 and 20 | |

Advance Information

**TABLE 10: DC OPERATING CHARACTERISTICS ($V_{DD}$ = $V_{DDF}$ AND $V_{DDS}$ = 2.7-3.3V)**

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | Units | |
| $I_{DD}$[1] | Active $V_{DD}$ Current | | | | Address input = $V_{ILT}/V_{IHT}$, at f=5 MHz, $V_{DD}=V_{DD}$ Max, all DQs open |
| | Read | | | | OE#=$V_{IL}$, WE#=$V_{IH}$ |
| | Flash | | 35 | mA | BEF#=$V_{IL}$, BES1#=$V_{IH}$, or BES2=$V_{IL}$ |
| | (P)SRAM | | 30 | mA | BEF#=$V_{IH}$, BES1#=$V_{IL}$ , BES2=$V_{IH}$ |
| | Concurrent Operation | | 60 | mA | BEF#=$V_{IH}$, BES1#=$V_{IL}$ , BES2=$V_{IH}$ |
| | Write[2] | | | | WE#=$V_{IL}$ |
| | Flash | | 40 | mA | BEF#=$V_{IL}$, BES1#=$V_{IH}$, or BES2=$V_{IL}$, OE#=$V_{IH}$ |
| | (P)SRAM | | 30 | mA | BEF#=$V_{IH}$, BES1#=$V_{IL}$ , BES2=$V_{IH}$ |
| $I_{SB}$ | Standby $V_{DD}$ Current SRAM | | 30 | µA | $V_{DD}$ = $V_{DD}$ Max, BEF#=BES1#=$V_{IHC}$, BES2=$V_{ILC}$ |
| | PSRAM | | 85 | µA | |
| $I_{RT}$ | Reset $V_{DD}$ Current | | 30 | µA | RST#=GND |
| $I_{LI}$ | Input Leakage Current | | 1 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max |
| $I_{LIW}$ | Input Leakage Current on WP# pin and RST# pin | | 10 | µA | WP#=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max<br>RST#=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}=V_{DD}$ Max |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD}$ Min |
| $V_{ILC}$ | Input Low Voltage (CMOS) | | 0.3 | V | $V_{DD}=V_{DD}$ Max |
| $V_{IH}$ | Input High Voltage | 0.7 $V_{DD}$ | | V | $V_{DD}=V_{DD}$ Max |
| $V_{IHC}$ | Input High Voltage (CMOS) | $V_{DD}$-0.3 | | V | $V_{DD}=V_{DD}$ Max |
| $V_{OLF}$ | Flash Output Low Voltage | | 0.2 | V | $I_{OL}$=100 µA, $V_{DD}=V_{DD}$ Min |
| $V_{OHF}$ | Flash Output High Voltage | $V_{DD}$-0.2 | | V | $I_{OH}$=-100 µA, $V_{DD}=V_{DD}$ Min |
| $V_{OLS}$ | (P)SRAM Output Low Voltage | | 0.4 | V | IOL =1 mA, $V_{DD}=V_{DD}$ Min |
| $V_{OHS}$ | (P)SRAM Output High Voltage | 2.2 | | V | IOH =-500 µA, $V_{DD}=V_{DD}$ Min |

T10.0 1282

1. Address input = $V_{ILT}/V_{IHT}$, $V_{DD}=V_{DD}$ Max (See Figure 19)
2. $I_{DD}$ active while Erase or Program is in progress.

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**TABLE 11: RECOMMENDED SYSTEM POWER-UP TIMINGS**

| Symbol | Parameter | Minimum | Units |
|---|---|---|---|
| $T_{PU-READ}$[1] | Power-up to Read Operation | 100 | µs |
| $T_{PU-WRITE}$[1] | Power-up to Write Operation | 100 | µs |

T11.0 1282

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 12: CAPACITANCE ($T_A$ = 25°C, f=1 Mhz, other pins open)**

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$ = 0V | 20 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V | 16 pF |

T12.0 1282

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 13: FLASH RELIABILITY CHARACTERISTICS**

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---|---|---|---|---|
| $N_{END}$[1] | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| $T_{DR}$[1] | Data Retention | 100 | Years | JEDEC Standard A103 |
| $I_{LTH}$[1] | Latch Up | 100 + $I_{DD}$ | mA | JEDEC Standard 78 |

T13.0 1282

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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## AC CHARACTERISTICS

**TABLE 14: (P)SRAM READ CYCLE TIMING PARAMETERS**

| | | Min | Max | Units |
|---|---|---|---|---|
| $T_{RCS}$ | Read Cycle Time | 70 | | ns |
| $T_{AAS}$ | Address Access Time | | 70 | ns |
| $T_{BES}$ | Bank Enable Access Time | | 70 | ns |
| $T_{OES}$ | Output Enable Access Time | | 35 | ns |
| $T_{BYES}$ | UBS#, LBS# Access Time | | 70 | ns |
| $T_{BLZS}$[1] | BES# to Active Output | 0 | | ns |
| $T_{OLZS}$[1] | Output Enable to Active Output | 0 | | ns |
| $T_{BYLZS}$[1] | UBS#, LBS# to Active Output | 0 | | ns |
| $T_{BHZS}$[1] | BES# to High-Z Output | | 25 | ns |
| $T_{OHZS}$[1] | Output Disable to High-Z Output | | 25 | ns |
| $T_{BYHZS}$[1] | UBS#, LBS# to High-Z Output | | 35 | ns |
| $T_{OHS}$ | Output Hold from Address Change | 10 | | ns |

T14.0 1282

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 15: (P)SRAM WRITE CYCLE TIMING PARAMETERS**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{WCS}$ | Write Cycle Time | 70 | | ns |
| $T_{BWS}$ | Bank Enable to End-of-Write | 60 | | ns |
| $T_{AWS}$ | Address Valid to End-of-Write | 60 | | ns |
| $T_{ASTS}$ | Address Set-up Time | 0 | | ns |
| $T_{WPS}$ | Write Pulse Width | 60 | | ns |
| $T_{WRS}$ | Write Recovery Time | 0 | | ns |
| $T_{BYWS}$ | UBS#, LBS# to End-of-Write | 60 | | ns |
| $T_{ODWS}$ | Output Disable from WE# Low | | 30 | ns |
| $T_{OEWS}$ | Output Enable from WE# High | 0 | | ns |
| $T_{DSS}$ | Data Set-up Time | 30 | | ns |
| $T_{DHS}$ | Data Hold from Write Time | 0 | | ns |

T15.0 1282

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**TABLE 16: FLASH READ CYCLE TIMING PARAMETERS $V_{DD}$ = 2.7-3.3V**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RC}$ | Read Cycle Time | 70 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 70 | ns |
| $T_{AA}$ | Address Access Time | | 70 | ns |
| $T_{OE}$ | Output Enable Access Time | | 35 | ns |
| $T_{CLZ}$[1] | BEF# Low to Active Output | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | ns |
| $T_{CHZ}$[1] | BEF# High to High-Z Output | | 16 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 16 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | ns |
| $T_{RP}$[1] | RST# Pulse Width | 500 | | ns |
| $T_{RHR}$[1] | RST# High Before Read | 50 | | ns |
| $T_{RY}$[1,2] | RST# Pin Low to Read | | 20 | µs |

T16.0 1282

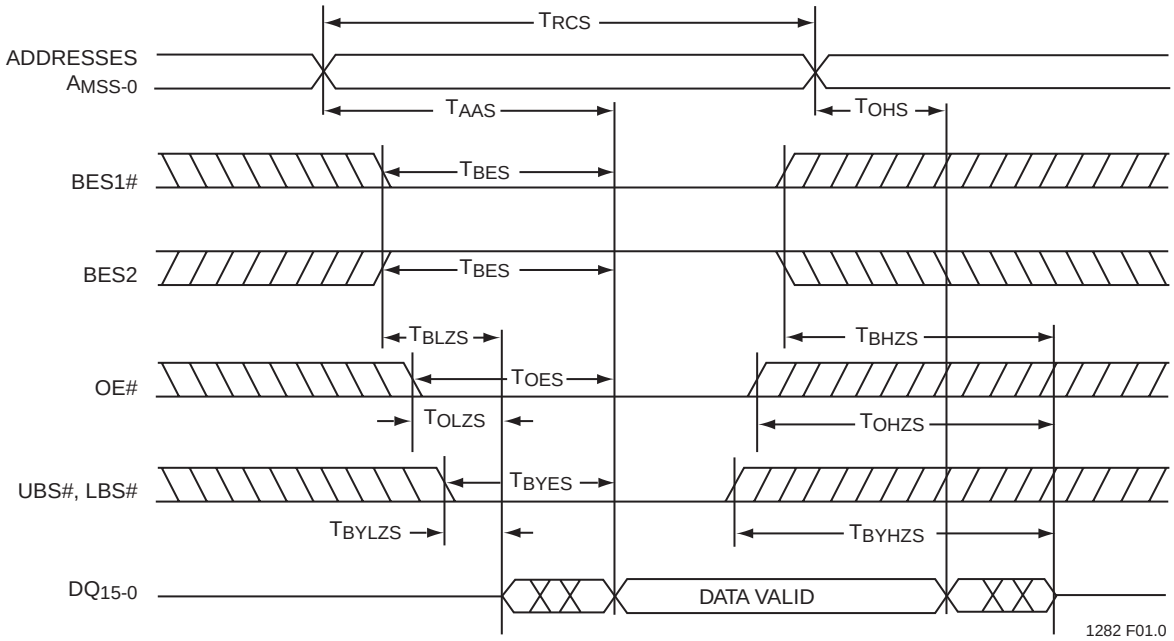
1. This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase and Program operations. This parameter does not apply to Chip-Erase.

**TABLE 17: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{BP}$ | Program Time | | 10 | µs |
| $T_{AS}$ | Address Setup Time | 0 | | ns |
| $T_{AH}$ | Address Hold Time | 40 | | ns |
| $T_{CS}$ | WE# and BEF# Setup Time | 0 | | ns |
| $T_{CH}$ | WE# and BEF# Hold Time | 0 | | ns |
| $T_{OES}$ | OE# High Setup Time | 0 | | ns |
| $T_{OEH}$ | OE# High Hold Time | 10 | | ns |
| $T_{CP}$ | BEF# Pulse Width | 40 | | ns |
| $T_{WP}$ | WE# Pulse Width | 40 | | ns |
| $T_{WPH}$[1] | WE# Pulse Width High | 30 | | ns |
| $T_{CPH}$[1] | BEF# Pulse Width High | 30 | | ns |
| $T_{DS}$ | Data Setup Time | 30 | | ns |
| $T_{DH}$[1] | Data Hold Time | 0 | | ns |
| $T_{IDA}$[1] | Software ID Access and Exit Time | | 150 | ns |
| $T_{ES}$ | Erase-Suspend Latency | | 10 | µs |
| $T_{BY}$[1,2] | RY/BY# Delay Time | 90 | | ns |
| $T_{BR}$[1] | Bus Recovery Time | | 1 | µs |
| $T_{SE}$ | Sector-Erase | | 25 | ms |
| $T_{BE}$ | Block-Erase | | 25 | ms |
| $T_{SCE}$ | Chip-Erase | | 50 | ms |

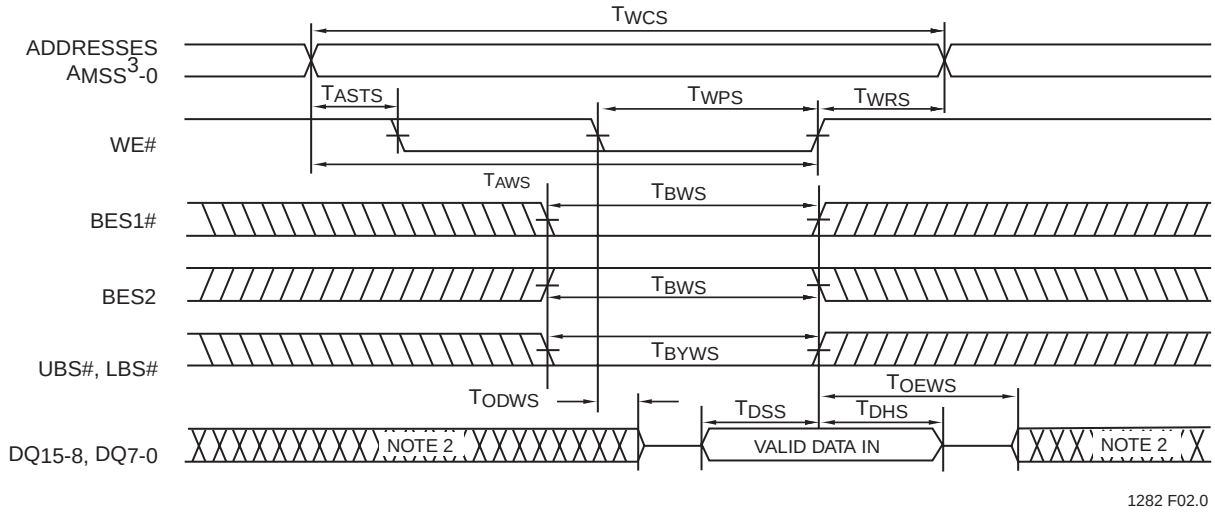
T17.1 1282

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
   This parameter does not apply to Chip-Erase operations.



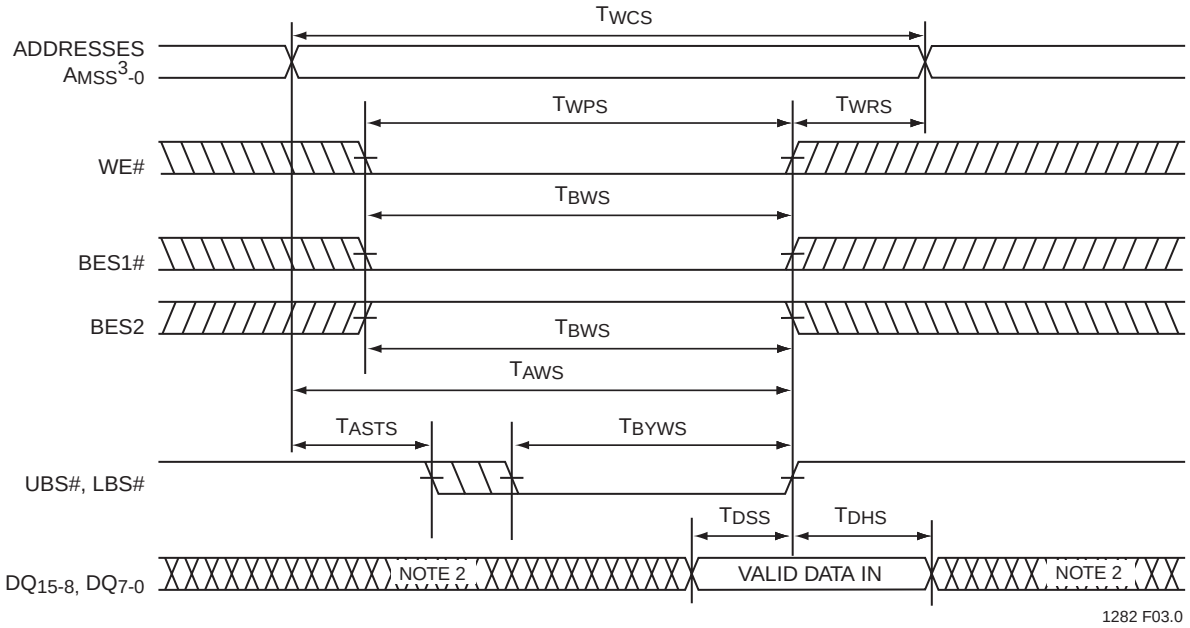

**Note:** $A_{MSS}$ = Most Significant Address
$A_{MSS} = A_{17}$ for SST34HF324xC and $A_{18}$ for SST34HF328x

**FIGURE 3: (P)SRAM READ CYCLE TIMING DIAGRAM**




**Note:** 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES1# goes Low or BES2 goes high coincident with or after WE# goes Low, the output will remain at high impedance. If BES1# goes High or BES2 goes low coincident with or before WE# goes High, the output will remain at high impedance. Because $D_{IN}$ signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. $A_{MSS}$ = Most Significant SRAM Address
$A_{MSS} = A_{17}$ for SST34HF324xC and $A_{18}$ for SST34HF328x

**FIGURE 4: (P)SRAM WRITE CYCLE TIMING DIAGRAM (WE# CONTROLLED)[1]**




**Note:** 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because $D_{IN}$ signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. $A_{MSS}$ = Most Significant SRAM Address
$A_{MSS}$ = $A_{17}$ for SST34HF324xC and $A_{18}$ for SST34HF328x

**FIGURE 5: (P)SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)[1]**

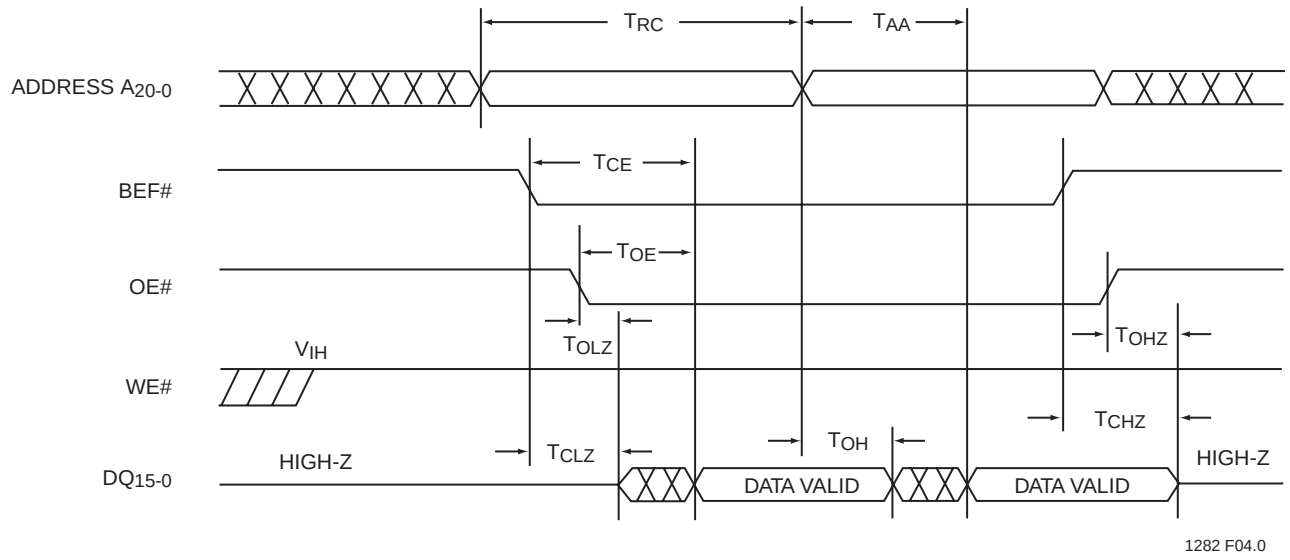
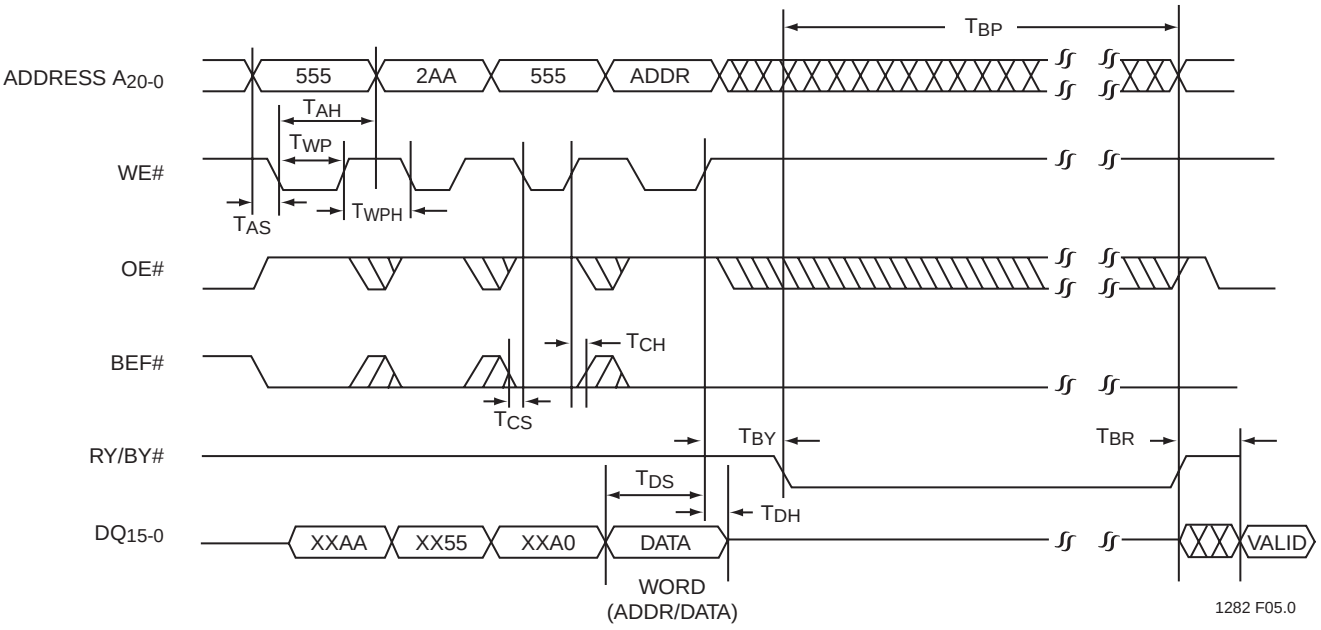
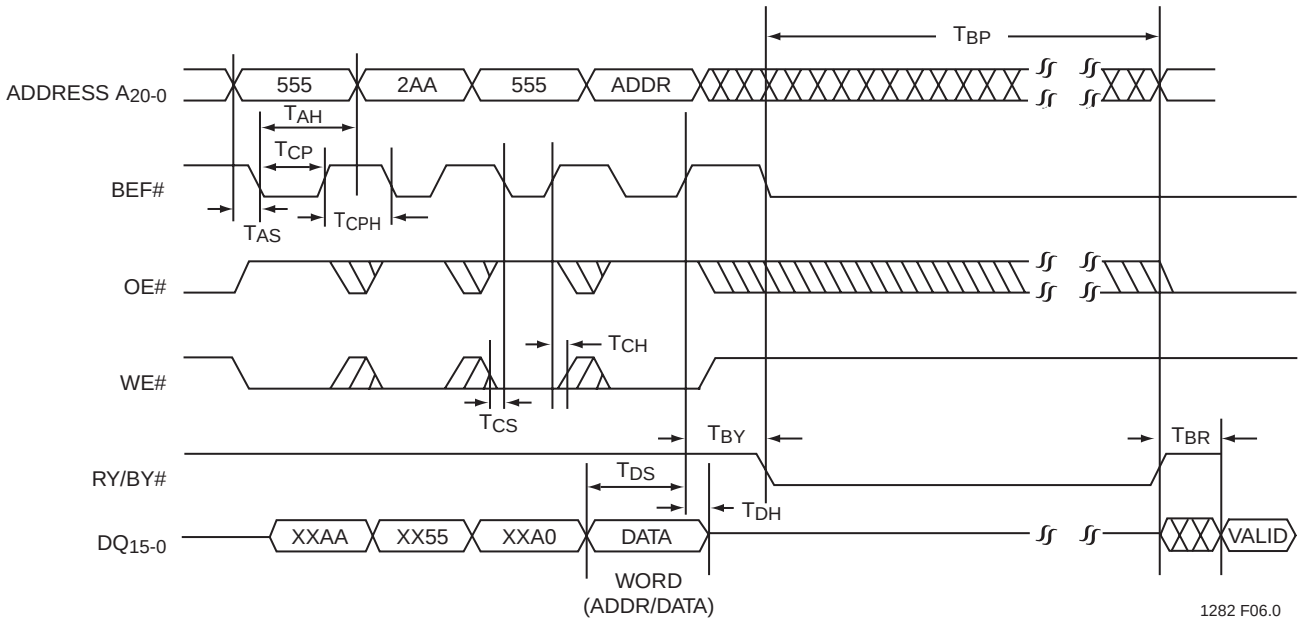



**FIGURE 6: FLASH READ CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = ADDRESS INPUT)**




**Note:** X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 7: FLASH WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = ADDRESS INPUT)**




**Note:** X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 8: FLASH BEF# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = ADDRESS INPUT)**

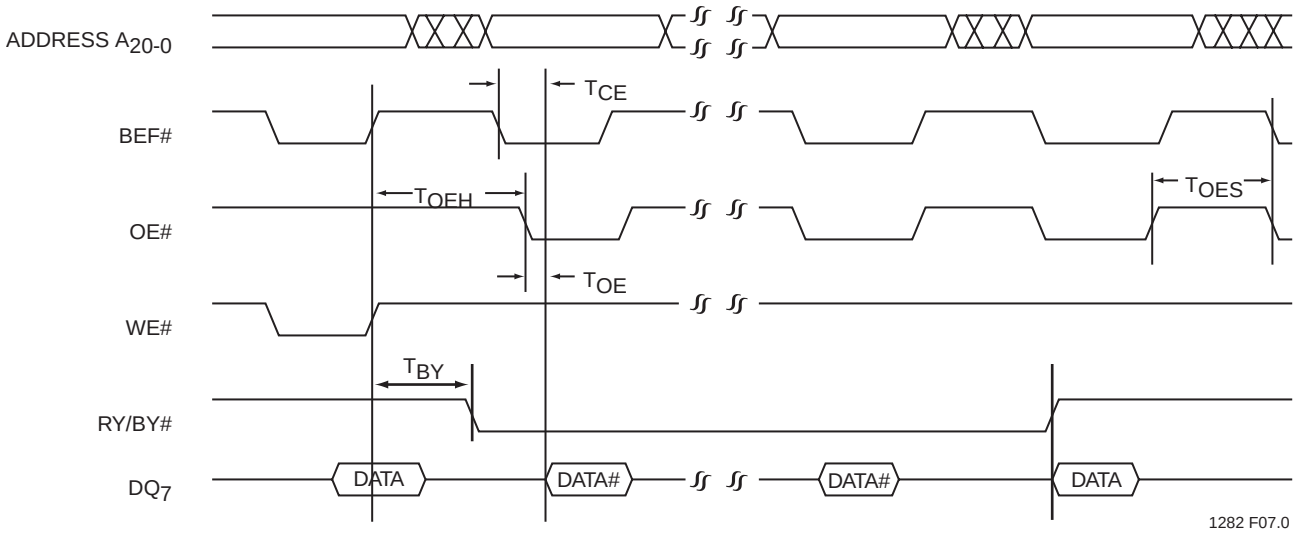



**FIGURE 9: FLASH DATA# POLLING TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = ADDRESS INPUT)**

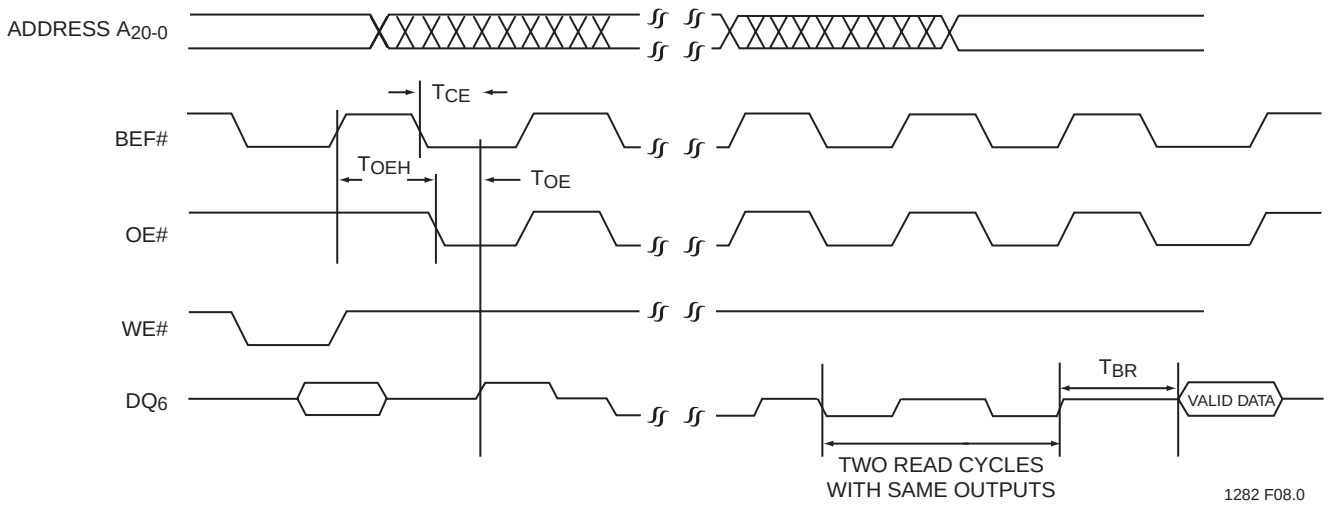
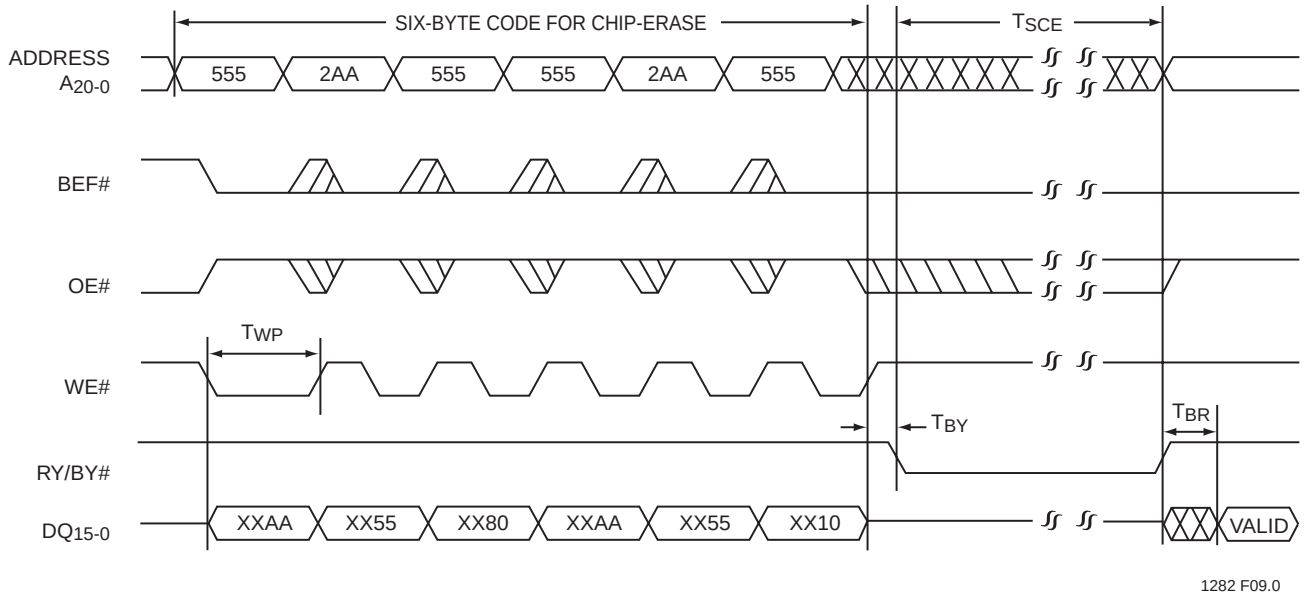
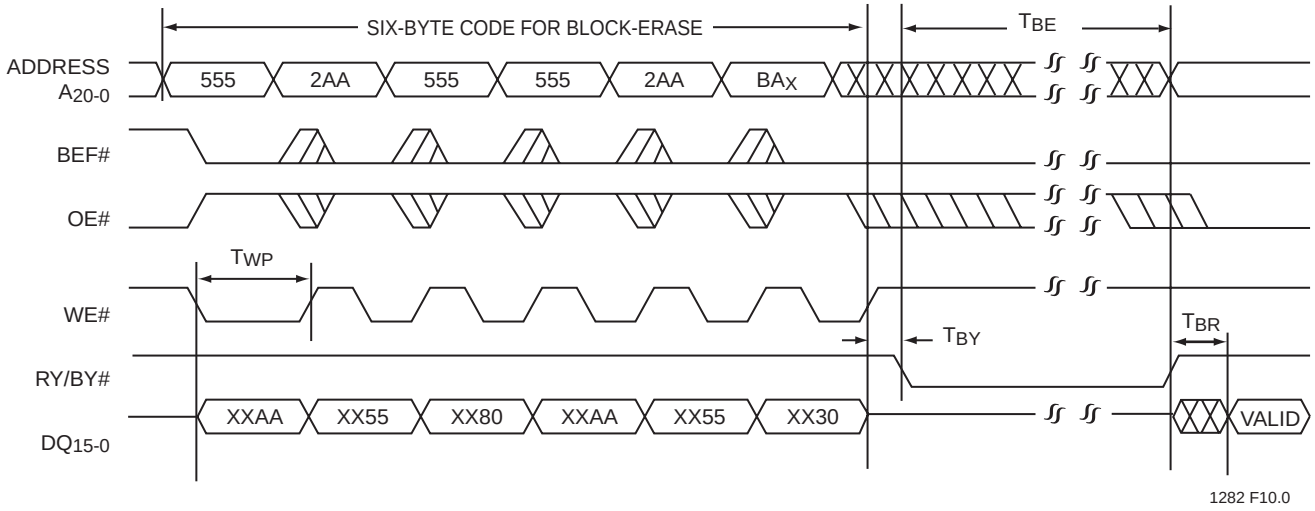



**FIGURE 10: FLASH TOGGLE BIT TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = DON'T CARE)**



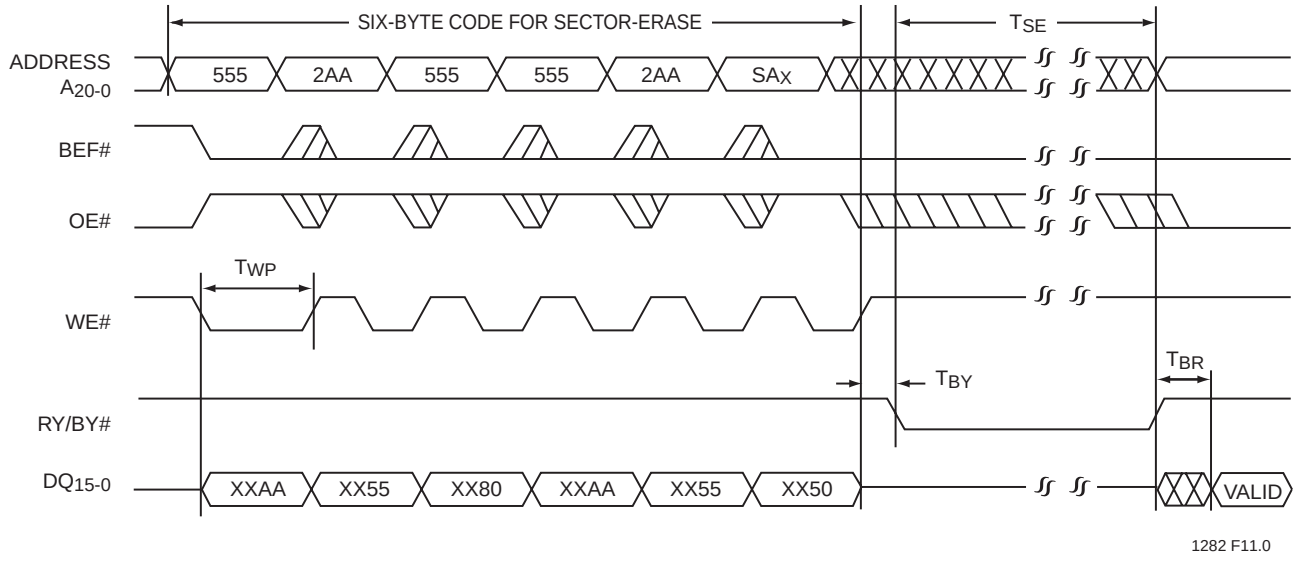

**Note:** This device also supports BEF# controlled Chip-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 17.)
X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 11: FLASH WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = DON'T CARE)**



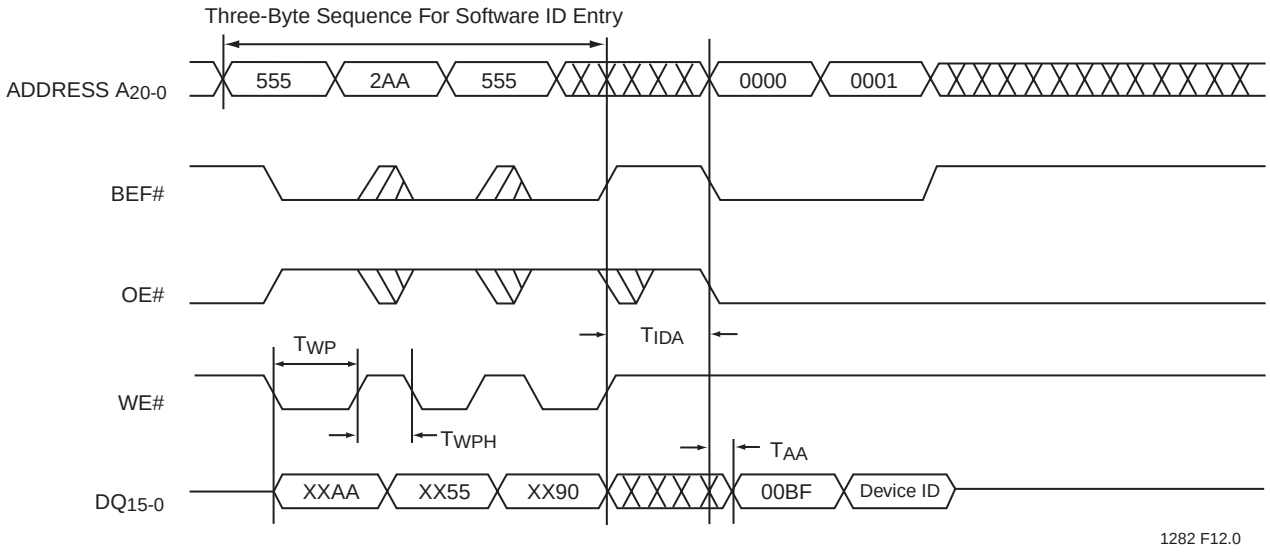

**Note:** This device also supports BEF# controlled Block-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 17.)
$BA_X$ = Block Address
X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 12: FLASH WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = DON'T CARE)**



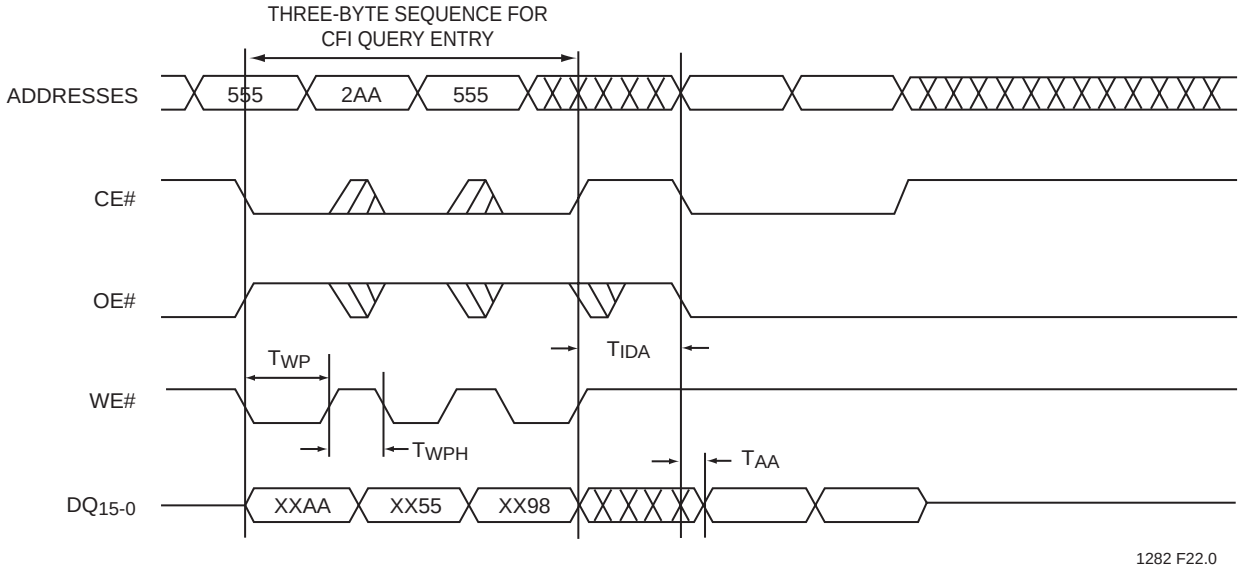

**Note:** This device also supports BEF# controlled Sector-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 17.)
$SA_X$ = Sector Address
X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 13: FLASH WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM FOR WORD MODE (FOR BYTE MODE $A_{-1}$ = DON'T CARE)**



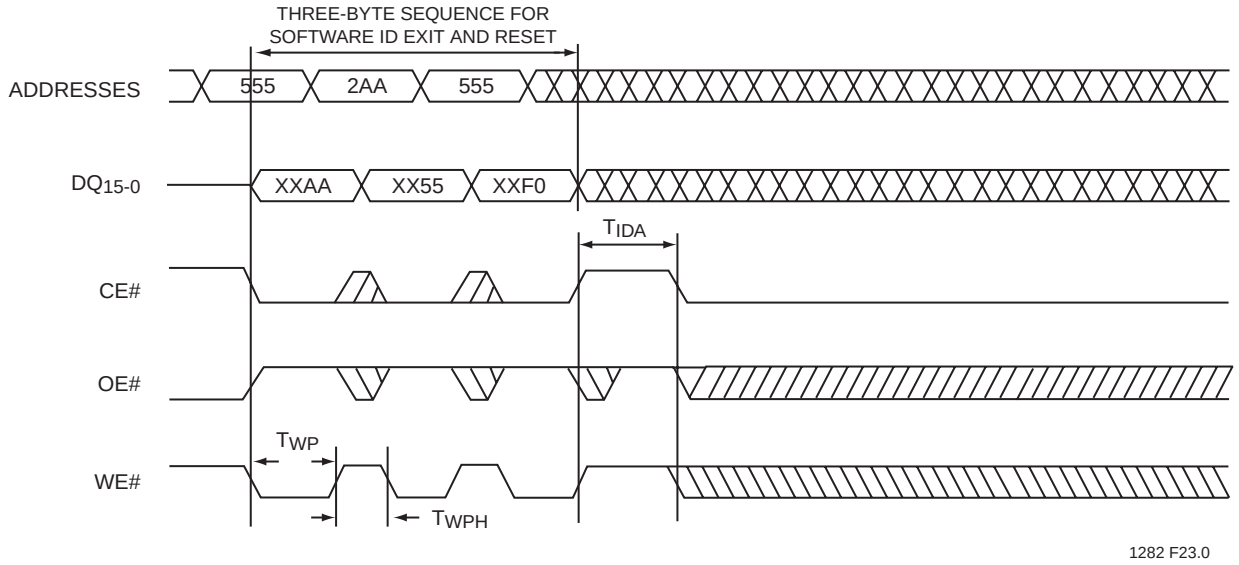

**Note:** X can be $V_{IL}$ or $V_{IH,}$ but no other value.
Device ID = 7351H for SST34HF3242C/3282 or 7353H for SST34HF3244C/3284

**FIGURE 14: FLASH SOFTWARE ID ENTRY AND READ (FOR BYTE MODE $A_{-1}$ = 0)**




Note: X can be $V_{IL}$ or $V_{IH,}$ but no other value.

**FIGURE 15: CFI ENTRY AND READ**




Note: X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 16: SOFTWARE ID EXIT/CFI EXIT**

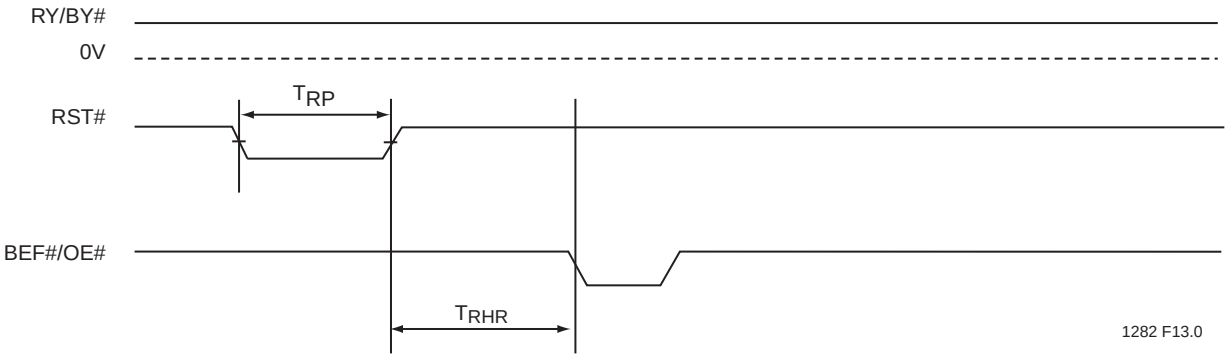



**FIGURE 17: RST# TIMING (WHEN NO INTERNAL OPERATION IS IN PROGRESS)**

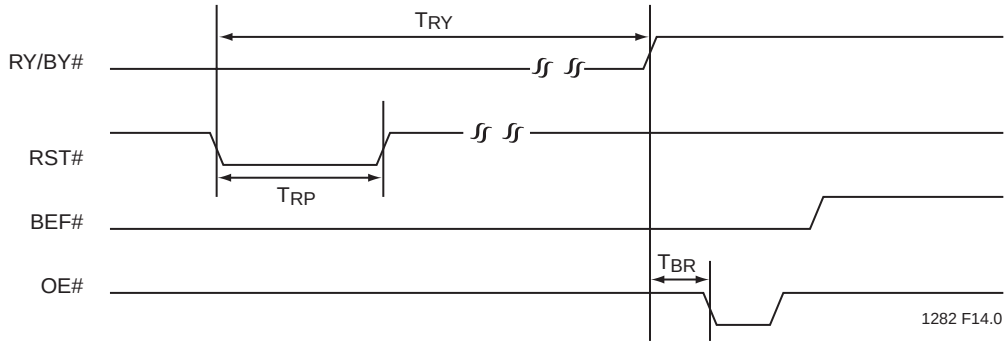
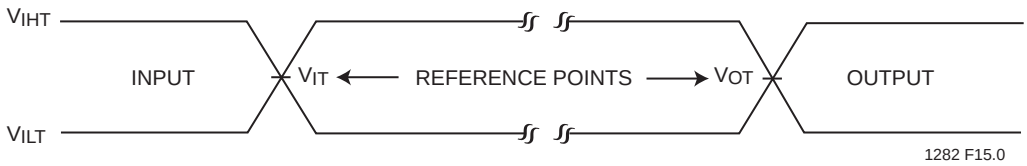



**FIGURE 18: RST# TIMING (DURING SECTOR- OR BLOCK-ERASE OPERATION)**




AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic "1" and $V_{ILT}$ (0.1 $V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

**Note:** $V_{IT}$ - $V_{INPUT}$ Test
$V_{OT}$ - $V_{OUTPUT}$ Test
$V_{IHT}$ - $V_{INPUT}$ HIGH Test
$V_{ILT}$ - $V_{INPUT}$ LOW Test

**FIGURE 19: AC INPUT/OUTPUT REFERENCE WAVEFORMS**

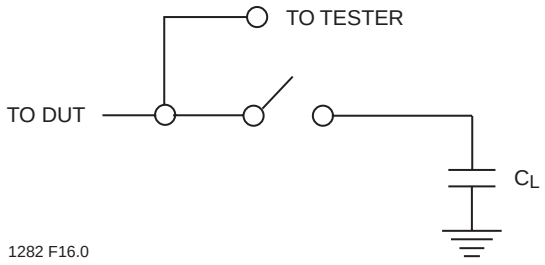
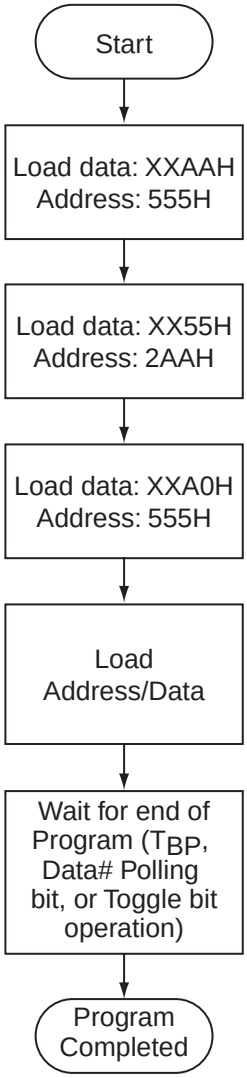



**FIGURE 20: A TEST LOAD EXAMPLE**




**Note:** X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 21: PROGRAM ALGORITHM**

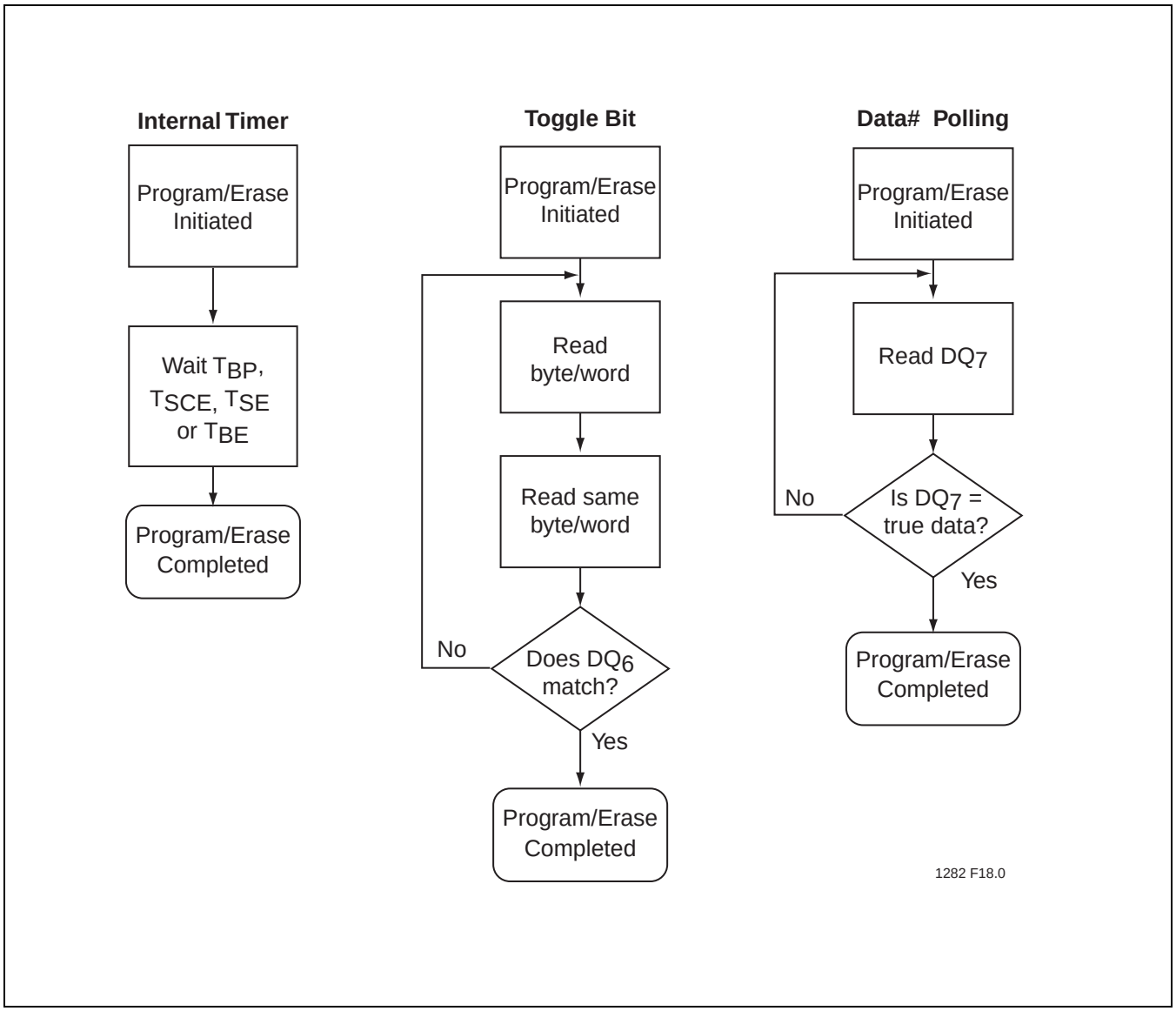
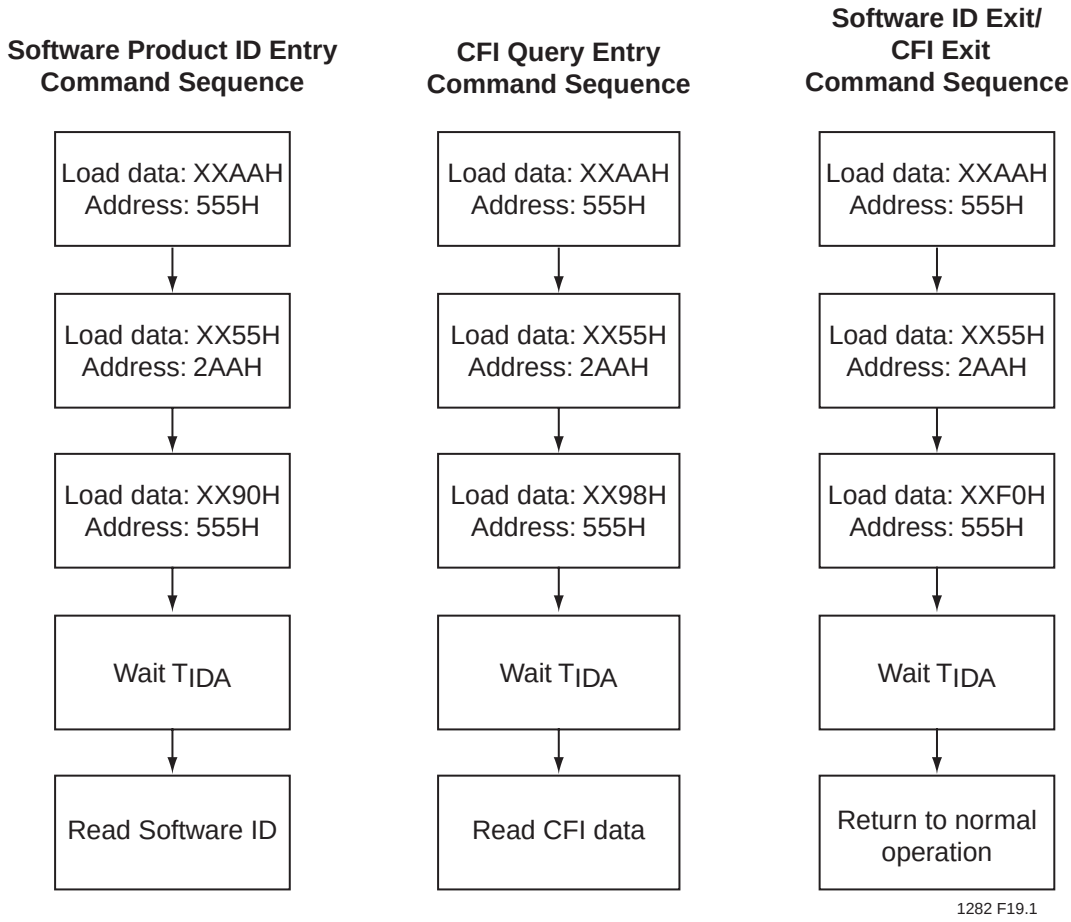



**FIGURE 22: WAIT OPTIONS**




**Note:** X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 23: SOFTWARE PRODUCT ID COMMAND FLOWCHARTS**

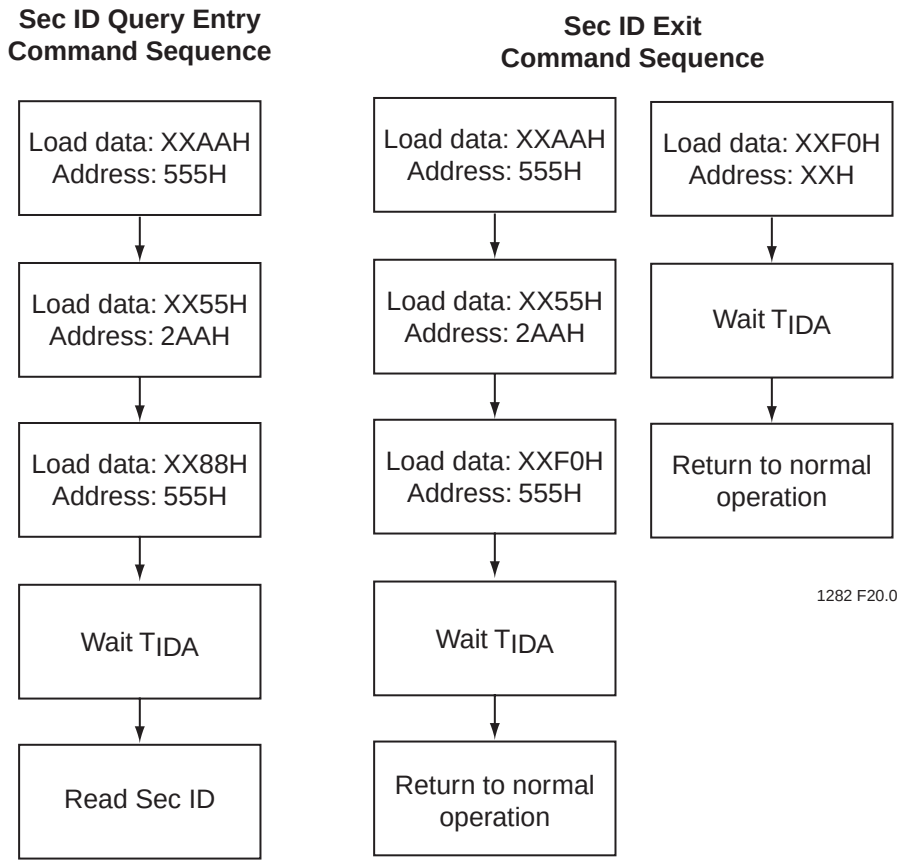
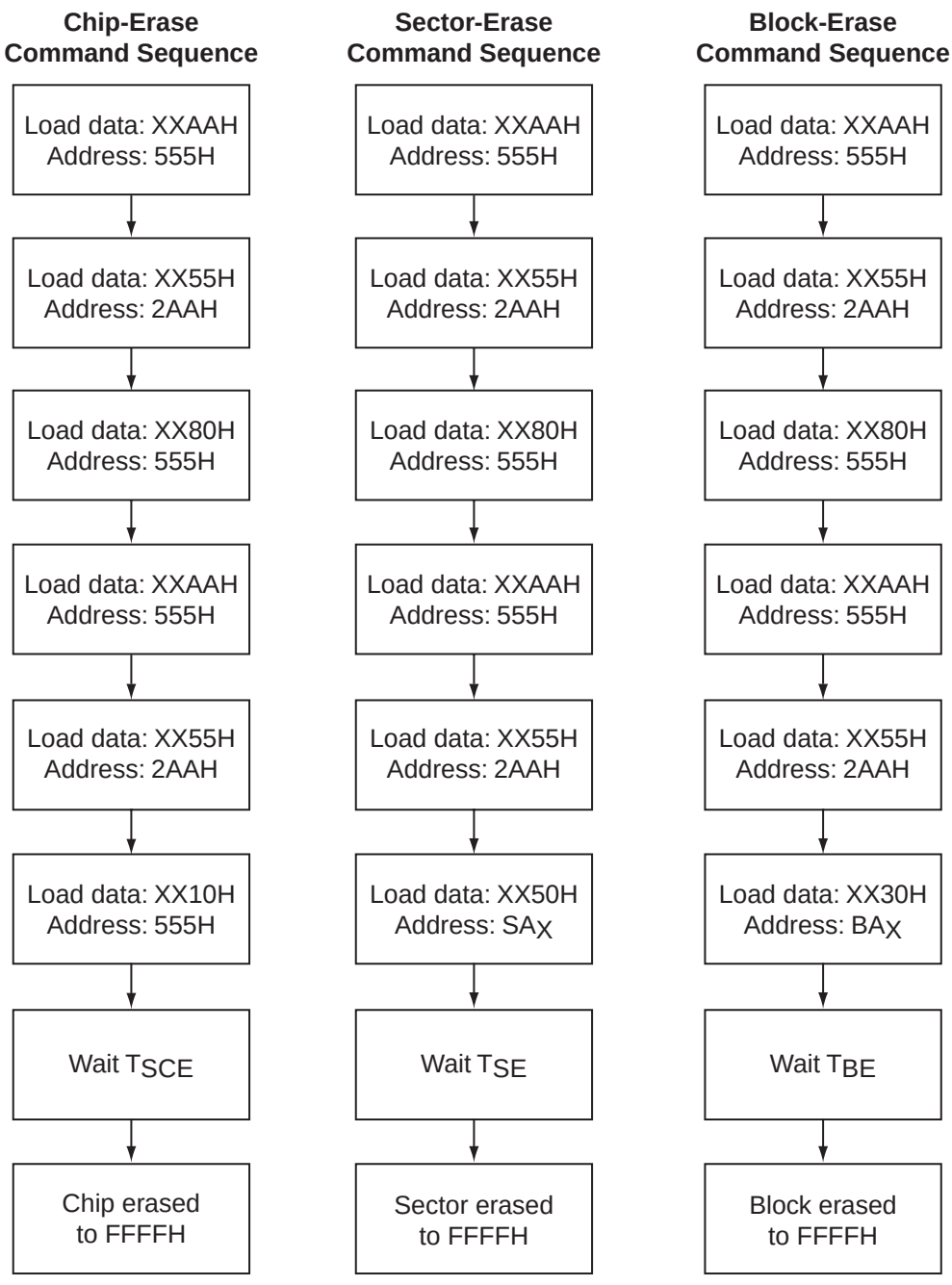



**FIGURE 24: SOFTWARE SEC ID COMMAND FLOWCHARTS**




**Note:** X can be $V_{IL}$ or $V_{IH}$, but no other value.

**FIGURE 25: ERASE COMMAND SEQUENCE**

## PRODUCT ORDERING INFORMATION

**Device** **Speed** **Suffix1** **Suffix2**

SST34HF32x4X- XXX - XX - XXXX

**Environmental Attribute**
E[1] = non-Pb

**Package Modifier**
P = 56 balls
S = 62 balls

**Package Type**
L1 = LFBGA (8mm x 10mm x 1.4mm, 0.45mm ball size)
L = LFBGA (8mm x 10mm x 1.4mm, 0.40mm ball size)

**Temperature Range**
E = Extended = -20°C to +85°C

**Minimum Endurance**
4 =10,000 cycles

**Read Access Speed**
70 = 70 ns

**Version**
C = x16 Mbit SRAM
blank = x16 PSRAM

**Bank Split and Top Boot Block Protection**
2 = 4 Mbit + 28 Mbit
4 = 8 Mbit + 24 Mbit

**(P)SRAM Density**
4 = 4 Mbit
8 = 8 Mbit

**Flash Density**
32 = 32 Mbit

**Voltage**
H = 2.7-3.3V

**Product Series**
34 = Concurrent SuperFlash + (P)SRAM ComboMemory

1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Advance Information

**Valid combinations for SST34HF3242C**

SST34HF3242C-70-4E-L1P
SST34HF3242C-70-4E-L1PE

**Valid combinations for SST34HF3244C**

SST34HF3244C-70-4E-L1P
SST34HF3244C-70-4E-L1PE SST34HF3244C-70-4E-LSE

**Valid combinations for SST34HF3282**

SST34HF3282-70-4E-L1P
SST34HF3282-70-4E-L1PE

**Valid combinations for SST34HF3284**

SST34HF3284-70-4E-L1P
SST34HF3284-70-4E-L1PE SST34HF3284-70-4E-LSE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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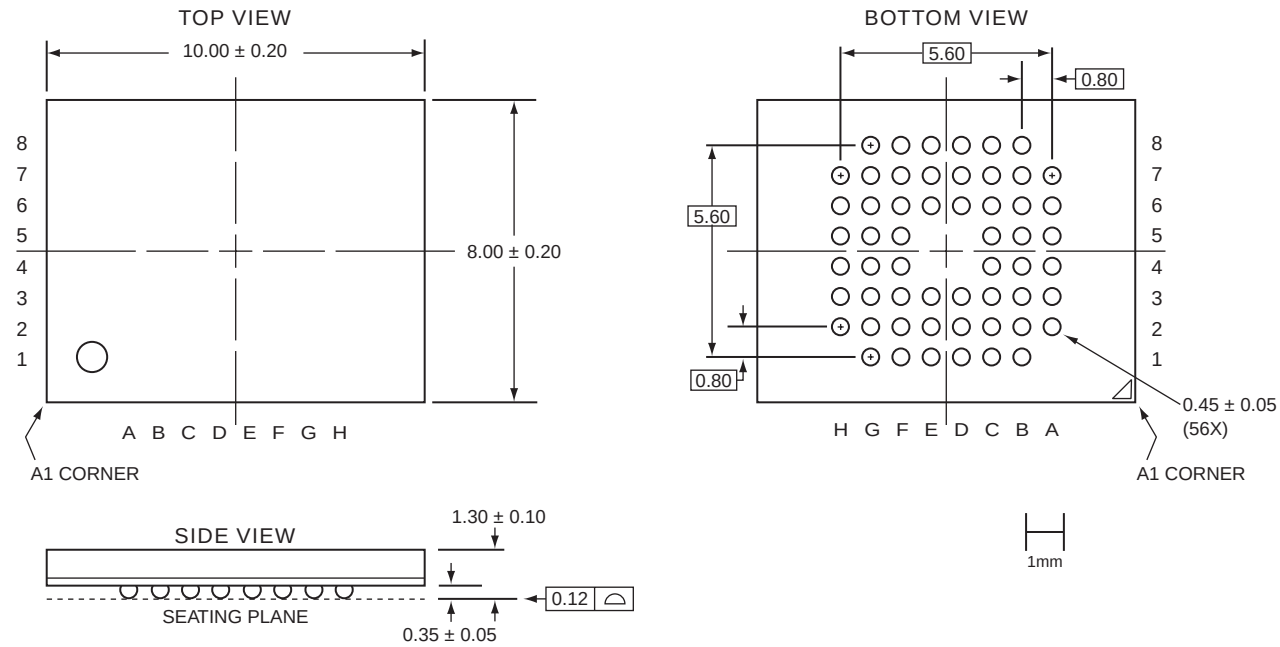
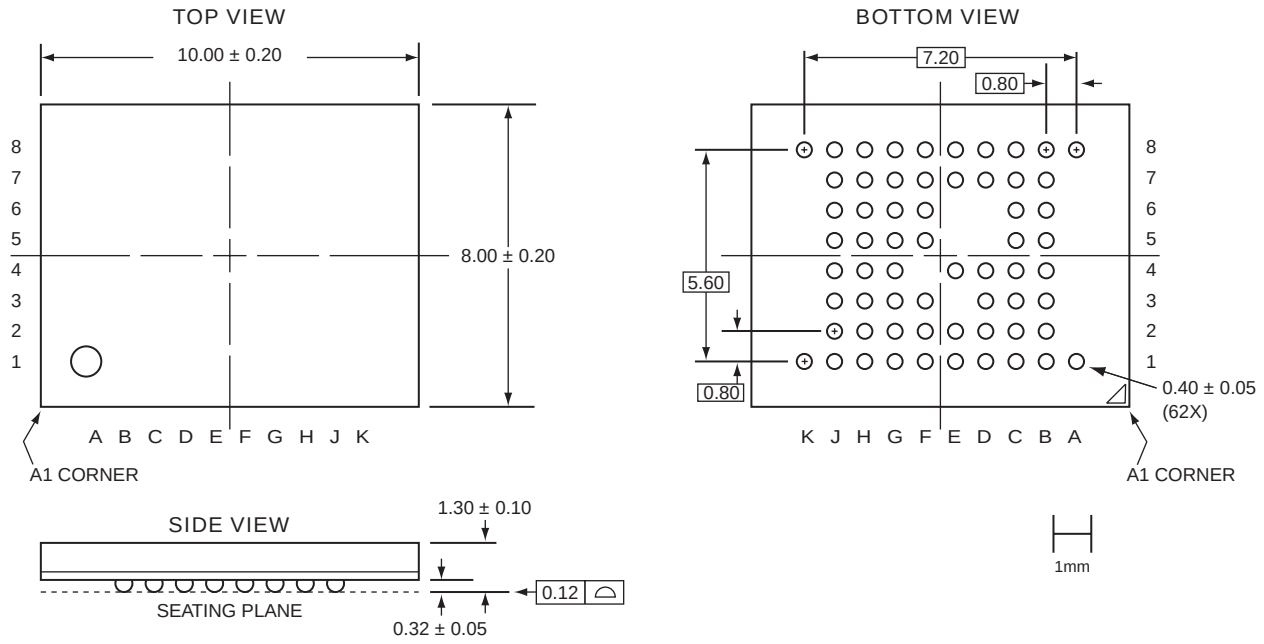
## PACKAGING DIAGRAMS




Note:
1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

56-lfbga-L1P-8x10-450mic-4

**56-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 8MM X 10MM**
**SST PACKAGE CODE: L1P**




Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.32 mm (± 0.05 mm)

62-lfbga-LS-8x10-400mic-4

**62-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 8MM X 10MM**
**SST PACKAGE CODE: LS**

**TABLE 18: REVISION HISTORY**

| Number | Description | Date |
|---|---|---|
| 00 | • Initial Release | Aug 2005 |



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