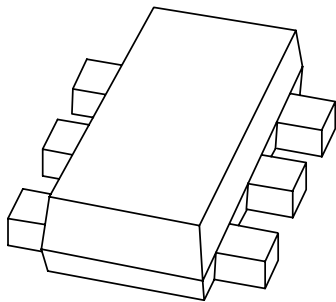


# DATA SHEET



## **PEMZ7** NPN/PNP general purpose transistors

Product specification  
Supersedes data of 2001 Sep 25

2001 Nov 07

# NPN/PNP general purpose transistors

# PEMZ7

## FEATURES

- 300 mW total power dissipation
- Very small 1.6 × 1.2 mm ultra thin package
- Self alignment during soldering due to straight leads
- Low collector capacitance
- Low  $V_{CEsat}$
- High current capabilities
- Improved thermal behaviour due to flat leads
- Reduced required PCB area
- Reduced pick and place costs.

## APPLICATIONS

- Heavy duty battery powered equipment (automotive, telecom and audio-video) such as motor and lamp drivers
- $V_{CEsat}$  critical applications such as latest low supply voltage IC applications
- All battery driven equipment, to save battery power.

## DESCRIPTION

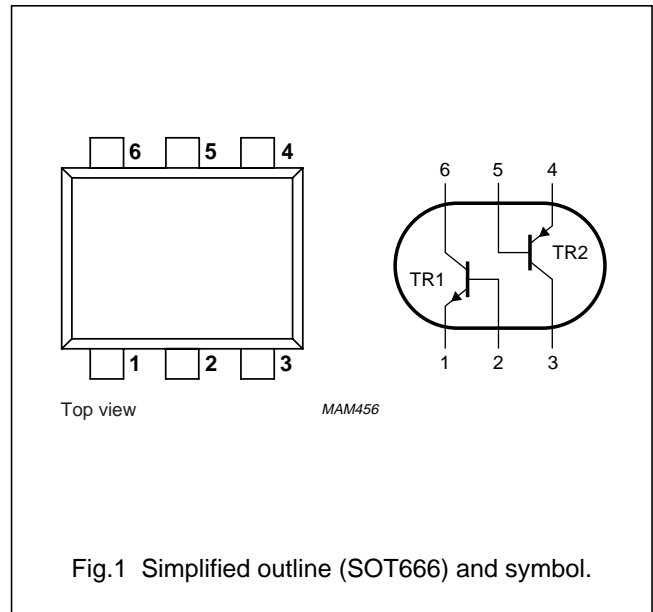
NPN/PNP low  $V_{CEsat}$  transistor pair in a SOT666 plastic package.

## MARKING

TYPE NUMBER	MARKING CODE
PEMZ7	Z7

## PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



## NPN/PNP general purpose transistors

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	15	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	12	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	6	V
I <sub>C</sub>	collector current (DC)		–	500	mA
I <sub>CM</sub>	peak collector current		–	1	A
I <sub>BM</sub>	peak base current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

**Notes**

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

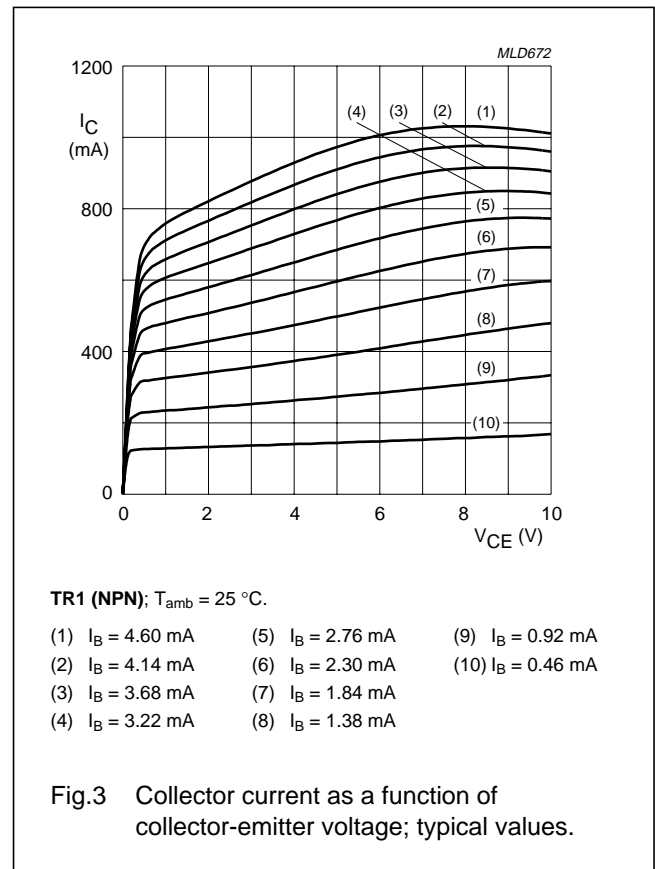
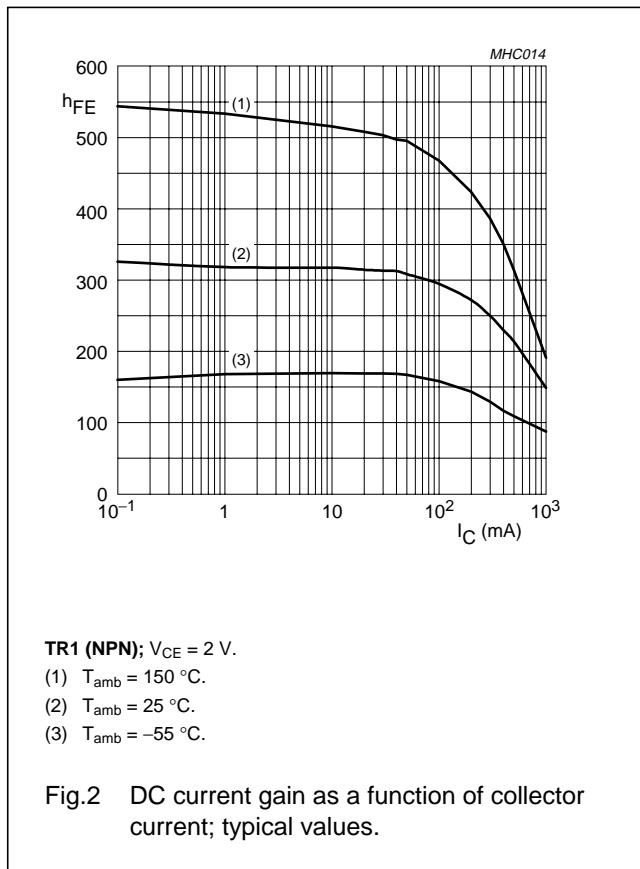
NPN/PNP general purpose transistors

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**CHARACTERISTICS**

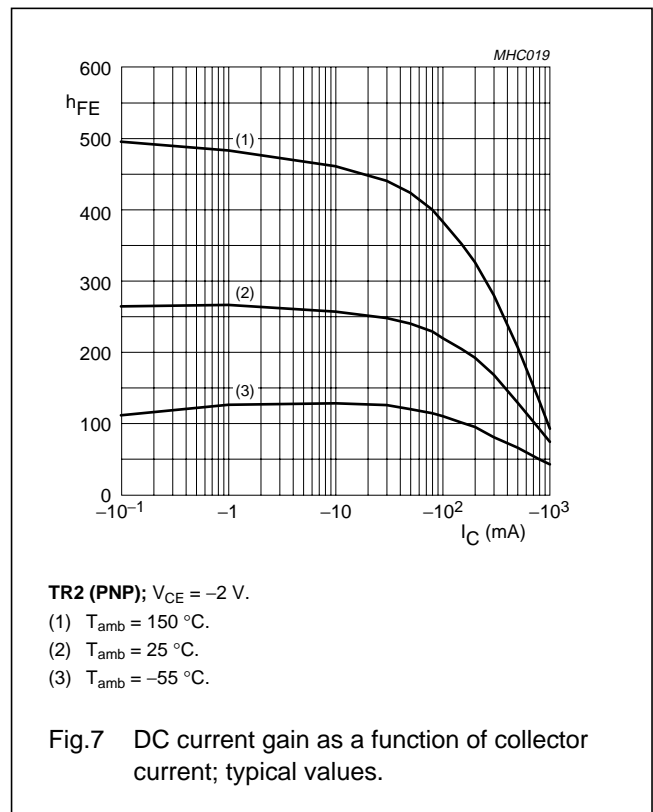
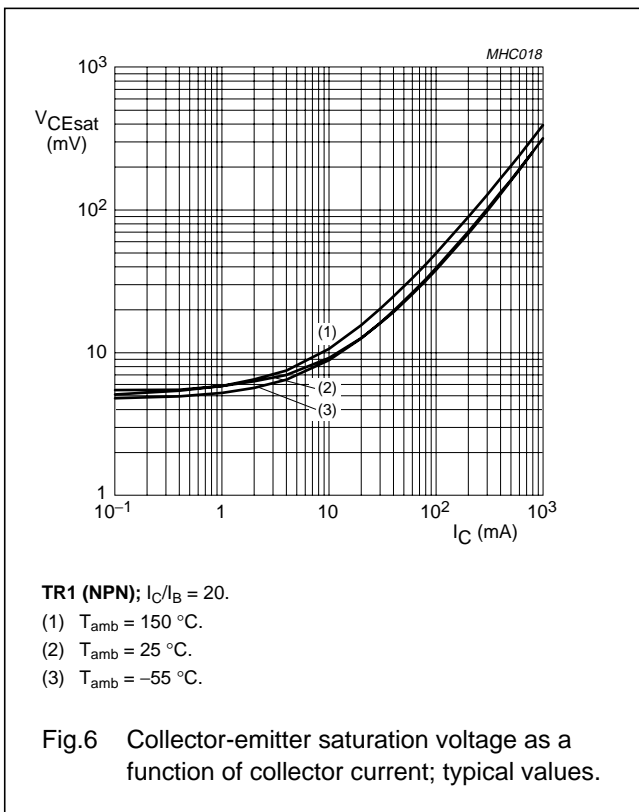
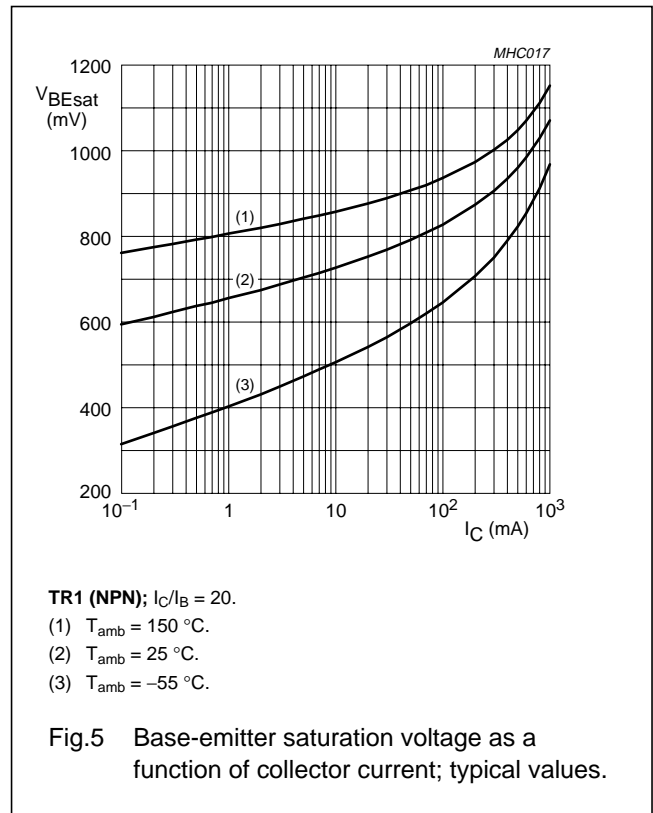
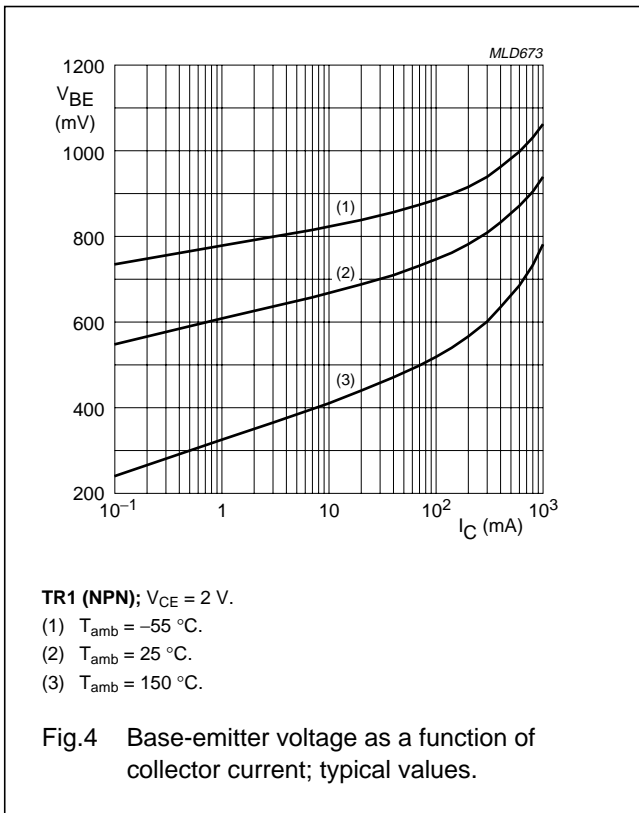
$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 15\text{ V}; I_E = 0$	–	–	100	nA
		$V_{CB} = 15\text{ V}; I_E = 0; T_j = 150\text{ }^{\circ}\text{C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 2\text{ V}; I_C = 10\text{ mA}$	200	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 200\text{ mA}; I_B = 10\text{ mA}$	–	–	220	mV
$f_T$	transition frequency TR1 (NPN) TR2 (PNP)	$I_C = 100\text{ mA}; V_{CE} = 5\text{ V};$ $f = 100\text{ MHz}$	250	420	–	MHz
			100	280	–	MHz
$C_c$	collector capacitance TR1 (NPN) TR2 (PNP)	$V_{CB} = 10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	4.4	6	pF
			–	–	10	pF



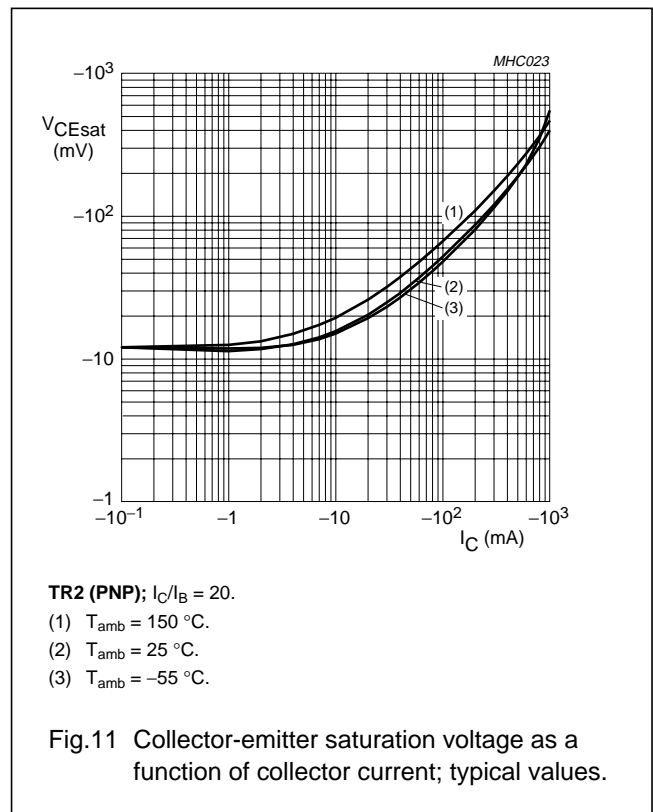
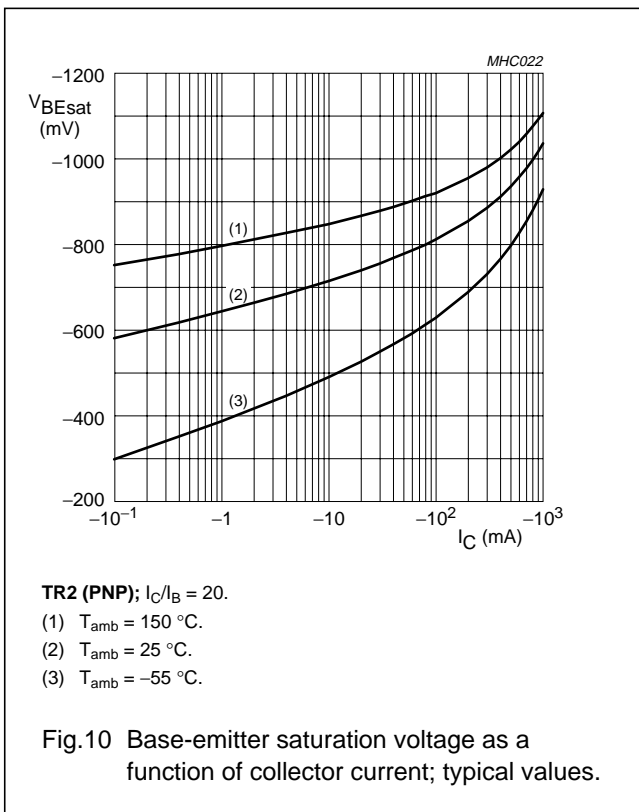
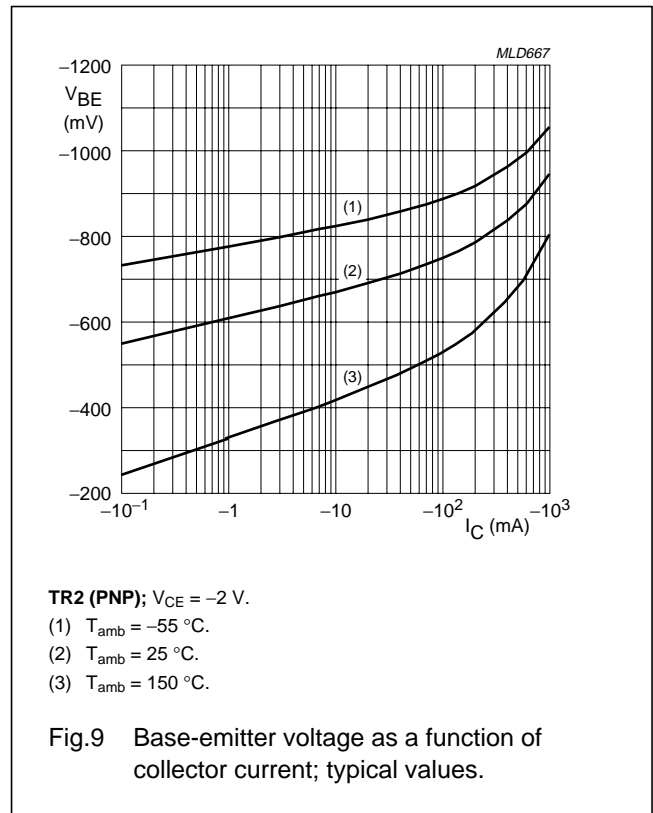
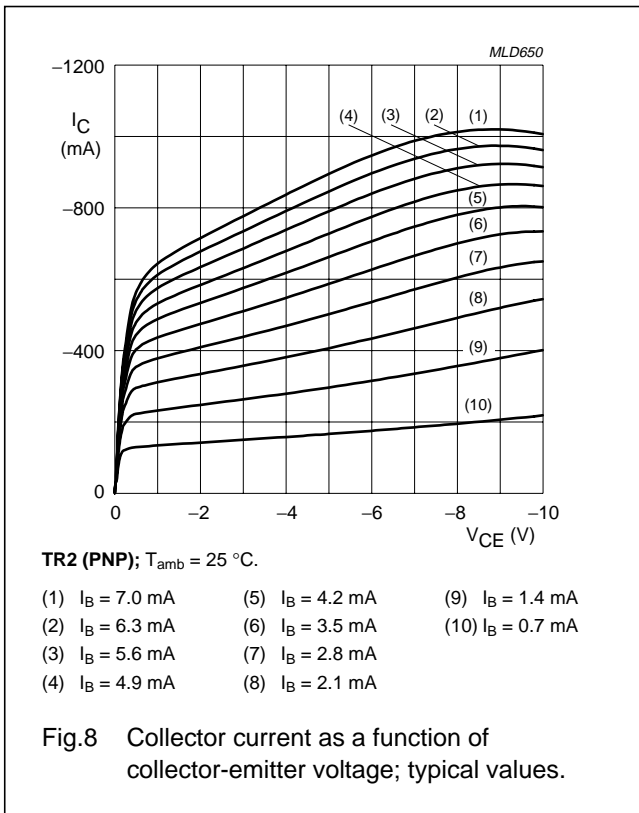
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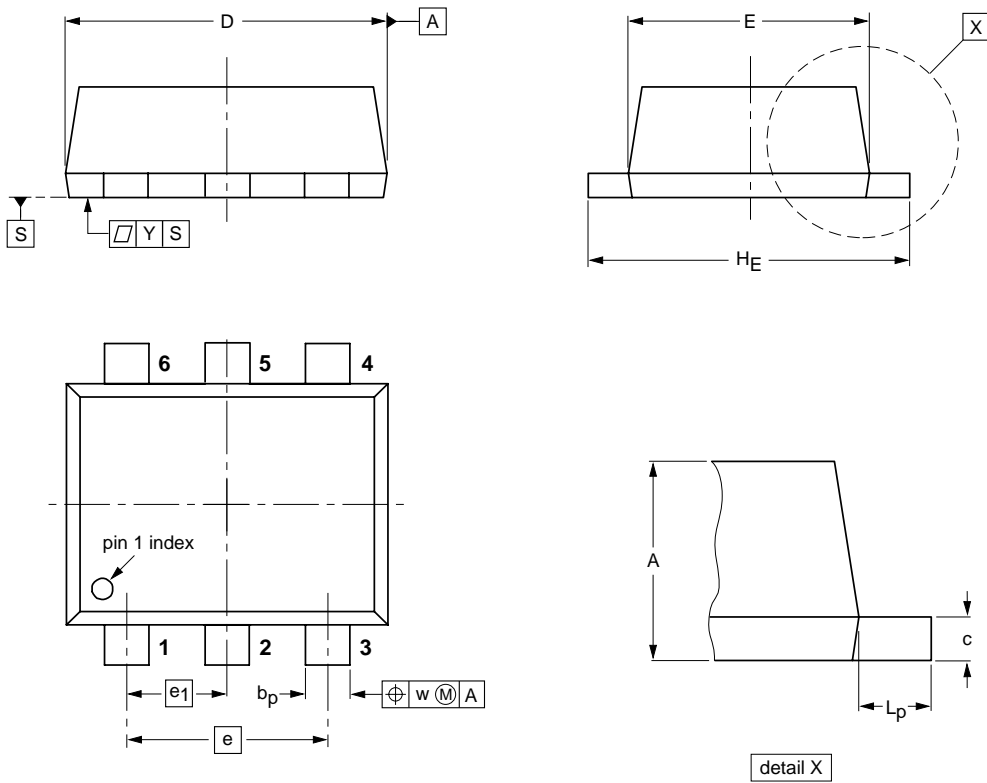
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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	$b_p$	c	D	E	e	$e_1$	$H_E$	$L_p$	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

## NPN/PNP general purpose transistors

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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**NOTES**

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**NOTES**

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