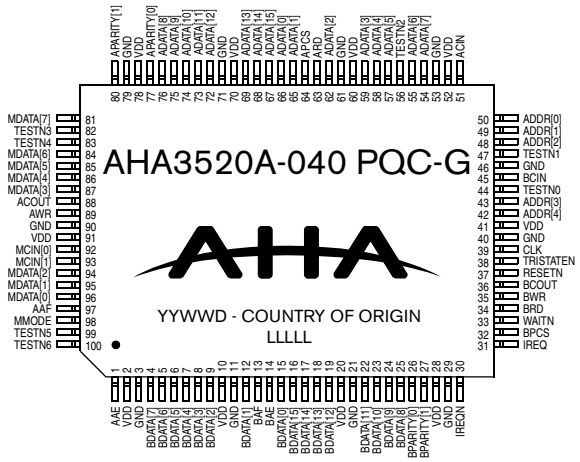
PRODUCT BRIEF*

AHA3520

20 MBYTES/SEC ALDC DATA COMPRESSION COPROCESSOR IC

The AHA3520 is a single-chip CMOS lossless compression and decompression integrated circuit. The device implements the ALDC compression algorithm defined by various industry standards. This algorithm is also known as Adaptive Lossless Data Compression.

The device compresses, decompresses or passes data through. Flexible interface connects directly with various microprocessors and DMA devices used in tape drive systems. Content Addressable Memory within the ALDC engine eliminates external SRAMs typically required for dictionary storage in a compression system. Other system features include compatibility to an ALDC1-20S-HA device.



NOTE: YYWWD = DATE CODE; LLLLL = LOT NUMBER

FEATURES

PERFORMANCE:

- 20 MBytes/sec data compression, decompression or pass-through rate
- 2 to 1 average compression ratio
- Multiple byte transfers without microprocessor intervention
- Error checking in decompression mode reportable via an interrupt

FLEXIBILITY:

- In-line or look-aside system architectures supported
- Polled or interrupt driven I/O
- Two independent DMA ports programmable for 8 or 16-bit transfers and handshaking modes

SYSTEM INTERFACE:

- Single-chip data compression solution
- Programmable interrupts
- Interfaces directly with industry standard SCSI chips

OTHERS:

- Industry standard ALDC adaptive lossless compression algorithm
- Complies to QIC-154, ECMA 222, ANSI X3.280-1996 and ISO 15200 standard specifications
- Compatible to ALDC1-20S-HA Specification
- 100 pin package in 14 mm × 20 mm PQFP
- RoHS compliant

APPLICATIONS

- Tape drives
- Printers and copiers

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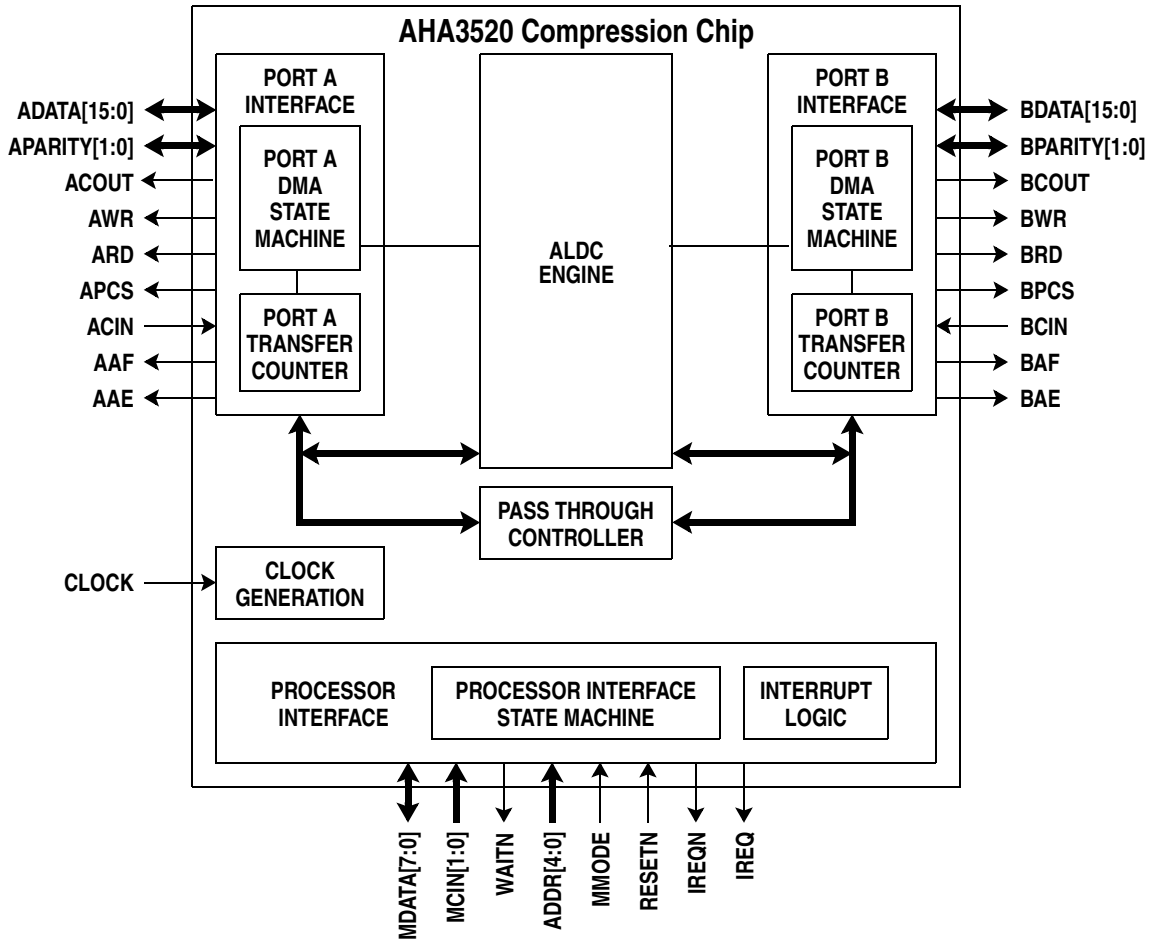
*Request the AHA3520 Product Specification for complete details.

Figure 1: AHA3520 Block Diagram



FUNCTIONAL DESCRIPTION

Major blocks in this device are the Microprocessor Interface, Port A Interface, Port B Interface, and the Compression/Decompression Engine. The Microprocessor Interface provides status and control information by register access. Port A and Port B Interfaces are DMA ports configurable for bus width, polarity, handshaking modes, and other options. The operating mode establishes the direction of both the Port A and Port B Interfaces. Compression or Compression Pass Through sets the Port A Interface as an input and the Port B Interface as an output. Conversely Decompression or Decompression Pass Through sets the Port A Interface as an output and the Port B Interface as an input. Decompression Output Disabled mode allows the device to decompress a block of data up to a predetermined point while dumping the uncompressed data, then automatically begin outputting the remaining uncompressed data in that block or record.

A four byte Transfer Size counter allows the user to partition the data into blocks of four gigabytes or less to process. Compression Pass Through mode and Decompression Pass Through modes allow data transfers through the device without changing the data. Both the Port A Interface and Port B Interface have a 16-byte FIFO with Almost Empty and Almost Full signal pins and programmable thresholds. Both of the DMA interfaces, Port A and Port B, have programmable wait states in addition to four selectable DMA transfer modes: asynchronous request/acknowledge pair, asynchronous burst mode, and two peripheral access modes that correlate with the two microprocessor modes.

THE ALDC COMPRESSION ALGORITHM

The ALDC (Adaptive Lossless Data Compression) algorithm is one variant of the LZ1 (Lempel-Ziv 1) class of data compression algorithms, first proposed by Abraham Lempel and Jacob Ziv in 1977.

LZ1 algorithms achieve compression by building and maintaining a data structure, called a HISTORYBUFFER. An LZ1 encode process and an LZ1 decode process both initialize this structure to the same known state, and update it in an identical fashion. The encoder does this using the input data it receives for compression, while the decoder generates an identical data stream as its output, which it also uses for the update process.

The compression process consists of examining the incoming data stream to identify any sequences or strings of data bytes which already exist in the encoder history. If an identical such history is available to a decoder, this matching string can be encoded and output as a 2 element COPYPOINTER, containing a byte count and history location. It is then possible for a decoder to reproduce this string exactly, by copying it from the given location in its own history. If the COPYPOINTER can be encoded in fewer bits of information than required for the data string it specifies, compression is achieved.

If an incoming byte of data does not form part of a matching string, a LITERAL, containing this embedded value, is encoded and then output to explicitly represent this byte.

A decoder performs the inverse operation by first parsing a compressed data stream into LITERALS and COPYPOINTERS for processing.

ALDC is a lossless algorithm, insuring that the decompressed data output is exactly the same as the uncompressed data input. QIC-154 Development Standard describes this industry standard algorithm in detail.

PORT A AND PORT B CONFIGURATION

Port A and Port B operate identically. They both are 16-bit bidirectional data ports with parity checking and generation. There are three configuration registers associated with each port and a polarity register that determines the polarity of all of the control signals for that port.

The function of the control pin is determined by either xCNF0[13, 12] bits or *Command* register programmed for peripheral access. The polarity of control signals are controlled by specific bits in the *Polarity* registers.

Table 1: Port A Interface Signals

SIGNAL NAME	*MASTER SLAVE=0*	*SLAVE SLAVE=1*	*APOL bit*	*DIRECTION*
ACIN	DACKA	DREQA	7	I
ACOUT	DREQA	DACKA	5	O
AWR	deasserted	AWR	4	O
ARD	deasserted	ARD	3	O
APCS	APCS	APCS	2	O
AAF	AAF	AAF	1	O
AAE	AAE	AAE	0	O

Table 2: Port B Interface Signals

SIGNAL NAME	*MASTER SLAVE=0*	*SLAVE SLAVE=1*	*BPOL bit*	*DIRECTION*
BCIN	DACKB	DREQB	7	I
BCOUT	DREQB	DACKB	5	O
BWR	deasserted	BWR	4	O
BRD	deasserted	BRD	3	O
BPCS	BPCS	BPCS	2	O
BAF	BAF	BAF	1	O
BAE	BAE	BAE	0	O

SYSTEMS APPLICATIONS

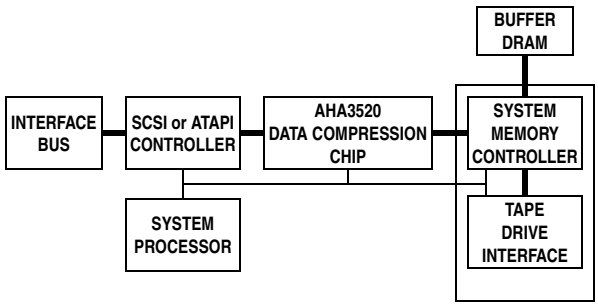
A typical application for the AHA3520 is the implementation of data compression in a tape drive system. An in-line architecture is employed in this system.

The in-line application inserts compression directly between the host and the system data buffer. There is no direct connection between the buffer and the host. For compression, data flows from the host, through the bus controller and into the AHA3520. The data is then compressed by the ALDC engine and flows into the system buffer followed by the tape drive interface. This data flow is usually controlled by a local microprocessor. For decompression, the flow is reversed.

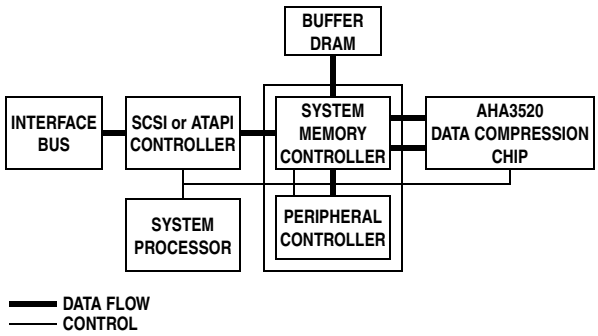
In an in-line architecture the AHA compression chip operates at the data rate of the host interface controller. The AHA3520 device supports a sustained data transfer rate of up to 20 MBytes/sec.

In a look-aside application, the system buffer is in series with the data flow. There is a direct connection between the host and the buffer memory through a DMA port. For compression, data flows from the host, through the bus interface and peripheral controller and into the system buffer. Data then flows from the system buffer into the AHA3520 where it is compressed and sent back to the system buffer. Finally, data is transferred from the system buffer interface. During decompression, this flow is reversed.

EXAMPLE IN-LINE APPLICATION



EXAMPLE LOOK-ASIDE APPLICATION



ORDERING INFORMATION

PART NUMBER	DESCRIPTION
AHA3520A-040 PQC-G	20 MBytes/sec ALDC Data Compression Coprocessor IC

ABOUT AHA

Comtech AHA Corporation (AHA) develops and markets superior integrated circuits, boards, and intellectual property core technology for communications systems architects worldwide. AHA has been setting the standard in Forward Error Correction and Lossless Data Compression technology for many years and provides flexible, cost-effective solutions for today's growing bandwidth and reliability challenges. Comtech AHA Corporation is a wholly owned subsidiary of Comtech Telecommuncations Corp. (NASDAQ: CMTL). For more information, visit www.aha.com.

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