



**ANO110N, ANO120N
ANO130N, ANO140N**

**N-CHANNEL ENHANCEMENT MODE D-MOS FETs
8-CHANNEL ARRAYS**

T. 43-25

ORDERING INFORMATION

18 Pin Plastic DIP	ANO110NA	ANO120NA	ANO130NA	ANO140NA
Description (each channel)	100V,100Ω	200V,300Ω	300V,300Ω	400V,350Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <800pA
- High Channel-to-Channel Isolation
- 100V to 400V Capability
- Industry Standard Pin-Out

APPLICATIONS

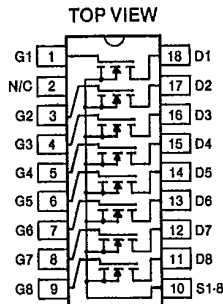
- Electrostatic Array Drivers
- Electroluminescent Panel Drivers
- Converters
- Multi-Channel Array Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C per channel unless otherwise specified)

Drain-Source Voltage	
ANO110N	+100V
ANO120N	+200V
ANO130N	+300V
ANO140N	+400V
Drain-Gate Voltage (V_{GS}=0)	
ANO110N	+100V
ANO120N	+200V
ANO130N	+300V
ANO140N	+400V
Channel-to-Channel Isolation Voltage	
Drain-to-Drain Voltage (V_{GS}=0)	
ANO110N	+100V
ANO120N	+200V
ANO130N	+300V
ANO140N	+400V
Gate-Source Voltage	
±30V	
Operating and Storage Temperature Range	
-55 to +85°C	
Lead Temperature (1/16" from mounting Surface for 10 sec.)	
+300°C	

Continuous Drain Current, Total Package		
	T _A = +25°C	T _C = +25°C
ANO110N	80mA	140mA
ANO120N, ANO130N	50mA	80mA
ANO140N	40mA	75mA
Continuous Drain Current, Single Channel		
	T _A = +25°C	T _C = +25°C
ANO110N	50mA	100mA
ANO120N, ANO130N	30mA	60mA
ANO140N	25mA	50mA
Continuous Device Dissipation		
	T _A = +25°C	T _C = +25°C
Total Package	.64W	2.0W
Single Channel	.30W	1.0W
Linear Derating Factor		
	T _A = +25°C	T _C = +25°C
Total Package	10.67mW/°C	33.2mW/°C
Single Channel	5mW/°C	16.6mW/°C

PIN CONFIGURATION & SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS

18-Pin Plastic DIP
(See Package 11)



**ANO110N, ANO120N
ANO130N, ANO140N**

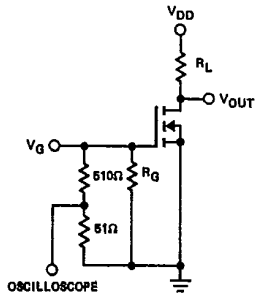
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ per channel unless otherwise noted)

T-43-25

#	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS		
1	BV _{DSS}	Drain-Source Breakdown Voltage	AN0110	100	160	V	I _D = 100μA, V _{GS} = 0		
2			AN0120	200	300				
3			AN0130	300	400				
4			AN0140	400	450				
5	I _{DSS}	Drain-Source OFF Leakage Current	AN0110		5.0	nA	V _{DS} = 80V V _{GS} = 0 (NOTE 1)		
6			AN0120		5.0				
7			AN0130		5.0				
8			AN0140		5.0				
9	I _{GBS}	Gate-Body Leakage Current			10	nA	V _{GS} = 20V, V _{DS} = 0		
10			V _{GS(th)}	Gate-Source Threshold Voltage	2.0				5.0
11	r _{DS(on)}	Drain-Source ON Resistance	AN0110	60	100	ohms	I _D = 10mA, V _{GS} = 10V		
12			AN0120	210	300				
13			AN0130	260	300				
14			AN0140	325	350				
15	I _{D(on)}	Drain-Source ON Current	AN0110	50		mA	V _{DS} = 25V, V _{GS} = 10V		
16			AN0120	25					
17			AN0130	25					
18			AN0140	25					
19	g _{fs}	Common-Source Forward Transcond	AN0110	8.0		mmhos	V _{DS} = 25V, I _D = 10mA, f = 1KHz		
20			AN0120	4.0					
21			AN0130	4.0					
22			AN0140	4.0					
23	C _{iss}	Common-Source Input Capacitance		8.0	10	pF	V _{DS} = 25V, V _{GS} = 0, f = 1MHz		
24			C _{oss}	Common-Source Output Capacitance				1.5	2.0
25			C _{rss}	Common-Source Reverse Transfer Capacitance				0.8	1.0
26			t _{d(on)}	Turn-ON Delay Time				3	
27	t _r	Rise Time		3					
28	t _{d(off)}	Turn-OFF Delay Time		5					
29	t _f	Fall Time		5					

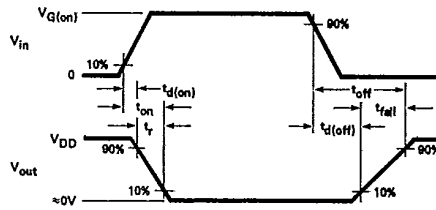
Note 1: Limit is OFF leakage of all 8 segments in parallel.

SWITCHING TIMES TEST CIRCUIT



INPUT PULSE
 $t_r < 0.5 \text{ nSEC}$
 PULSE WIDTH - 100 nSEC
 SAMPLING OSCILLOSCOPE
 $t_r < 0.38 \text{ nSEC}$
 $R_{in} > 1M\Omega$
 $C_{in} < 2.0 \text{ pF}$

TEST WAVEFORMS

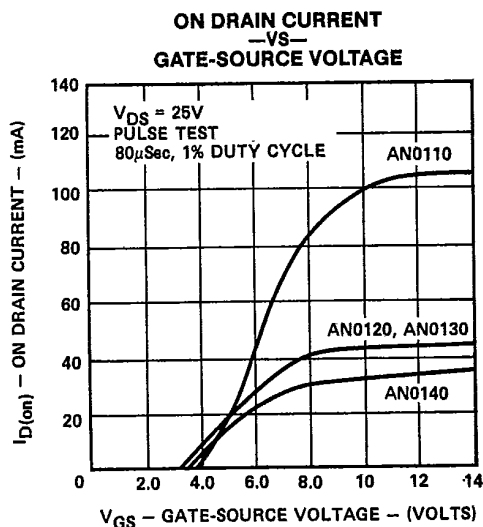
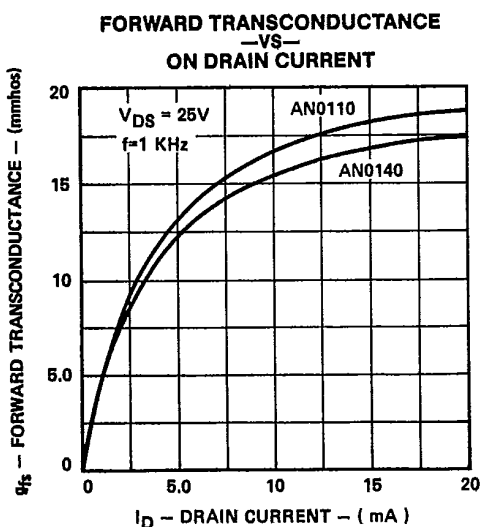
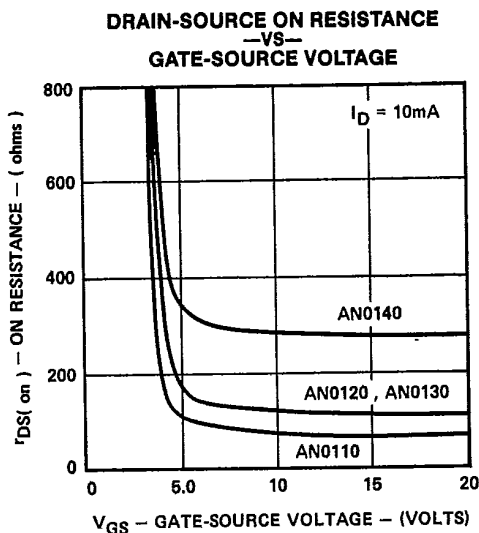
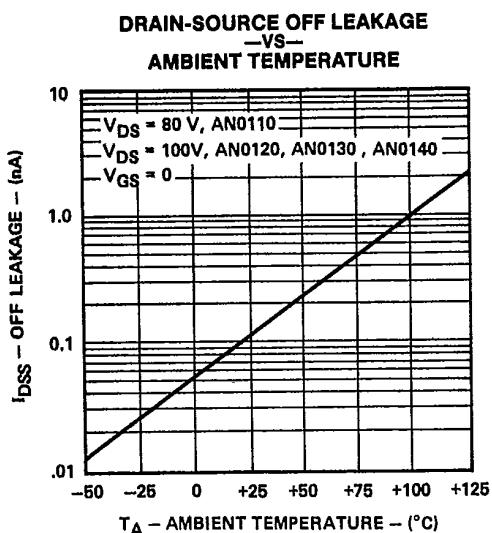




**ANO110N, ANO120N
ANO130N, ANO140N**

T-43.25

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)



TOPAZ

SEMICONDUCTOR

T-43-25

AP0120N, AP0130N, AP0140N

P-CHANNEL ENHANCEMENT MODE D-MOS FETs 8-CHANNEL ARRAYS

ORDERING INFORMATION

18 Pin Plastic DIP	AP0120NA	AP0130NA	AP0140NA
Description (each channel)	-200V, 600Ω	-300V, 600Ω	-400V, 700Ω

FEATURES

- Ultra-Low Channel OFF Leakage, <-800pA
- High Channel-to-Channel Isolation
- N-Channel Complements available
- Industry Standard Pin-Out

APPLICATIONS

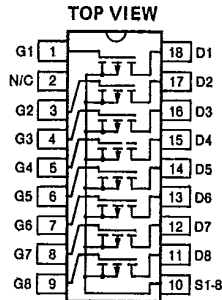
- Electrostatic Array Drivers
- Electroluminescent Panel Drivers
- Converters
- Multi-Channel Array Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C per channel, unless otherwise specified)

Drain-Source Voltage	
AP0120N	-200V
AP0130N	-300V
AP0140N	-400V
Drain-Gate Voltage (V _{GS} = 0)	
AP0120N	-200V
AP0130N	-300V
AP0140N	-400V
Channel-to-Channel Isolation Voltage	
Drain-to-Drain Voltage (V _{GS} = 0)	
AP0120N	-200V
AP0130N	-300V
AP0140N	-400V
Gate-Source Voltage	±40V
Operating and Storage Temperature	
Range	-55 to +85°C
Lead Temperature (1/16" from mounting	
Surface for 10 sec.)	+300°C

Continuous Drain Current, Total Package		
	T _A = +25°C	T _C = +25°C
AP0120N, AP0130N	-25mA	-40mA
AP0140N	-20mA	-35mA
Continuous Drain Current, Single Channel		
	T _A = +25°C	T _C = +25°C
AP0120N, AP0130N,		
AP0140N	-15mA	-25mA
Continuous Device Dissipation		
	T _A = +25°C	T _C = +25°C
Total Package	.64W	2.0W
Single Channel	.30W	1.0W
Linear Derating Factor		
	T _A = +25°C	T _C = +25°C
Total Package	10.67mW/°C	33.2mW/°C
Single Channel	5mW/°C	16.6mW/°C

PIN CONFIGURATION & SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS

18-Pin Plastic DIP
(See Package 11)

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AP0120N, AP0130N, AP0140N

ELECTRICAL CHARACTERISTICS (T_A = +25°C per channel unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
1	B _{V(DSS)}	Drain-Source Breakdown Voltage	AP0120N	-200		V	I _D = -100μA, V _{GS} = 0	
2			AP0130N	-300				
3			AP0140N	-400				
4	I _{LOSS}	Drain-Source OFF Leakage Current			-5.0	nA	V _{DS} = -100V, V _{GS} = 0 (NOTE 1)	
5	I _{GSS}	Gate-Body Leakage Current			±10	nA	V _{GS} = ±20V, V _{DS} = 0	
6					±1.0	μA	V _{GS} = ±40V, V _{DS} = 0	
7	V _{GS(th)}	Gate-Source Threshold Voltage	-2.0		-5.0	V	V _{DS} = V _{GS} , I _D = -0.5mA	
8	r _{DS(on)}	Drain-Source ON Resistance	AP0120N, AP0130N		600	ohms	I _D = -10mA, V _{GS} = -10V	
9			AP0140N		700			
10	I _{D(on)}	Drain-Source ON Current	-15			mA	V _{DS} = -25V, V _{GS} = -10V	
11	g _{fs}	Common-Source Forward Transconductance	3.0			mmhos	V _{DS} = -25V, I _D = -5mA f = 1KHz	
12		C _{iss}	Common-Source Input Capacitance		8.0	10	pF	V _{DS} = -25V, V _{GS} = 0, f = 1MHz
13		C _{oss}	Common-Source Output Capacitance		1.5	2.0		
14			Common-Source Reverse Transfer Capacitance		0.8	1.0		
15		t _{d(on)}	Turn-ON Delay Time		6		nS	V _{DD} = -25V, V _{GS(on)} = -10V R _L = 500Ω R _G = 51Ω
16	t _r	Rise time		6				
17	t _{d(off)}	Turn-OFF Delay Time		8				
18	t _f	Fall Time		6				

Note 1: Limit is OFF leakage of all 8 segments in parallel.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$, per channel, unless otherwise specified)

