Complete, Quad, 16-Bit, High Accuracy, Serial Input, Bipolar Voltage Output DAC

Preliminary Technical Data

AD5764

FEATURES

Complete quad 16-bit D/A converter
Programmable output range: ±10 V, ±10.25 V, or ±10.5 V
±1 LSB max INL error, ±1 LSB max DNL error
Low noise : 60 nV/√Hz
Settling time: 10µs max
Integrated reference buffers
Internal reference, 10 ppm/°C
On-chip temp sensor, ±5°C accuracy
Output control during power-up/brownout
Programmable short-circuit protection
Simultaneous updating via LDAC
Asynchronous $\overline{CLR}$ to zero code
Digital offset and gain adjust
Logic output control pins
DSP/microcontroller compatible serial interface
Temperature range:–40°C to +85°C
***i*CMOS™ Process Technology**

APPLICATIONS

Industrial automation
Closed-loop servo control, process control
Data acquisition systems
Automatic Test Equipment
Automotive test and measurement
High accuracy instrumentation

GENERAL DESCRIPTION

The AD5764 is a quad, 16-bit serial input, voltage output digital-to analog converter that operates from supply voltages of ±12 V up to ±15 V. Nominal full-scale output range is ±10 V, provided are integrated output amplifiers, reference buffers, internal reference, and proprietary power-up/power-down control circuitry. It also features a digital I/O port that may be programmed via the serial interface, and an analog temperature sensor. The part incorporates digital offset and gain adjust registers per channel.

The AD5764 is a high performance converter that offers guaranteed monotonicity, integral nonlinearity (INL) of ±1 LSB, low noise and 10 µs settling time and includes an on-chip 5 V reference with a reference tempco of 10 ppm/°C max. During power-up (when the supply voltages are changing), Vout is clamped to 0V via a low impedance path.

The AD5764 uses a serial interface that operates at clock rates up to 30 MHz and is compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is programmable to either twos complement or straight binary formats. The asynchronous clear function clears all DAC registers to either bipolar zero or zero-scale depending on the coding used. The AD5764 is ideal for both closed-loop servo control and open-loop control applications. The AD5764 is available in a 32-lead TQFP package, and offers guaranteed specifications over the –40°C to +85°C industrial temperature range. See functional block diagram, Figure 1.

*i*CMOS™ Process Technology
For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30V and operating at +/-15V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.

Rev. PrC **21-Oct-04**

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REVISION HISTORY

Revision PrC 21-Oct-04: Preliminary Version

FUNCTIONAL BLOCK DIAGRAM

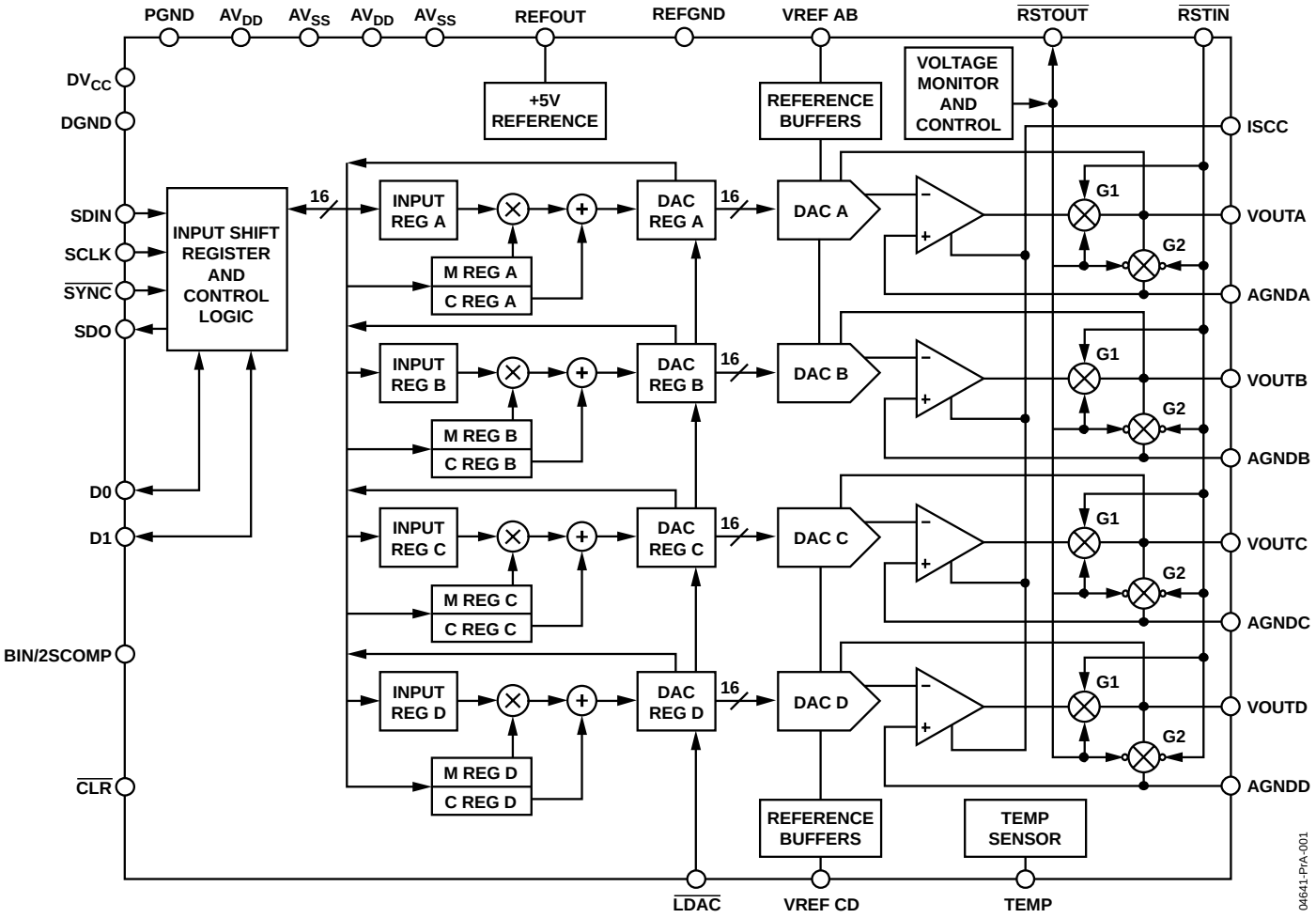

Figure 1. Functional Block Diagram

SPECIFICATIONS

AV_{DD} = +11.4 V to +15.75 V, AV_{SS} = −11.4 V to −15.75 V, AGND = DGND = REFGND = PGND=0 V; REFAB = REFCD= 5 V Ext; DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 10 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Grade[1]	B Grade[1]	C Grade[1]	Unit	Test Conditions/Comments
ACCURACY					
Resolution	16	16	16	Bits	
Relative Accuracy (INL)	±4	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic
Bipolar Zero Error	±1	±1	±1	mV max	At 25°C. Error at other temperatures obtained using bipolar zero TC.
Bipolar Zero TC	±2	±2	±2	ppm FSR/°C max	
Zero Code Error	±1	±1	±1	mV max	At 25°C. Error at other temperatures obtained using zero code TC.
Zero Code TC	±2	±2	±2	ppm FSR/°C max	
Gain Error	±0.02	±0.02	±0.02	% FSR max	At 25°C. Error at other temperatures obtained using gain TC.
Gain TC	2	2	2	ppm FSR/°C max	
DC Crosstalk[2]	0.5	0.5	0.5	LSB max	
REFERENCEINPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage	5	5	5	V nom	±1% for specified performance
DC Input Impedance	1	1	1	MΩ min	Typically 100 MΩ
Input Current	±10	±10	±10	µA max	Typically ±30 nA
Reference Range	1/5	1/5	1/5	V min/max	
Reference Output					
Output Voltage	4.999/5.001	4.999/5.001	4.999/5.001	V min/max	At 25°C
Reference TC	±10	±10	±10	ppm/°C max	
	±3	±3	±3	Ppm/°C typ	
Output Noise(0.1 Hz to 10 Hz)	TBD	TBD	TBD	µV p-p typ	
Noise Spectral Density	TBD	TBD	TBD	nV/$\sqrt{Hz}$ typ	
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range[3]	±10	±10	±10	V min/max	AV_{DD}/AV_{SS} = ±11.4 V
	±13	±13	±13	V min/max	AV_{DD}/AV_{SS} = ±14.75 V
Output Voltage TC	±2	±2	±2	ppm FSR/°C max	
Output Voltage Drift V_S Time	±TBD	±TBD	±TBD	ppm FSR/1000 Hours typ	
Short Circuit Current	10	10	10	mA max	RI_{SCC} = 6 KΩ , See Figure ???
Load Current	±1	±1	±1	mA max	
Capacitive Load Stability					
R_L = ∞	200	200	200	pF max	
R_L = 10 kΩ	TBD	TBD	TBD	pF max	
DC Output Impedance	0.3	0.3	0.3	Ω max	

[1] Temperature range −40°C to +85°C; typical at +25°C. Device functionality is guaranteed to +105°C with degraded performance.
[2] Guaranteed by characterization. Not production tested.
[3] Output amplifier headroom requirement is 1.4 V min.

Parameter	A Grade[1]	B Grade[1]	C Grade[1]	Unit	Test Conditions/Comments
DIGITAL INPUTS[2]					DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2	2	2	V min	
V_{IL}, Input Low Voltage	0.8	0.8	0.8	V max	
Input Current	±10	±10	±10	µA max	Total for All Pins. $T_A = T_{MIN}$ to T_{MAX}.
Pin Capacitance	10	10	10	pF max	
DIGITAL OUTPUTS (D0,D1, SDO) [2]					
Output Low Voltage	0.4	0.4	0.4	V max	DV_{CC}= 5 V ± 10%, sinking 200 µA
Output High Voltage	DV_{CC} – 1	DV_{CC} – 1	DV_{CC} – 1	V min	DV_{CC} = 5 V ± 10%, Sourcing 200 µA
Output Low Voltage	0.4	0.4	0.4	V max	DV_{CC} = 2.7 V to 3.6 V, Sinking 200 µA
Output High Voltage	DV_{CC} – 0.5	DV_{CC} – 0.5	DV_{CC} – 0.5	V min	DV_{CC} = 2.7 V to 3.6 V, Sourcing 200 µA
High Impedance Leakage Current	±1	±1	±1	µA max	SDO only
High Impedance Output Capacitance	5	5	5	pF typ	SDO only
TEMP SENSOR					
Accuracy	±1	±1	±1	°C typ	At 25°C
	±5	±5	±5	°C max	–40°C < T <+85°C
Output Voltage @ 25°C	1.5	1.5	1.5	V typ	
Output Voltage Scale Factor	5	5	5	mV/°C typ	
Output Voltage Range	0/3.0	0/3.0	0/3.0	V min/max	
Output Load Current	200	200	200	µA max	Current source only.
Power On Time	10	10	10	ms typ	To within ±5°C
POWER REQUIREMENTS					
AV_{DD}/AV_{SS}	11.4/15.75	11.4/15.75	11.4/15.75	V min/max	
DV_{CC}	2.7/5.5	2.7/5.5	2.7/5.5	V min/max	
Power Supply Sensitivity[4]					
$\Delta V_{OUT}/\Delta AV_{DD}$	–85	–85	–85	dB typ	
AI_{DD}	3.75	3.75	3.75	mA/Channel max	Outputs unloaded
AI_{SS}	2.75	2.75	2.75	mA/Channel max	Outputs unloaded
DI_{CC}	1	1	1	mA max	$V_{IH} = DV_{CC}$, V_{IL} = DGND. TBD mA typ
Power Dissipation	244	244	244	mW typ	±12 V operation output unloaded

[4] Guaranteed by characterization. Not production tested.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = +11.4 V to +15.75 V, AV_{SS} = −11.4 V to −15.75 V, AGND = DGND = REFGND = PGND=0 V; REFAB = REFCD= 5 V Ext; DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 10 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization, not production tested.

Table 2.

Parameter	A Grade	B Grade	C Grade	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time	8	8	8	µs typ	Full-scale step
	10	10	10	µs max	
	1	1	1	µs max	512 LSB step settling
Slew Rate	5	5	5	V/µs typ	
Digital-to-Analog Glitch Energy	5	5	5	nV-s typ	
Glitch Impulse Peak Amplitude	5	5	5	mV max	
Channel-to-Channel Isolation	100	100	100	dB typ	
DAC-to-DAC Crosstalk	5	5	5	nV-s typ	
Digital Crosstalk		5	5	nV-s typ	
Digital Feedthrough		1	1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise (0.1 Hz to 10 Hz)		0.1	0.1	LSB p-p typ	
Output Noise (0.1 kHz to 100 kHz)[5]		45	45	µV rms max	
1/f Corner Frequency		1	1	kHz typ	
Output Noise Spectral Density		60	60	nV/$\sqrt{Hz}$ typ	Measured at 10 kHz
Complete System Output Noise Spectral Density[6]		80	80	nV/$\sqrt{Hz}$ typ	Measured at 10 kHz

[5] Guaranteed by design and characterization. Not production tested.
[6] Includes noise contributions from integrated reference buffers, 16-bit DAC and output amplifier.

TIMING CHARACTERISTICS

AV_{DD} = +11.4 V to +15.75 V, AV_{SS} = −11.4 V to −15.75 V, AGND = DGND = REFGND = PGND = 0 V; REFAB = REFCD= 5 V Ext; DV_{CC} = 2.7 V to 5.5 V, R_{LOAD} = 10 kΩ, C_L = 200 pF. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[7,8,9]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time
t_5 [10]	13	ns min	24th SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_6	40	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_7	5	ns min	Data setup time
t_8	0	ns min	Data hold time
t_9	20	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge
t_{10}	20	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{11}	5	ns min	$\overline{\text{LDAC}}$ falling edge to DAC output response time
t_{12}	10	µs max	DAC output settling time
t_{13}	20	ns min	$\overline{\text{CLR}}$ pulse width low
t_{14}	12	µs max	$\overline{\text{CLR}}$ pulse activation time
t_{15}[11,12]	20	ns max	SCLK rising edge to SDO valid
t_{16}[12]	8	ns min	$\overline{\text{SCLK}}$ falling edge to SYNC rising edge
t_{17}[12]	20	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge

[7] Guaranteed by design and characterization. Not production tested.
[8] All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[9] See Figure 2, Figure 3, and Figure 4.
[10] Stand-alone mode only.
[11] Measured with the load circuit of Figure 5.
[12] Daisy-chain mode only.

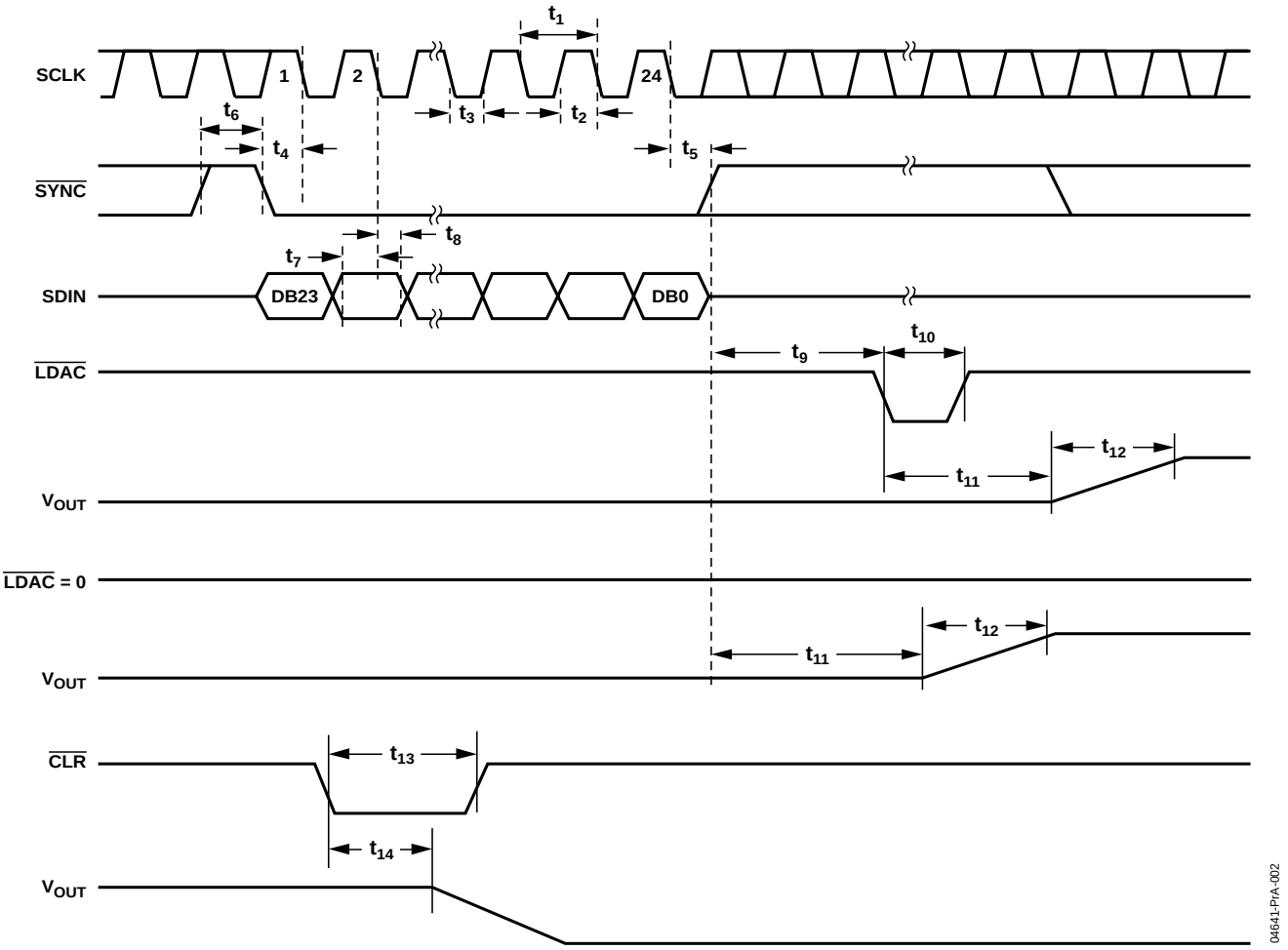

Figure 2. Serial Interface Timing Diagram

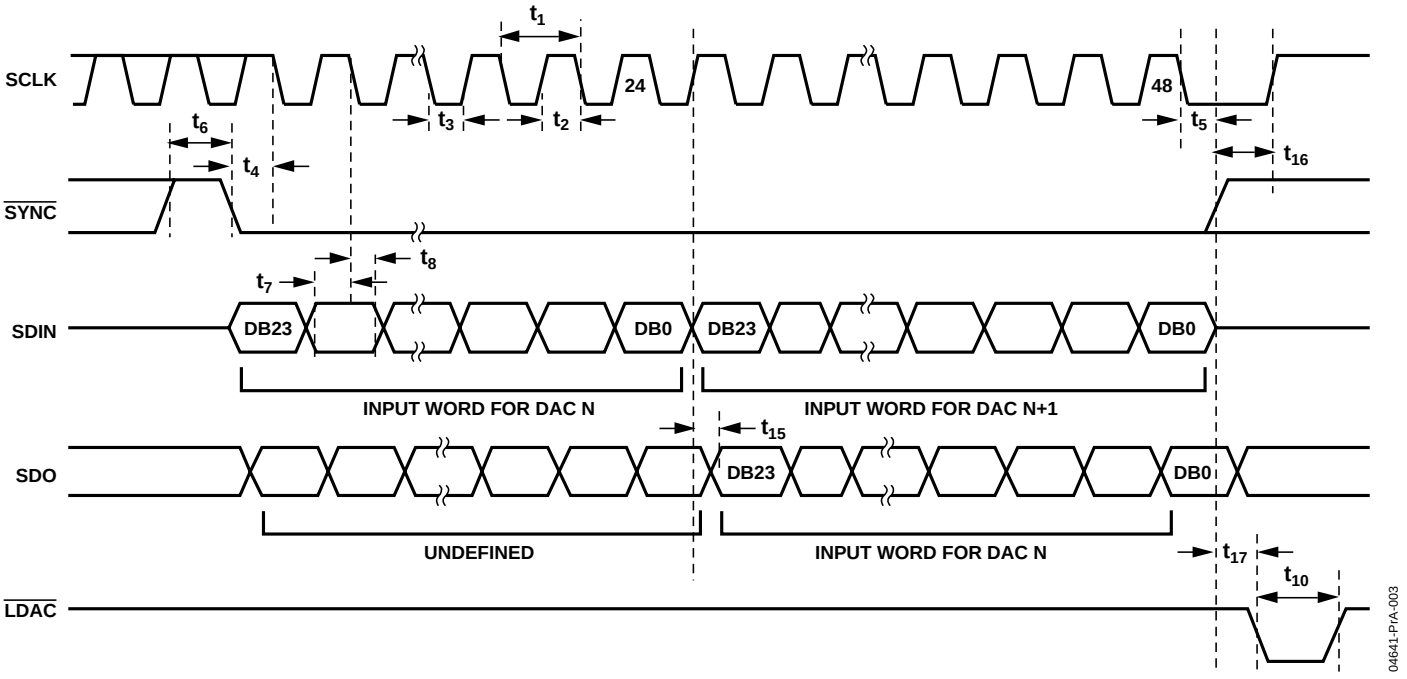

Figure 3. Daisy Chain Timing Diagram

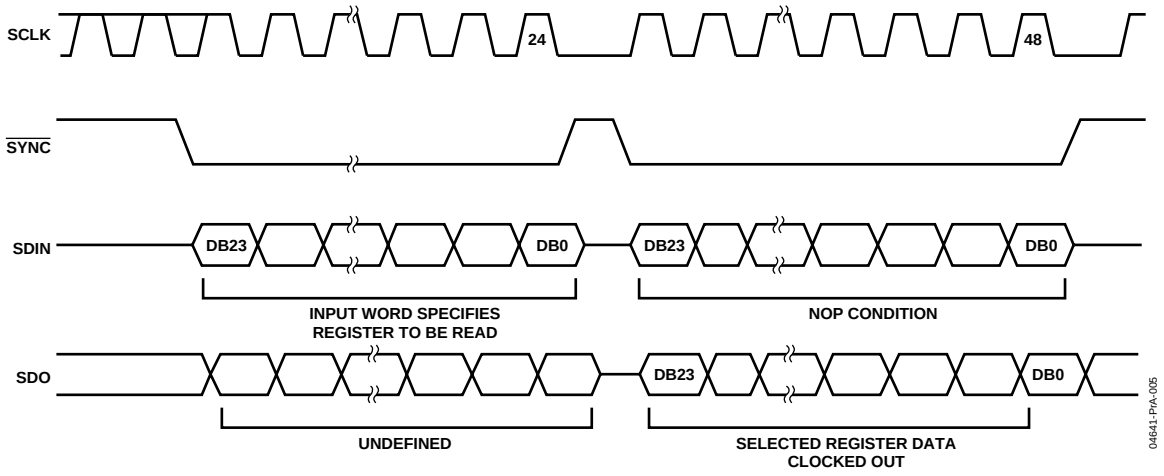

Figure 4. Readback Timing Diagram

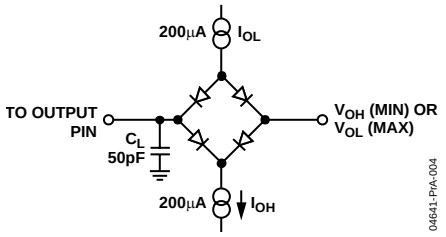

Figure 5. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.
Transient currents of up to 100 mA will not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3 V to +17 V
AV_{SS} to AGND, DGND	+0.3 V to −17 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V
REF IN to AGND, PWRGND	−0.3 V to +17 V
REF OUT to AGND	AV_{SS} to AV_{DD}
V_{OUT}A,B,C,D to AGND	AV_{SS} to AV_{DD}
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
32-Lead TQFP Package,	TBD°C/W
θ_{JA} Thermal Impedance	
Reflow Soldering	
Peak Temperature	220°C
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

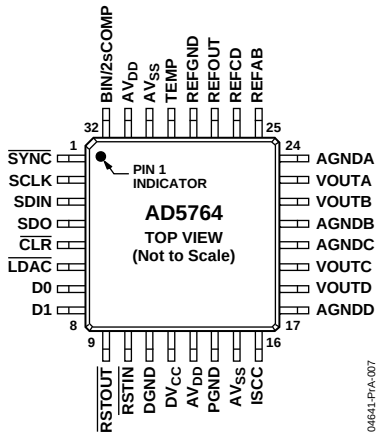

Figure 6. 32-Lead TQFP Pin Configuration Diagram

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	$\overline{\text{SYNC}}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK.
2	SCLK[13]	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
3	SDIN[13]	Serial Data Input. Data must be valid on the falling edge of SCLK.
4	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode.
5	$\overline{\text{CLR}}$[13]	Active Low Input. Asserting this pin sets the DAC registers to 0x0000.
6	$\overline{\text{LDAC}}$	Load DAC. Logic input. This is used to update the DAC registers and consequently the analog output. When tied permanently low, the addressed DAC register is updated on the 24th clock of the serial register write. If $\overline{\text{LDAC}}$ is held high during the write cycle, the DAC input register is updated but the output is held off until the falling edge of $\overline{\text{LDAC}}$. In this mode, all analog outputs can be updated simultaneously on the falling edge of $\overline{\text{LDAC}}$.
7, 8	D0, D1	D0 and D1 form a digital I/O port. The user can configure these pins as inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, these pins have weak internal pull-ups to DV_{CC}.
9	$\overline{\text{RSTOUT}}$	Reset Logic Output. This is the output from the on-chip voltage monitor used in the reset circuit. If desired, it may be used to control other system components.
10	$\overline{\text{RSTIN}}$	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input resets the DAC output to 0 V. In normal operation, $\overline{\text{RSTIN}}$ should be tied to Logic 1.
11	DGND	Digital GND Pin.
12	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V. When programmed as outputs, D0 and D1 are referenced to DV_{CC}.
13, 31	AV_{DD}	Positive Analog Supply Pins. Voltage ranges from 11.4 V to 15.75 V.
14	PGND	Ground Reference Point for Analog Circuitry.
15, 30	AV_{SS}	Negative Analog Supply Pins. Voltage ranges from –11.4 V to –15.75 V.
16	ISCC	This pin us used in association with an external resistor to AGND to program the short-circuit current of the output amplifiers.
17	AGNDD	Ground Reference Pin for DAC D Output amplifier.

[13] Internal pull-up device on this logic input. Therefore, it can be left floating and will default to a logic high condition.

Pin No.	Mnemonic	Function
18	VOUTD	Analog Output Voltage of DAC D. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
19	VOUTC	Analog Output Voltage of DAC C. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
20	AGNDC	Ground Reference Pin for DAC C Output Amplifier.
21	AGNDB	Ground Reference pin for DAC B Output Amplifier.
22	VOUTB	Analog Output Voltage of DAC B. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
23	VOUTA	Analog Output Voltage of DAC A. Buffered output with a nominal full-scale output range of ±10 V. The output amplifier is capable of directly driving a 10 kΩ, 200 pF load.
24	AGNDA	Ground Reference Pin for DAC A Output Amplifier.
25	REFAB	External Reference Voltage Input for Channels A and B. Reference input range is 1 V to 5 V; programs the full-scale output voltage. REFIN = 5 V for specified performance.
26	REFCD	External Reference Voltage Input for Channels C and D. Reference input range is 1 V to 5 V; programs the full-scale output voltage. REFIN = 5 V for specified performance.
27	REFOUT	Reference Output. This is the buffered reference output from the internal voltage reference. The internal reference is 5 V ± 1 mV, with a reference tempco of 10 ppm/°C.
28	REFGND	Reference Ground Return for the Reference Generator and Buffers.
29	TEMP	This pin provides an output voltage proportional to temperature. The output voltage is 750 mV typical at 25°C; variation with temperature is 10 mV/°C.
32	BIN/$\overline{\text{2sCOMP}}$	Determines the DAC Coding. When set to a logic high, input coding is offset binary; 0x0000 outputs negative full-scale and 0xFFFF outputs positive full-scale. Invoking a $\overline{\text{CLR}}$ in this mode sets the output to negative full-scale. When set to a logic low, input coding is twos complement; 0x8000 outputs negative full-scale, 0x0000 outputs 0V, and 0x7FFF outputs positive full-scale. Invoking a $\overline{\text{CLR}}$ in this mode sets the output to 0 V.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure ?.

Differential Nonlinearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure ?.

Monotonicity

A DAC is monotonic, if the output either increases or remains constant for increasing digital input code. The AD5764 is monotonic over its full operating temperature range

Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (Straight Binary coding) or 0x0000 (2sComplement coding)

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFFF Hex) is loaded to the DAC register. Ideally the output should be programmed full scale value – 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure ?.

Negative Full-Scale Error / Zero Scale Error

Negative full-scale error is the error in the DAC output voltage when 0x0000 (Straight Binary coding) or 0x8000 (2sComplement coding) is loaded to the DAC register. Ideally the output voltage should be programmed negative full scale value – 1 LSB.

Output Voltage Settling Time

Output voltage settling time is the amount od time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate

The slew rate of a device is a limatation in the rate of change of the output voltage. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifierused at its output. Slew rate is measured from 10% to 90% of the output signal and is given in Vμs.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error

Total Unadjusted Error (TUE) is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure ?.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FFF Hex to 8000 Hex). See Figure ?.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

Power Supply Sensitivity

Power supply sensitivity indicates how the output of the DAC is affected by changes in the power supply voltage.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in μV.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC

due to a digital code changeand subsequent output change of another DAC. This includes both digital and anlalog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with /LDAC low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Channel-to-Channel Isolation

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

TYPICAL PERFORMANCE CHARACTERISTICS

GENERAL DESCRIPTION

The AD5764 is a quad 16-bit, serial input, bipolar voltage output DAC. It operates from supply voltages of ±11.4 V to ±16.5 V and has a buffered output voltage of up to ± 10.25 V. Data is written to the AD5764 in a 24-bit word format, via a 3-wire serial interface. The device also offers an SDO pin, which is available for daisy chaining or readback.

The AD5764 incorporates a power-on reset circuit, which ensures that the DAC outputs power up to 0V. The AD5764 also features a digital I/O port that may be programmed via the serial interface, an analog temperature sensor, on-chip 10 ppm/°C voltage reference, on-chip reference buffers and per channel digital gain and offset registers.

DAC ARCHITECTURE

The DAC architecture of the AD5764 consists of a 16-bit current-mode segmented R-2R DAC. The simplified circuit diagram for the DAC section is shown in Figure 13.

The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of the 15 matched resistors to either AGND or IOUT. The remaining 12 bits of the data word drive switches S0 to S11 of the 12-bit R-2R ladder network.

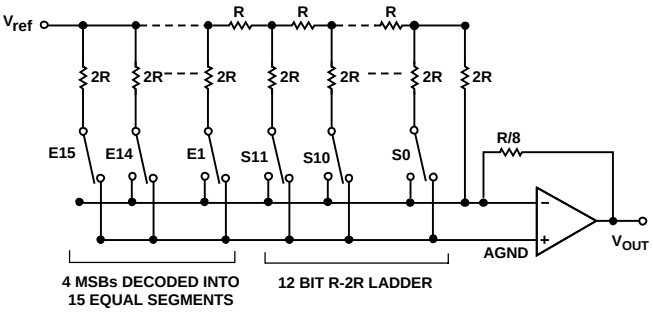

Figure 7. DAC Ladder Structure

REFERENCE BUFFERS

The AD5764 can operate with either an external or internal reference. The reference inputs (REFAB and REFCD) have an input range up to 5 V. This input voltage is then used to provide a buffered positive and negative reference for the DAC cores. The positive reference is given by

$$+ V_{REF} = 2^* V_{REF}$$

While the negative reference to the DAC cores is given by

$$-V_{REF} = -2^*V_{REF}$$

These positive and negative reference voltages (along with the gain register values) define the output ranges of the DACs.

SERIAL INTERFACE

The AD5764 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of a read/write bit, three register select bits, three DAC address bits and 16 data bits as shown in Table 6. The timing diagram for this operation is shown in Figure 2.

Upon power-up the DAC registers are loaded with zero code (0x0000). The corresponding output voltage depends on the state of the BIN/2sCOMP pin. If the BIN/2sCOMP pin is tied to DGND then the data coding is 2sComplement and the outputs will power-up to 0V. If the BIN/2sCOMP pin is tied high then the data coding is straight binary and the outputs will power-up to Negative Full-scale.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{\text{SYNC}}$ is brought back high again; if $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, the write is aborted. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, the input data will be corrupted. The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. In order for another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the input register of the addressed DAC.

When the data has been transferred into the input register of the addressed DAC, all DAC registers and outputs can be updated by taking $\overline{\text{LDAC}}$ low while $\overline{\text{SYNC}}$ is high.

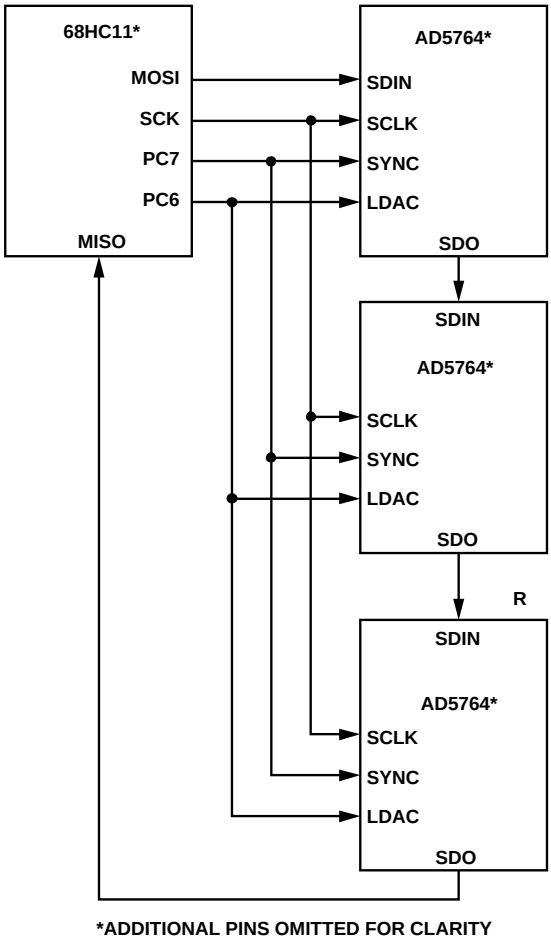

Figure 8. Daisy chaining the AD5764

Daisy-Chain Operation

For systems that contain several devices, the SDO pin may be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the DIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24N, where N is the total number of AD5764s in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock may be a continuous or a gated clock. A continuous SCLK source can only be used if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Readback Operation

Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit = 1 in the serial input register write. With R/$\overline{\text{W}}$ = 1, Bits A2–A0, in association with Bits REG2 , REG1, and REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output will contain the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. The readback diagram in Figure 4 shows the readback sequence. For example, to read back the fine gain register of Channel A on the AD5764, the following sequence should be implemented. First, write 0xA0XXXX to the AD5764 input register. This configures the AD5764 for read mode with the fine gain register of Channel A selected. Note that all the data bits, D15 to D0, are don't cares. Follow this with a second write, a NOP condition, 0x00XXXX. During this write, the data from the fine gain register is clocked out on the SDO line, i.e., data clocked out will contain the data from the fine gain register in Bits D5 to D0.

SIMULTANEOUS UPDATING VIA $\overline{\text{LDAC}}$

After data has been transferred into the input register of the DACs, there are two ways in which the DAC registers and DAC outputs can be updated. Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, one of two update modes is selected.

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low any time after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

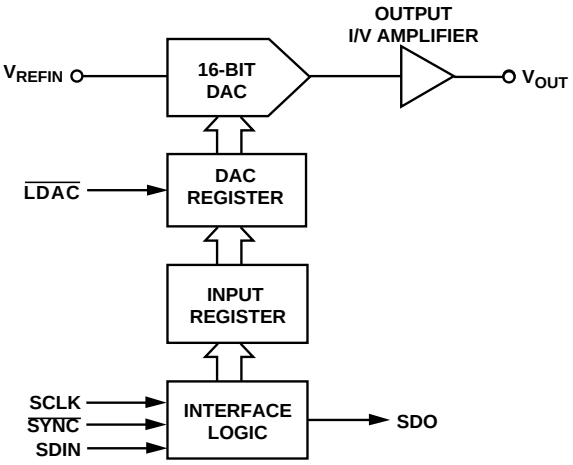

Figure 9. Simplified Serial Interface showing input loading circuitry for one DAC Channel

TRANSFER FUNCTION

Table ? Shows the ideal input code to output voltage relationship for the AD5764 for both straight binary and twos complement data coding.

Digital Input				Analog Output
Straight Binary Data Coding				
MSB			**LSB**	**V_{OUT}**
1111	1111	1111	1111	+2 V_{REF} x (32767/32768)
1000	0000	0000	0001	+2 V_{REF} x (1/32768)
1000	0000	0000	0000	0 V
0111	1111	1111	1111	-2 V_{REF} x (1/32768)
0000	0000	0000	0000	-2 V_{REF} x (32767/32768)
Twos Complement Data Coding				
MSB			**LSB**	**V_{OUT}**
0111	1111	1111	1111	+2 V_{REF} x (32767/32768)
0000	0000	0000	0001	+2 V_{REF} x (1/32768)
0000	0000	0000	0000	0 V
1111	1111	1111	1111	-2 V_{REF} x (1/32768)
1000	0000	0000	0000	-2 V_{REF} x (32767/32768)

The output voltage expression is given by

$$V_{OUT} = -2 \times V_{REFIN} + 4 \times V_{REFIN} \left[\frac{D}{65536} \right]$$

where:
D is the decimal equivalent of the code loaded to the DAC.
V_{REFIN} is the reference voltage applied at the REFIN pin.

ASYNCHRONOUS CLEAR ($\overline{CLR}$)

$\overline{CLR}$ is an active low, level sensitive clear that allows the outputs to be cleared to either 0 V (straight binary coding) or negative full scale (twos complement coding). It is necessary to maintain $\overline{CLR}$ low for a minimum amount of time (refer to Figure 3) for the operation to complete. When the $\overline{CLR}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The $\overline{CLR}$ signal has priority over $\overline{LDAC}$ and $\overline{SYNC}$. A clear can also be initiated through software by writing the command 0x04XXXX to the AD5764.

Table 6. Input Register Format

MSB																						LSB
R/$\overline{W}$	0	REG2	REG1	REG0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 7. Input Register Bit Functions

R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
REG2, REG1, REG0	Used in association with the address bits to determine if a read or write operation is to the data register, offset register, gain register, or function register.			
	REG2	**REG1**	**REG0**	**Function**
	0	0	0	Function Register
	0	1	0	Data Register
	0	1	1	Coarse Gain Register
	1	0	0	Fine Gain Register
	1	0	1	Offset Register
A2, A1, A0	These bits are used to decode the DAC channels			
	A2	**A1**	**A0**	**Channel Address**
	0	0	0	DAC A
	0	0	1	DAC B
	0	1	0	DAC C
	0	1	1	DAC D
	1	0	0	ALL DACs
D15 – D0	Data Bits			

FUNCTION REGISTER

The Function Register is addressed by setting the three REG bits to 000. The values written to the address bits and the data bits determine the function addressed. The Functions available through the function register are shown in Table 8 and Table 9.

Table 8. Function Register Options

REG2	**REG1**	**REG0**	**A2**	**A1**	**A0**	**D15 …. D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	NOP, Data = Don't Care						
0	0	0	0	0	1	Don't Care	Local-Ground-Offset Adjust	D1 Direction	D1 Value	D0 Direction	D0 Value	SDO Disable
0	0	0	1	0	0	CLR, Data = Don't Care						
0	0	0	1	0	1	LOAD, Data = Don't Care						

Table 9. Explanation of Function Register Options

NOP	No operation instruction used in readback operations.
Local-Ground-Offset Adjust	Set by the user to enable local-ground-offset adjust function. Cleared by the user to disable local-ground-offset adjust function (default).
D0 / D1 Direction	Set by the user to enable D0/D1 as outputs. Cleared by the user to enable D0/D1 as inputs (default). Have weak internal pull-ups.
D0 / D1 Value	I/O port status bits. Logic values written to these locations determine the logic outputs on the D0 and D1 pins when configured as outputs. These bits indicate the status of the D0 and D1 pins when the I/O port is active as an input. When enabled as inputs, these bits are don't cares during a write operation.
SDO Disable	Set by the user to disable the SDO output. Cleared by the user to enable the SDO output (default).
CLR	Addressing this function resets the DAC outputs to 0 V in twos complement mode and negative full scale in binary mode.
LOAD	Addressing this function updates the DAC registers and consequently the analog outputs.

DATA REGISTER

The Data register is addressed by setting the three REG bits to 010. The DAC address bits select with which DAC Channel the Data transfer is to take place (Refer to Table 7). The 16 data bits are in positions D15 to D0 as shown in Table 10.

Table 10. Programming the Data Register

REG2	REG1	REG0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	DAC Address			16 Bit DAC Data															

COARSE GAIN REGISTER

The Coarse Gain Register is addressed by setting the three REG bits to 011. The DAC address bits select with which DAC Channel the Data transfer is to take place (Refer to Table 7). The Coarse Gain Register ia a 2-bit register and allows the user to select the output range of each DAC as shown in Table 12.

Table 11. Programming the Coarse Gain Register

REG2	REG1	REG0	A2	A1	A0	D15 …. D2	D1	D0
0	1	1	DAC Address			Don't Care	CG1	CG0

Table 12. Output Range Selection

Output Range	CG1	CG0
± 10 V	0	0
± 10.25 V	0	1
± 10.5 V	1	0

FINE GAIN REGISTER

The Fine Gain Register is addressed by setting the three REG bits to 100. The DAC address bits select with which DAC Channel the Data transfer is to take place (Refer to Table 7). The Fine Gain Register is a 6-bit register and allows the user to adjust the gain of each DAC channel by -32 LSBs to +31 LSBs in 1 LSB steps as shown in Table 13 and Table 14.

Table 13. Programming the Fine Gain Register

REG2	REG1	REG0	A2	A1	A0	D15 …. D6	D5	D4	D3	D2	D1	D0
1	0	0	DAC Address			Don't Care	FG5	FG4	FG3	FG2	FG1	FG0

Table 14. Fine Gain Register Options

Gain Adjustment	FG5	FG4	FG3	FG2	FG1	FG0
+31 LSBs	0	0	0	0	0	0
+30 LSBs	0	0	0	0	0	1
	-	-	-	-	-	-
No Adjustment	1	0	0	0	0	0
	-	-	-	-	-	-
-31 LSBs	1	1	1	1	1	0
-32 LSBs	1	1	1	1	1	1

OFFSET REGISTER

The Offset Register is addressed by setting the three REG bits to 101. The DAC address bits select with which DAC Channel the Data transfer is to take place (Refer to Table 7). The Offset Register is an 8-bit register and allows the user to adjust the offset of each channel by – 15.875 LSBs to + 16 LSBs in steps of 1/8 LSB as shown in Table 15 and Table 16.

Table 15. Programming the Offset Register

REG2	REG1	REG0	A2	A1	A0	D15 …. D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	DAC Address			Don't Care	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Table 16. Offset Register options

Offset Adjustment	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
+15.875 LSBs	0	0	0	0	0	0	0	0
+15.75 LSBs	0	0	0	0	0	0	0	1
	-	-	-	-	-	-	-	-
No Adjustment	1	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-
-15.875 LSBs	1	1	1	1	1	1	1	0
-16 LSBs	1	1	1	1	1	1	1	1

AD5764 FEATURES

ANALOG OUTPUT CONTROL

In many industrial process control applications, it is vital that the output voltage be controlled during power up and during brownout conditions. When the supply voltages are changing, the VOUT pin is clamped to 0 V via a low impedance path. To prevent the output amp being shorted to 0 V during this time, transmission gate G1 is also opened. These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the Reset In ($\overline{\text{RSTIN}}$) control input. For instance, if $\overline{\text{RSTIN}}$ is driven from a battery supervisor chip, the $\overline{\text{RSTIN}}$ input is driven low to open G1 and close G2 on power-off or during a brownout. Conversely, the on-chip voltage detector output ($\overline{\text{RSTOUT}}$) is also available to the user to control other parts of the system. The basic transmission gate functionality is shown in Figure 10.

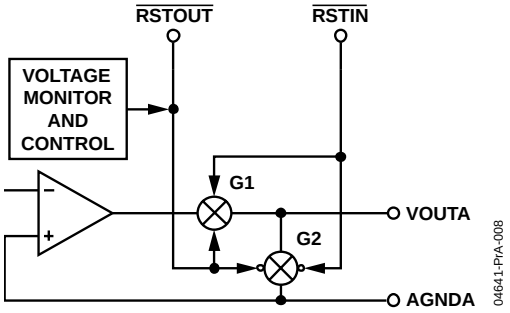

Figure 10. Analog Output Control Circuitry

DIGITAL OFFSET AND GAIN CONTROL

The AD5764 incorporates a digital offset adjust function with a ±16 LSB adjust range and 0.125 LSB resolution. The gain register allows the user to adjust the AD5764's full-scale output range. The full-scale output can be programmed to achieve full-scale ranges of ±10 V, ±10.256 V, and ±10.526 V. A fine gain trim is also available, allowing a trim range of ±16 LSB in 1 LSB steps.

PROGRAMMABLE SHORT-CIRCUIT PROTECTION

The short-circuit current of the output amplifiers can be programmed by inserting an external resistor between the ISCC pin and AGND. The programmable range for the current is 500 μA to 10 mA, corresponding to a resistor range of 120 kΩ to 6 kΩ. If the ISCC pin is left unconnected the short circuit current limit defaults to 5 mA. It should be noted that limiting the short circuit current to a small value can affect the slew rate of the output when driving into a capacitive load, therefore the value of short-circuit current programmed should take into account the size of the capacitive load being driven.

DIGITAL I/O PORT

The AD5764 contains a 2-bit digital I/O port (D1 and D0); these bits can be configured as inputs or outputs independently, and can be driven or have their values read back via the serial interface. The I/O port signals are referenced to DV_{CC} and DGND. When configured as outputs, they can be used as control signals to multiplexers or can be used to control calibration circuitry elsewhere in the system. When configured as inputs, the logic signals from limit switches, for example, are applied to D0 and D1 and can be read back via the digital interface.

TEMPERATURE SENSOR

The on-chip temperature sensor provides a voltage output that is linearly proportional to the Centigrade temperature scale. The typical accuracy of the temperature sensor is ±1°C at +25°C and ±5°C over the −40°C to +105°C range. Its nominal output voltage is 1.5V at +25°C, varying at 5 mV/°C, giving a typical output range of 1.175V to 1.9 V over the full temperature range. Its low output impedance, low self heating, and linear output simplify interfacing to temperature control circuitry and A/D converters.

LOCAL GROUND OFFSET ADJUST

The AD5764 incorporates a Local Ground Offset Adjust feature which when enabled in the Function Register adjusts the DAC outputs for voltage differences between The individual DAC ground pins and the REFGND pin ensuring that the DAC output voltages are always with respect to the local DAC ground pin. For instance if pin AGNDA is at +5mV with respect to the REFGND pin and VOUTA is measured with respect to AGNDA then a +5mV error will result, enabling the Local Ground Offset Adjust feature will offset VOUTA by +5mV eliminating the error.

APPLICATIONS INFORMATION

TYPICAL OPERATING CIRCUIT

Figure ?? shows the typical operating circuit for the AD5764. The only external components needed for this precision 16-bit DAC are decoupling capacitors on the supply pins, R-C connection from REFOUT to REFAB and REFCD and a short circuit current setting resistor. Because the device incorporates a voltage reference, and reference buffers, it eliminates the need for an external bipolar reference and associated buffers. This leads to an overall saving in both cost and board space.

In the circuit below, VDD and VSS are both conneted to ±15 V, but VDD and VSS can operate with supplies from ±11.4 V to ±16.5 V. In Figure ??, AGNDA is connected to REFGND, but the option of Force/Sense is included on this device, if required by the user.

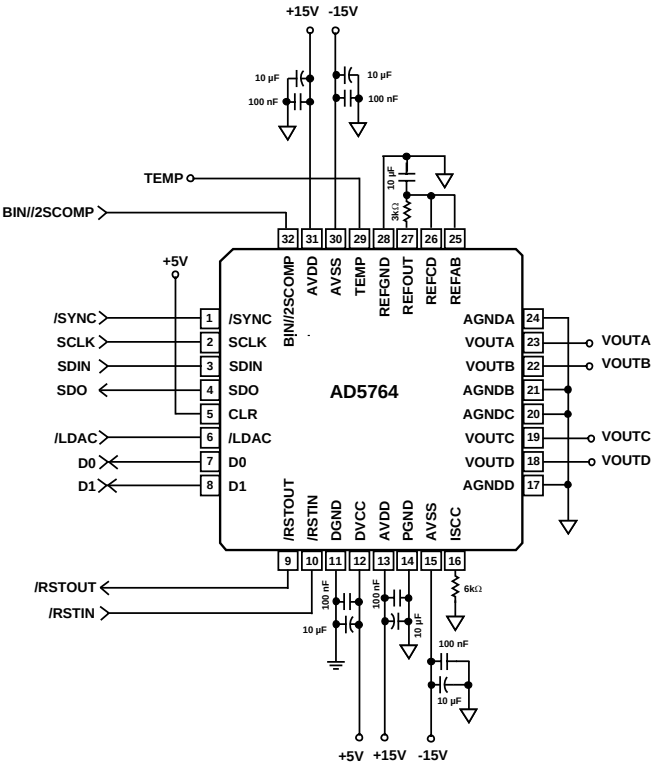

Figure 11. Typical operating circuit

Force/Sense of AGND

Because of the extremelyhigh accuracy of this device, system design issues such as grounding and contact resistance are very important. The AD5764, with ±10 V output, has an LSB size of 305 µV. Therefore, series wiring and connector resistances of very small values could cause voltage drops of an LSB. For this reason, the AD5764 offers a Force/Sense output configuration.

Figure ?? shows how to connect the AD5764 to the Force/Sense amplifier. Where accuracy of the output is important, an amplifier such as the OP177 is ideal. The OP177 is ultraprecise with offset voltages of 10 µV maximum at room temperature and offset drift 0f 0.1 µV/°C maximum. Alternative recommended amplifiers are the OP1177 and the OP77. For applications where optimization of the circuit for settling time is needed, the AD845 is recommended.

Figure ??. Driving REFGND and AGNDA using a force/sense amplifier

Precision Voltage Reference Selection

To achieve the optimum performance from the AD5764 over it's full operating temperature range an external voltage reference must be used. Thought should be given to the selection of a precision voltage reference. The AD5764 has two reference inputs, REFAB and REFCD. The voltages applied to the reference inputs are used tomprovide a buffered positiver and negative reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift and output voltage noise.

Initial accuracy error on the output voltage of an external reference could lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Also, choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim system errors out by setting the reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight lon-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL and TUE. A reference with a tight tempaerature coefficient specifiaction should be chosen to reduce the dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference waith as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET design) produce low output noise in the 0.1 Hx to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimise the output noise.

Table ??. Partial List of Precision References Recommended for use with the AD5764

Part No.	Initial Accuracy (mV max)	Long-Term Drift (ppm typ)	Temp Drift (ppm/ °C max)	0.1 Hz to 10 Hz Noise (µV p-p typ)
ADR435	± 6	30	3	3.4
ADR425	± 6	50	3	3.4
ADR02	± 5	50	3	15
ADR395	± 6	50	25	5
AD586	± 2.5	15	10	4

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5764 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5764 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5764 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5764 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board, which has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line, because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3 kV. The serial loading structure of the AD5764 makes it ideal for opto-isolated interfaces, because the number of interface lines is kept to a minimum. Figure ?? shows a 4-channel isolated interface to the AD5764. To reduce the number of opto-isolators, if the simultaneous updating of the DAC is not required, the LDAC pin may be tied permanently low. The DAC can then be updated on the rising edge of SYNC.

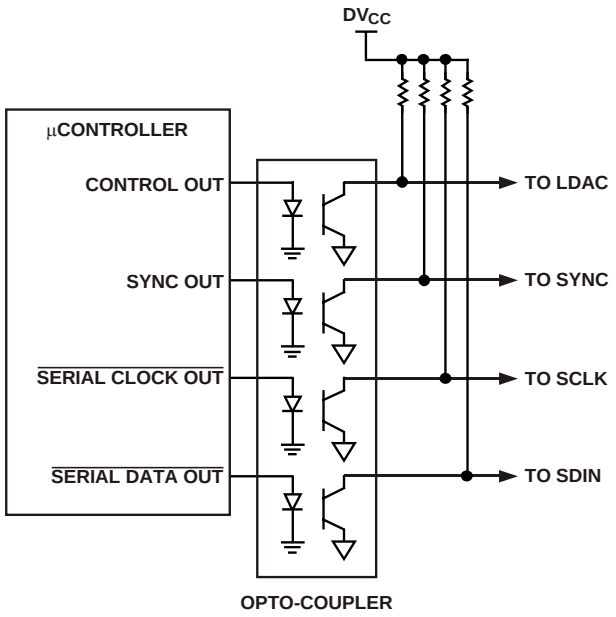

Figure 12. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5764 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5764 requires a 24-bit data word with data valid on the falling edge of SCLK.

For all the interfaces, the DAC output update may be done automatically when all the data is clocked in, or it may be done under the control of LDAC. The contents of the DAC register may be read using the readback function.

AD5764 to MC68HC11 Interface

Figure ?? shows an example of a serial interface between the AD5764 and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), clock polarity bit (CPOL = 0), and the clock phase bit (CPHA = 1). The SPI is configured by

writing to the SPI control register (SPCR)—see the *68HC11 User Manual*. SCK of the 68HC11 drives the SCLK of the AD5764, the MOSI output drives the serial data line (DIN) of the AD5764, and the MISO input is driven from SDO. The SYNC is driven from one of the port lines, in this case PC7.

When data is being transmitted to the AD5764, the SYNC line (PC7) is taken low and data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK. Eight falling clock edges occur in the transmit cycle, so, in order to load the required 24-bit word, PC7 is not brought high until the third 8-bit word has been transferred to the DAC's input shift register.

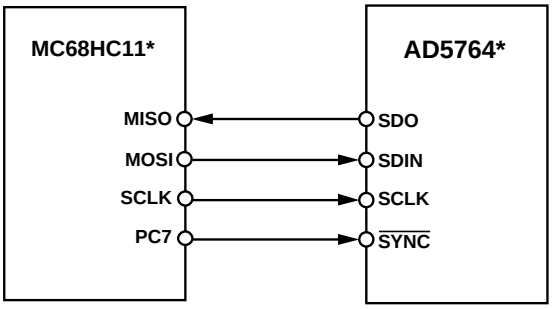

Figure 13. AD5764 to MC68HC11 Interface

LDAC is controlled by the PC6 port output. The DAC can be updated after each 3-byte transfer by bringing LDAC low. This example does not show other serial lines for the DAC. If CLR were used, it could be controlled by port output PC5, for example.

AD5764 to 8051 Interface

The AD5764 requires a clock synchronized to the serial data. For this reason, the 8051 must be operated in Mode 0. In this mode, serial data enters and exits through RxD, and a shift clock is output on RxD.

P3.3 and P3.4 are bit programmable pins on the serial port and are used to drive SYNC and LDAC, respectively.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user must ensure that the data in the SBUF register is arranged correctly, because the DAC expects MSB first.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is clocked out of the microcontroller on the rising edge of TxD and is valid on the falling edge. As a result, no glue logic is required between this DAC and the microcontroller interface.

The 8051 transmits data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Because the DAC expects a 24-bit word, SYNC (P3.3) must be left low after the first eight bits are transferred. After the third byte has been transferred, the P3.3 line is taken high. The DAC may be updated using LDAC via P3.4 of the 8051.

AD5764 to ADSP2101/ADSP2103 Interface

An interface between the AD5764 and the ADSP2101/ ADSP2103 is shown in Figure ??. The ADSP2101/ADSP2103 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP2101/ADSP2103 are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 24-bit word length.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the DAC. In the interface shown, the DAC output is updated using the LDAC pin via the DSP. Alternatively, the LDAC input could be tied permanently low, and then the update takes place automatically when TFS is taken high.

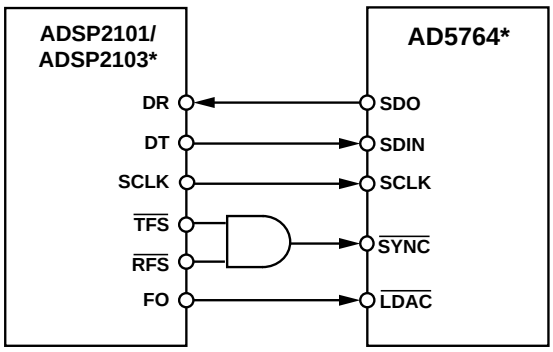

Figure 14. AD5764 to ADSP2101/ADSP2103 Interface

AD5764 to PIC16C6x/7x Interface

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit set to 0. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual*. In this example, I/O port RA1 is being used to pulse SYNC and enable the serial port of the AD5764. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive write operations are needed. Figure ?? shows the connection diagram.

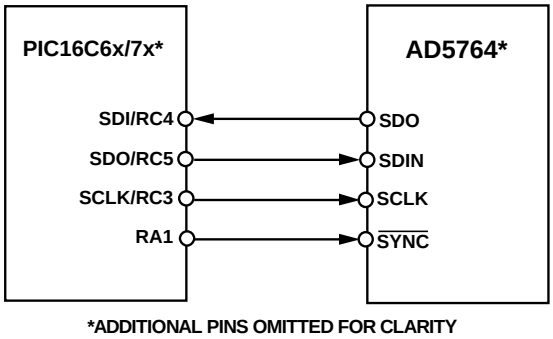

Figure 15. AD5764 to PIC16C6x/7x Interface

EVALUATION BOARD

The AD5764 comes with a full evaluation board to aid designers in evaluating the high performance of the part with a minimum of effort. All that is required with the evaluation board is a power supply, a PC, and an oscilloscope.

The AD5764 evaluation kit includes a populated, tested AD5764 printed circuit board. The evaluation board interfaces to the USB interface of the PC. Software is available with the evaluation board, which allows the user to easily program the AD5764. A schematic of the evaluation board is shown in Figure ??. The software runs on any PC that has Microsoft Windows® 95/98/ME/2000/NT/XP installed.

An application note is available that gives full details on operating the evaluation board.

OUTLINE DIMENSIONS

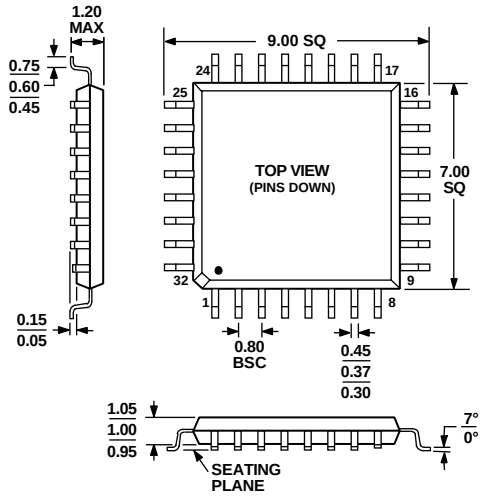

Figure 16. 32-Lead Thin Quad Flatpack [TQFP]
(SU-32)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Function	INL	Package Description	Package Option
AD5764CSU	Quad 16-Bit DAC	± 1 LSB Max	32-Lead TQFP	SU-32
AD5764BSU	Quad 16-Bit DAC	± 2 LSB Max	32-Lead TQFP	SU-32
AD5764ASU	Quad 16-Bit DAC	± 4 LSB Max	32-Lead TQFP	SU-32