Triple-Output LDO for WLAN

Features

- 3.0V to 3.6V input voltage range
- Preset output voltage with excellent line and load regulation
- LDO1 = 1.80V/500mA, ±1.5% max load regulation
- LDO2 = 2.84V/300mA, ±1% max load regulation
- LDO3 = 2.84V/200mA, ±1% max load regulation
- Low output noise (<30µVrms for LDO3)
- Low dropout voltage; 135mV (typ.) for LDO2 at 300mA, and 110mV (typ.) for LDO3 at 200mA.
- Low quiescent current, < 600µA typical
- Integrated microprocessor RESET circuit with adjustable RESET delay (2.5ms per nF of C_T)
- Logic controlled shutdown
- Power good signal
- Built-in power up and power down sequence control between LDO1 and LDO2
- Over-temperature and over-current protection
- TQFN-16, RoHS compliant lead-free package

Applications

- Wireless LAN 802.11 chipset power supply
- Wireless LAN cards
- Wireless instrumentation

Product Description

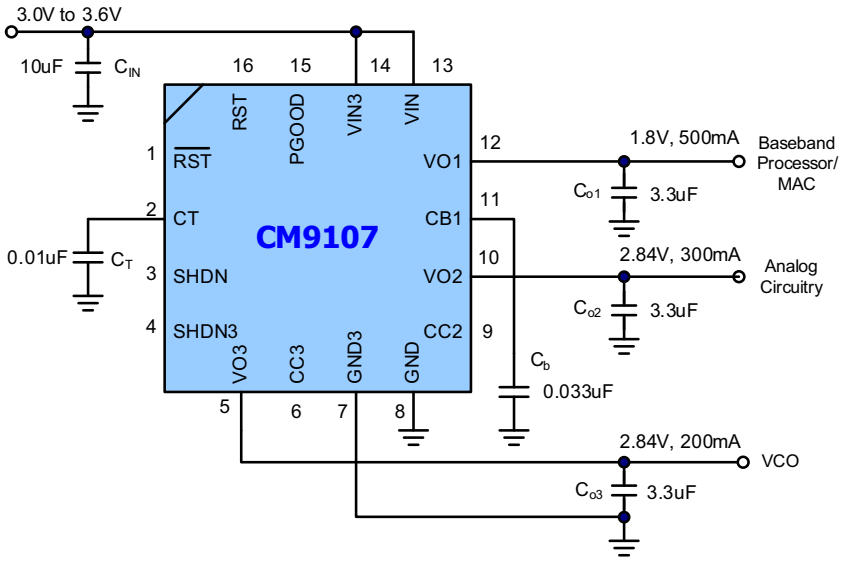
The CM9107 is a triple-output, low noise, low dropout (LDO) linear regulator with an integrated microprocessor reset circuit. It is designed for use with wireless local-area network chipsets. It has an input voltage range of 3.0V to 3.6V, and supplies a 500mA, 1.80V preset output (LDO1); a 300mA, 2.84V output (LDO2), and a 200mA, low noise output of 2.84V (LDO3). The CM9107 has excellent line and load regulation over the operating temperature range.

The CM9107 LDOs features low dropout voltage by using efficient P-channel MOSFETs for each output. It also features a power good signal (active high) when all three LDOs are in regulation. It provides two shutdown control pins, LDO1 and LDO2 power sequencing, plus short-circuit and over-temperature shutdown protection.

The CM9107 also provides a microprocessor RESET circuit with RST and $\overline{RST}$ outputs. The RESET signal is asserted when the V_{IN} supply voltage drops below 2.63V, remaining asserted for the adjustable RESET delay period, controlled by an external capacitor on the CT pin.

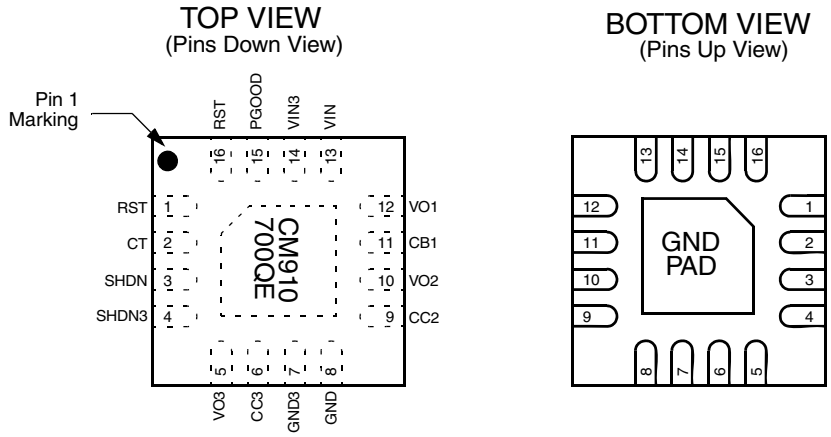
The CM9107 is packaged in a 16-pin TQFN (4mm x 4mm) package. It can operate over the industrial temperature range of –40°C to 85°C.

Typical Application



Package Pinout

PACKAGE / PINOUT DIAGRAM



CM9107-00QE
16-Lead TQFN Package (4mmx4mm)

Note: This drawing is not to scale.

PIN DESCRIPTIONS

LEAD(s)	NAME	DESCRIPTION
1	$\overline{\text{RST}}$	Reset bar pin. This is the inverse output of the RST signal pin (pin 16).
2	CT	CT pin for setting the delay time for RST assert (2.5ms per nF).
3	SHDN	Shutdown control input pin for LDO1 and LDO2. Active low, LDO1 and LDO2 will be off when the pin is pulled low. Connect to V_{IN} when unused.
4	SHDN3	Shutdown control input pin for LDO3. Active low. Connect to V_{IN} when unused.
5	VO3	LDO3 output pin (2.84V). Connect a low-ESR bypass capacitor of 2.2µF, minimum.
6	CC3	This pin is used for testing. In the application it could be either floating or tied to ground
7	GND3	Ground pin for LDO3
8	GND	Ground pin for LDO1, LDO2 and control circuit
9	CC2	This pin is used for testing. In the application it could be either floating or tied to ground
10	VO2	LDO2 output pin (2.84V). Connect a low-ESR bypass capacitor of 2.2µF, minimum.
11	CB1	Bypass capacitor pin for internal bandgap reference (typically 0.033µF low-ESR type).
12	VO1	LDO1 output pin (1.80V). Connect a low-ESR bypass capacitor of 2.2µF, minimum.
13	VIN	Power input pin for LDO2 and LDO3. Connect to a low-ESR bypass capacitor of 2.2µF, minimum.
14	VIN3	Power input pin for LDO3. Connect to Pin 13, on the PC board, very near the device.
15	PGOOD	Power good output pin with internal pull-up resistor to VIN, goes high when all 3 LDOs are in regulation.

Pin Descriptions (cont'd)

PIN DESCRIPTIONS		
16	RST	Reset output pin. When V_{IN} falls below the RESET threshold, this RST pin is asserted (active high). When V_{IN} rises above the RESET threshold, RST goes low after a delay of 2.5ms per nF of CT capacitance. Refer to RESET section in the Application Information.

Ordering Information

PART NUMBERING INFORMATION			
		Lead Free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking
16	TQFN	CM9107-00QE	CM9107 00QE

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD Protection (HBM)	±2	kV
V_{IN}, V_{IN3}, GND3 to GND	[GND - 0.3] to +6.0	V
Pin Voltages		
V_{O1}, V_{O2}, V_{O3} to GND	[GND - 0.3] to +6.0	V
C_{B1} to GND to GND	[GND - 0.3] to +6.0	V
SHDN, SHDN3 to GND	[GND - 0.3] to +5.0	V
CT, RST, $\overline{RST}$, PGOOD to GND	[GND - 0.3] to +5.0	V
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Lead Temperature (Soldering, 10sec)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	All outputs are no load		600	750	µA
V_{SHDN}	Shutdown Supply Current	SHDN = SHDN3 = 0		5.0	10	µA
V_{IL}	Shutdown (active low) Input Low Threshold				0.4	V
V_{IH}	Shutdown Input High Threshold		2.0			V
T_{START}	Start-up Time (from SHDN going high to V_{OUT} in regulation) (Note 3)	V_{OUT} = 95% of final value		120		µs

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
T_{PGOOD}	PGOOD Threshold	All output currents = 50% rating	-5		+5	%
O_{PGOOD}	PGOOD Output Level	I_{SINK} = 2mA			0.25	V
T_{OVER}	OTP Threshold			150		ºC
T_{HYS}	OTP Hysteresis			20		ºC
UVLO	Undervoltage Lockout (Note 2)	All outputs are no load.	2.20	2.45	2.65	V
LDO1						
V_{OUT}	Output Voltage			1.80		V
$V_{OUT\ acc}$	Output Voltage Accuracy	I_{OUT} = 10mA	-1.5		+1.5	%
I_{LIM}	Over-current Limit (Note 2)		550	750		mA
$V_{R\ LIN}$	Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15		0.15	%/V
$V_{R\ LOAD}$	Load Regulation (Note 5)	I_{OUT} =10mA to 500mA	-1.5		1.5	%
$V_{OUT\ N}$	Output Noise	10Hz < f < 100kHz, Co1 = 3.3µF, I_{OUT} = 50mA		100		µVrms
LDO2						
V_{OUT}	Output Voltage			2.84		V
$V_{OUT\ acc}$	Output Voltage Accuracy	I_{OUT} = 10mA	-1.5		+1.5	%
I_{LIM}	Over-current Limit (Note 2)		330	550		mA
$V_{R\ LIN}$	Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15		0.15	%/V
$V_{R\ LOAD}$	Load Regulation (Note 5)	I_{OUT} = 10mA to 300mA		0.2	1.0	%
V_{DROP}	Dropout Voltage (Note 4)	I_{OUT} = 30 mA		135	220	mV
$V_{OUT\ N}$	Output Noise	10Hz < f < 100kHz, I_{OUT} = 10mA Co2 = 2.2µF Co2 = 10µF		 70 60		 µVrms µVrms
LDO3						
V_{OUT}	Output Voltage			2.84		V
$V_{OUT\ acc}$	Output Voltage Accuracy	I_{OUT} = 10mA	-1.5		+1.5	%
I_{LIM}	Over-current Limit (Note 2)		250	450		mA
$V_{R\ LIN}$	Line Regulation	V_{IN3} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15		0.15	%/V
$V_{R\ LOAD}$	Load Regulation (Note 5)	I_{OUT} = 10mA to 200mA		0.2	1.0	%
V_{DROP}	Dropout Voltage (Note 4)	I_{OUT} = 200mA		110	200	mV
$V_{OUT\ N}$	Output Noise	10Hz < f < 100kHz, I_{OUT} = 10mA Co3 = 2.2µF Co3 = 10µF		 30 20		 µVrms µVrms
RESET						
T_{RESET}	RESET Threshold (Vth) (Note 2)		2.56	2.63	2.69	V
$T_{HYS\ RESET}$	RESET Threshold Hysteresis			10		mV
$V_{DROP\ RESETD}$	V_{IN} Dropout Reset Delay	V_{CC} = Vth to Vth –100mV		20		µs
T_{RST}	RST / $\overline{RST}$ Timeout Period (Note 2)	CT = 10nF	25			ms

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{RST_L}	RST / $\overline{RST}$ Output Low Signal				0.4	V
V_{RST_H}	RST / $\overline{RST}$ Output High Signal		.8 x V_{IN}			V
$I_{Q\ RST}$	RESET Block Quiescent Current			4		µA

Note 1: $V_{IN} = V_{IN3} = 3.3V$. $C_{IN} = 10\mu F$, $C_O1 = C_O2 = C_O3 = 3.3\mu F$, $C_B = 33nF$. $T_A = 25°C$ unless otherwise specified.

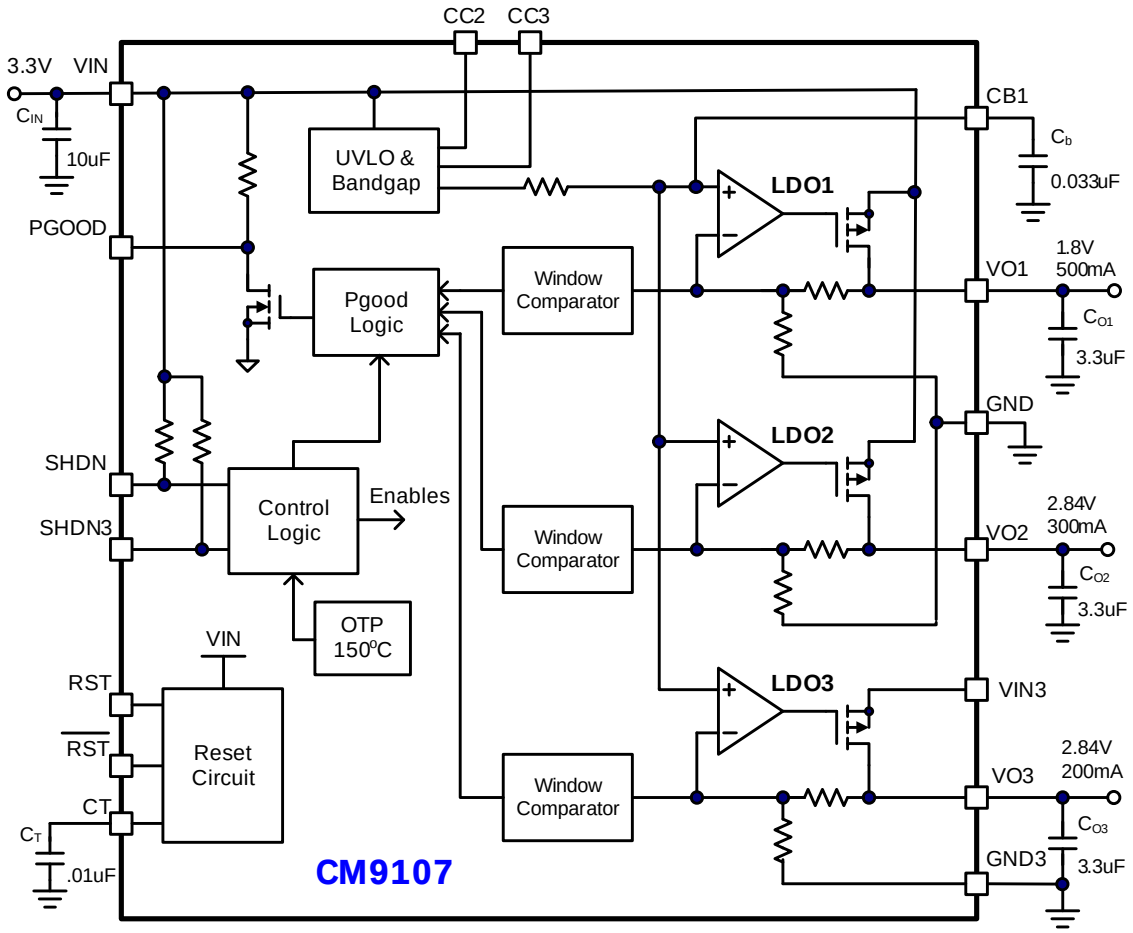
Note 2: Parameter is guaranteed by design, not production tested.

Note 3: The start-up time is defined as from SHDN pin goes high until Vo1 reaches regulation; or from SHDN3 goes high until VO3 reaches regulation.

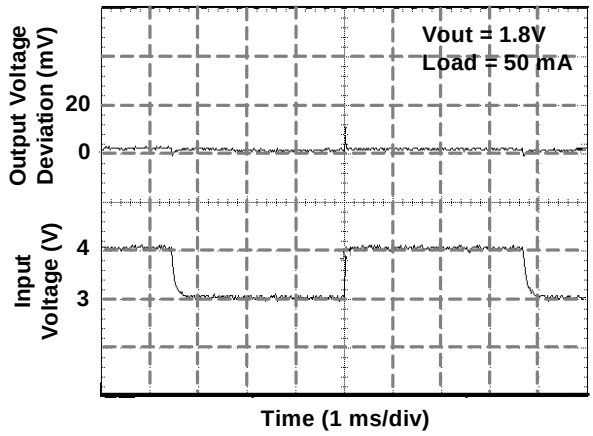
Note 4: The dropout voltage is defined as Vind– Vod, where Vod is 50mV below V_{OUT} value measured at $V_{IN} = 3.3V$.

Note 5: Regulation is measured at constant junction temperature using low duty cycle pulse testing.

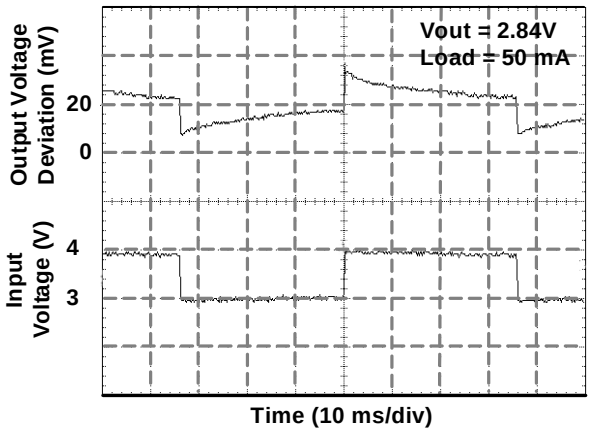
Functional Block Diagram



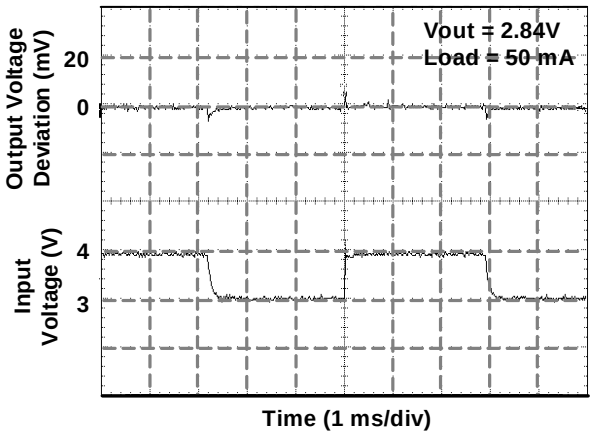
Typical Performance Curves



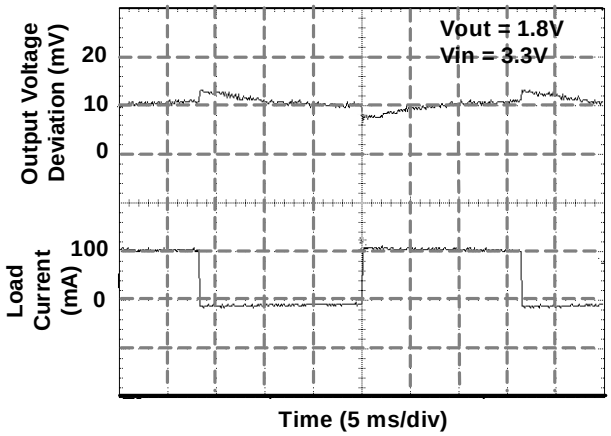
Line Reguation Response, LDO1



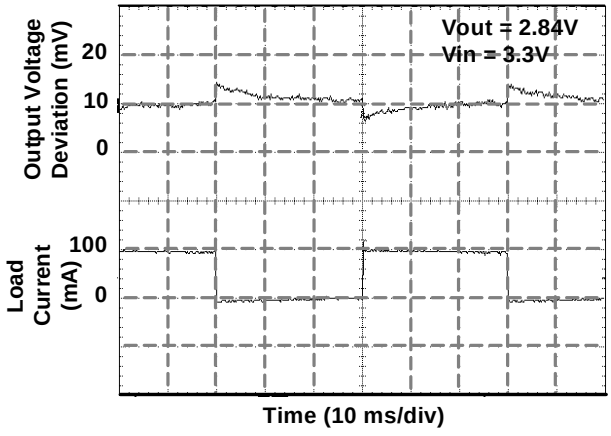
Line Reguation Response, LDO2



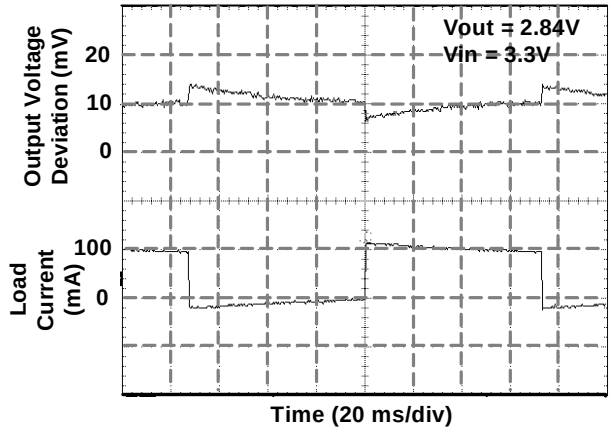
Line Reguation Response, LDO3



Load Reguation Response, LDO1



Load Reguation Response, LDO2



Load Reguation Response, LDO3

Application Information

The CM9107 is a triple-output, low noise, low dropout (LDO) linear voltage regulator with an integrated microprocessor reset circuit. It provides a single-chip power management solution for WLAN systems, providing the fixed output voltages needed for popular wireless chipsets. It has an input voltage range of 3.0V to 3.6V. The device can supply 500mA output from LDO1 (1.8V), 300mA from LDO2 (2.84V) and 200mA from the low-noise LDO3 (2.84V).

The CM9107 achieves its low dropout voltage by using efficient, internal P-channel MOSFETs for each output. The dropout voltage for LDO2 is less than 220mV at 300mA load. The dropout voltage for LDO3 is less than 200mV at 200mA load. The lower voltage output from LDO1 assures sufficient headroom to deliver 500mA once V_{IN} is above the undervoltage lockout point, typically 2.45V. The CM9107 has excellent line and load regulation over the operating temperature range. The LDO outputs allow the use of low cost, space-efficient ceramic capacitors.

The LDO3 has exceptionally low output noise, and is ideal for VCO power supplies. The WLAN's VCO circuit is very phase noise sensitive, and needs clean power for reliable operation. At 10mA output, the noise density from 10Hz to 100kHz is typically less than $30\mu V_{RMS}$ when using a 2.2µF output capacitor. With a 10µF output capacitor, the noise density is typically $20\mu V_{RMS}$.

Protection

The CM9107 has independent over-current protection for each LDO output, with current foldback. The minimum over-current limit is 550mA for LDO1, 330mA for LDO2, and 250mA for LDO3.

The CM9107 includes a thermal shutdown. If there is excessive internal power dissipation due to an over current condition, or a high V_{IN}-V_{OUT} differential, and device's junction temperature exceeds 150°C (typical), the outputs are turned off. The LDOs are turned on again after the junction temperature drops below 130°C.

Power Good

The CM9107 provides a high power good signal (PGOOD) if all three LDOs output voltages are within +/-5% of their nominal regulation value. The PGOOD pin will go low when any output is out of regulation due to over-current dropout, or when thermal shutdown is triggered.

The PGOOD pin has an internal pull-up resistor. In the shutdown mode (SHDN and SHDN3 both low), PGOOD goes high.

Shutdown Control and Power Up/Down Sequence

The CM9107 provides two active low, shutdown control pins, SHDN and SHDN3. SHDN controls both LDO1 and LDO2. LDO3 is independently controlled with SHDN3. Each shutdown pin has internal pull-up resistor to V_{IN}. Pulling the pins low shuts-down the appropriate output.

When SHDN goes high, LDO1's output will rise first. Once LDO1's output is above about 1.7V, LDO2's output will start to rise. When SHDN goes low, LDO2's output will drop first. When LDO2's output drops below about 2.7V, LDO1's output will start to drop. Refer to Figure 1.

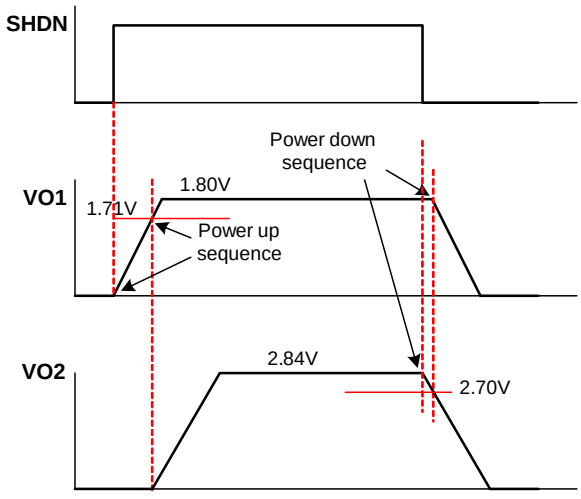


Figure 1. Power Sequencing

Reset

The CM9107's RESET circuit monitors the V_{IN} voltage only, upstream of the LDOs. This circuit is completely

Application Information (cont'd)

independent of the three LDOs and their control circuits, functioning as a supervisory circuit for the MAC/Baseband microprocessor. The RESET circuit has complimentary RST and $\overline{RST}$ push-pull outputs.

When the system is powered-up and V_{IN} reaches a pre-set threshold, RESET waits for the programmed time-period and then signals the microprocessor that V_{IN} is stable. During system operation, V_{IN} is continuously monitored, and if it drops below the preset threshold, it tells the microprocessor to reset, thus preventing loss of data.

The RESET signals are asserted when the V_{IN} supply voltage drops below 2.63V and will remain asserted for the adjustable RESET delay period, controlled by connecting an external capacitor on the CT pin. The RESET delay period is 2.5ms/nF of CT pin capacitance. At the end of the delay period, the RESET signals are released; RST goes low and $\overline{RST}$ goes high. Refer to Figure 2. If V_{IN} drops below the RESET threshold again, the RESET signal is re-asserted. The reset delay and threshold hysteresis help assure valid RESET signals in the presence of erratic V_{IN} behavior.

The maximum low output voltage is 0.3V at 1.6mA sink current. Minimum high output voltage is 80% of V_{IN}. The RESET circuit consumes less than 5µA quiescent current.

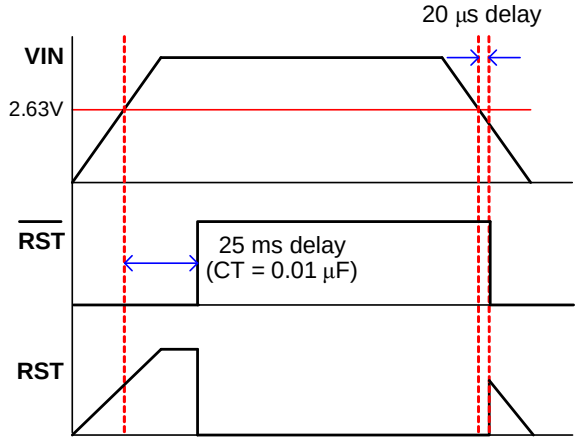


Figure 2. Reset Delay

Capacitor Selection

The CM9107's LDOs have a wide stability region for a range of output capacitance and ESR values. While 2.2µF will be sufficient for each LDO output, higher output capacitance, such as 3.3µF, 4.7µF or 10µF, will reduce output noise and over-shoot during load transients. Low ESR ceramic capacitors are ideally suited for the outputs of the CM9107, with X5R and X7R dielectrics being the most stable over voltage and temperature, providing the best performance.

To reduce the noise generated by the bandgap circuit, a 33nF, low ESR ceramic capacitor is recommended from the CB1 pin to ground.

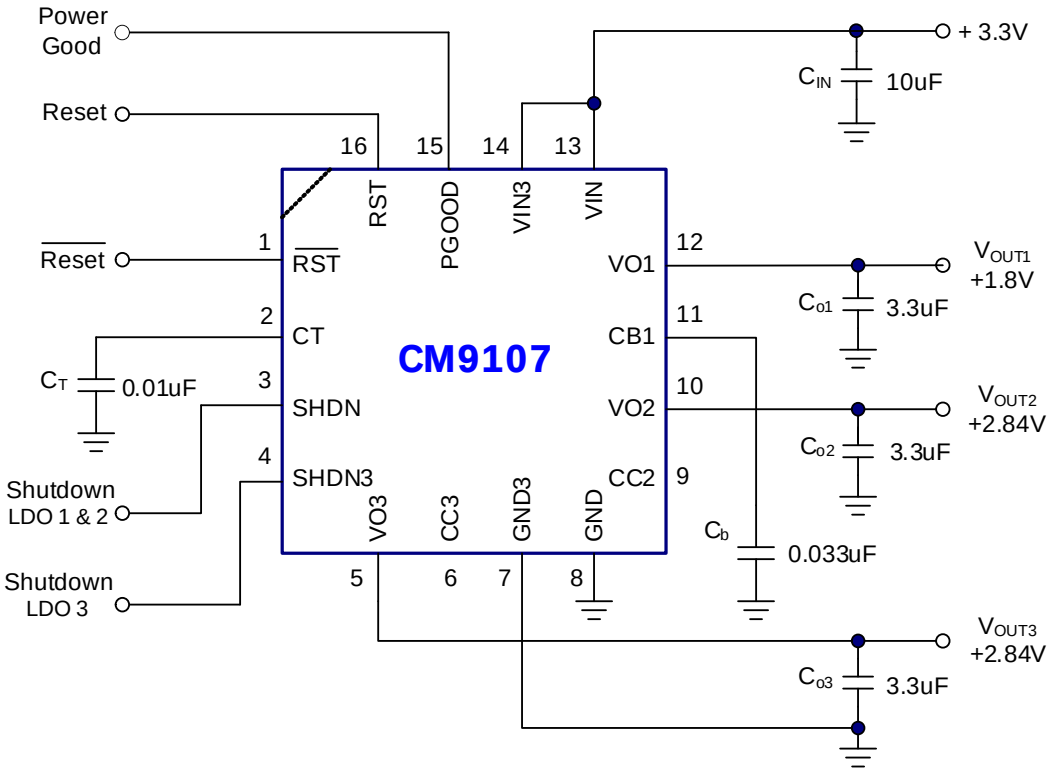
Load Transient

The input and output capacitors will effect the transient load response. The input capacitor will reduce input drop during load transients, improving response on all outputs, while increased output capacitance improves the individual LDO output's load transient response.

Layout Issues

Input and output capacitors should be located close to the device. For good thermal conduction, connections to large areas of C_U should be provided on the PCB.

Application Circuit



Bill of Materials

BILL OF MATERIALS				
ITEM	**QUANTITY**	**REFERENCE**	**PART**	**MFR**
1	1	C_{IN}	10µF/10V/1210/X7R	any
2	3	C_{o1}, C_{o2}, C_{o3}	3.3µF/10V/1206/X7R	any
3	1	C_T	.01µF/10V/X7R	any
4	1	C_B	.033µF/10V/X7R	any

Mechanical Details

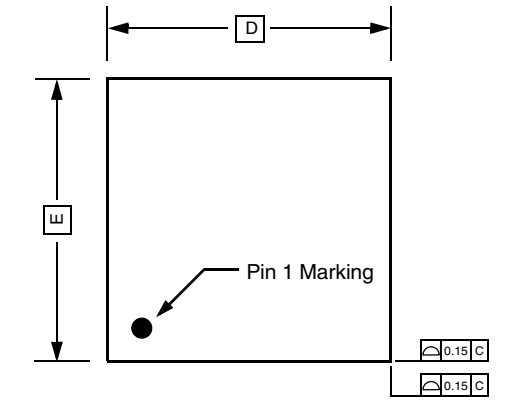
TQFN-16 Mechanical Specifications

The CM9107-00QE is supplied in a 16-lead, 4.0mm x 4.0mm TQFN package. Dimensions are presented below.

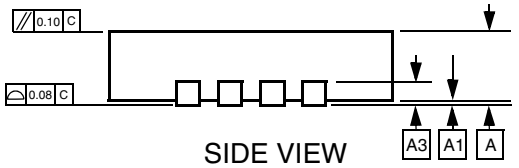
For complete information on the TQFN16, see the California Micro Devices TQFN Package Information document.

PACKAGE DIMENSIONS						
Package	TQFN-16 (4x4)					
Leads	16					
Dim.	**Millimeters**			**Inches**		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.70	0.75	0.8	0.027	0.029	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			.008		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.85	4.00	4.15	0.152	0.157	0.163
D1	2.40	2.50	2.80	0.094	0.098	0.110
E	3.85	4.00	4.15	0.152	0.157	0.163
E1	2.40	2.50	2.80	0.094	0.098	0.110
e	0.65 BSC.			0.026		
L	0.40 BSC			0.016		
# per tape and reel	3000 pieces					
Controlling dimension: millimeters						

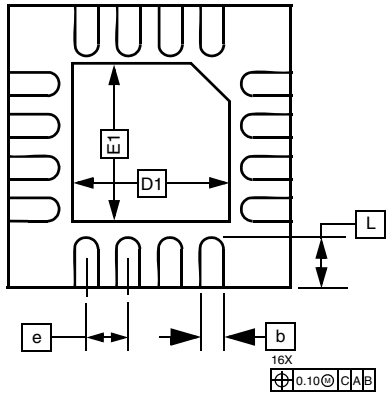
Mechanical Package Diagrams



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Package Dimensions for 16-Lead QFN