# iC-LF1401

128x1 Linear Image Sensor



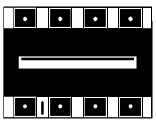
## FEATURES

- 128 active photo pixels of 56 µm at a 63.5 µm pitch (400 DPI)
- Integrating L-V conversion followed by a sample & hold circuit
- High sensitivity and uniformity over wavelength
- High clockrates of up to 5 MHz
- Only 128 clocks required for readout
- Shutter function enables flexible integration times
- Glitch-free analogue output
- Push-pull output amplifier
- 5 V single supply operation
- Can run off external bias to reduce power consumption
- Pin-to-pin compatible with TSL1401

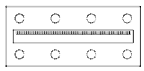
## APPLICATIONS

- Optical line image sensors
- CCD substitute

## PACKAGES



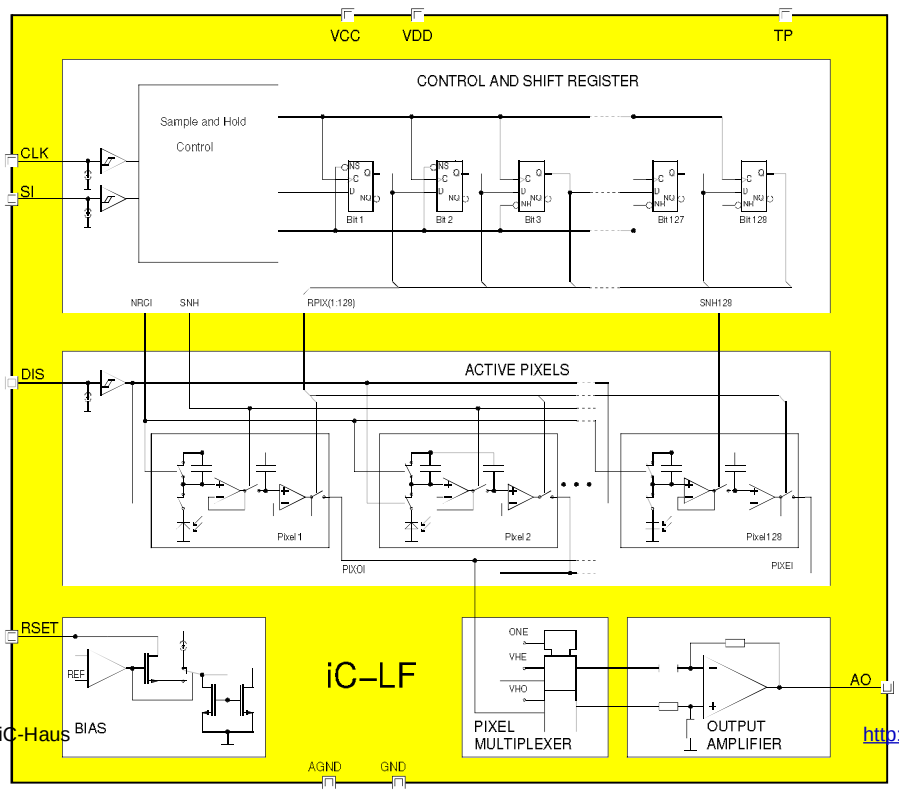
OLGA LF2C



OBGA™ LF3C

Die size (8.5 mm x 1.6 mm)

## BLOCK DIAGRAM



## DESCRIPTION

iC-LF1401 is an integrating light-to-voltage converter with a line of 128 pixels pitched at 63.5 µm (center-to-center distance). Each pixel consists of a 56.4 µm x 200 µm photodiode and an integration capacitor with a sample-and-hold circuit.

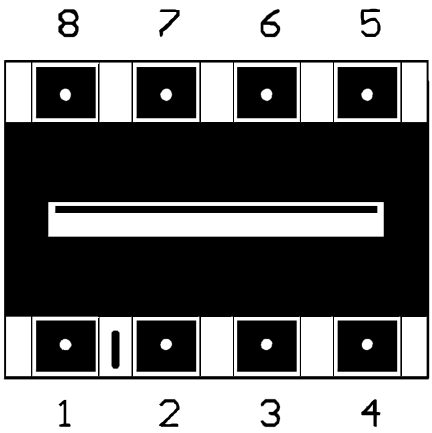
The integrated control logic makes operation very simple, with only a start and clock signal necessary. A third control input (DIS) enables the integration to be suspended at any time (electronic shutter).

When the start signal is given hold mode is activated for all pixels simultaneously with the next leading clock edge; starting with pixel 1 the hold voltages are switched in sequence to the push-pull output amplifier. The second clock pulse resets all integration capacitors and the integration period starts again in the background during the output phase. A run is complete after 128 clock pulses.

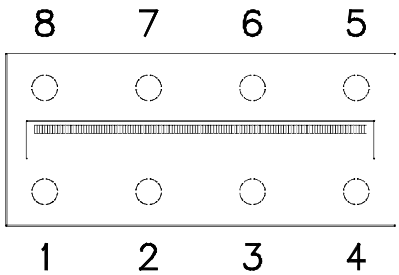
iC-LF1401 is suitable for high clock rates of up to 5 MHz. If this is not required the supply current can be reduced via the external bias setting (current into pin RSET).

## PACKAGES OLGA LF2C, OBGA™ LF3C

### PIN CONFIGURATION OLGA LF2C (top view)




### PIN CONFIGURATION OBGA™ LF3C (top view)

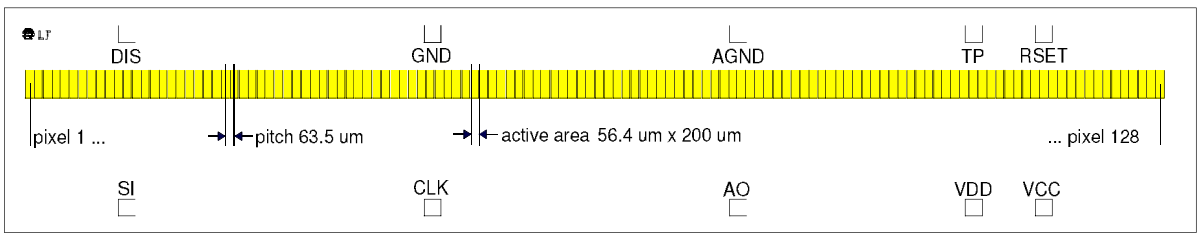



### PIN FUNCTIONS

| No. | Name | Function |
|---|---|---|
| 1 | SI | Start Integration Input |
| 2 | CLK | Clock Input |
| 3 | AO | Analogue Output |
| 4 | VCC | +5 V Supply Voltage |
| 5 | RSET | Bias Current (connected to GND for internal bias = default; resistor from VCC to RSET for reduced current consumption) |
| 6 | AGND | Analogue Ground |
| 7 | GND | Digital Ground |
| 8 | DIS | Hold Integration Input |

## CHIP LAYOUT

Die size: 8.5 mm x 1.6 mm



## ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

| Item No. | Symbol | Parameter | Conditions | Fig. | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| G001 | VDD | Digital Supply Voltage | | | -0.3 | 6 | V |
| G002 | VCC | Analog Supply Voltage | | | -0.3 | 6 | V |
| G003 | V() | Voltage at SI, CLK, DIS, RSET, TP, AO | | | -0.3 | VCC + 0.3 | V |
| G004 | I() | Current in RSET, TP, AO | | | -10 | 10 | mA |
| G005 | Vd() | ESD Susceptibility at all pins | MIL-STD-883, Method 3015, HBM 100 pF discharged through 1.5 kΩ | | | 2 | kV |
| G006 | Tj | Operating Junction Temperature | | | -40 | 125 | °C |
| G007 | Ts | Storage Temperature Range | see package specification | | | | |

## THERMAL DATA

Operating Conditions: VCC = VDD = 5 V ±10 %

| Item No. | Symbol | Parameter | Conditions | Fig. | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| T01 | Ta | Operating Ambient Temperature Range (extended range on request) | see package specification | | | | | |

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V ±10 %, RSET = GND, Tj = -25...85 °C unless otherwise noted

| Item No. | Symbol | Parameter | Conditions | Tj °C | Fig. | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **Total Device** | | | | | | | | | |
| 001 | VDD | Digital Supply Voltage Range | | | | 4.5 | | 5.5 | V |
| 002 | VCC | Analog Supply Voltage Range | | | | 4.5 | | 5.5 | V |
| 003 | I(VDD) | Supply Current in VDD | f(CLK) = 1 MHz | | | | 200 | 300 | µA |
| 004 | I(VCC) | Supply Current in VCC | | | | | 8 | 13 | mA |
| 005 | Vc()hi | Clamp Voltage hi at SI, CLK,DIS, TP, RSET | Vc()hi = V() – V(VCC), I() = 1 mA | | | 0.3 | | 1.8 | V |
| 006 | Vc()lo | Clamp Voltage lo at SI, CLK,DIS, TP, RSET | Vc()hi = V() – V(AGND), I() = -1 mA | | | -1.5 | | -0.3 | V |
| 007 | Vc()hi | Clamp Voltage hi at AO | Vc()hi = V(AO) – V(VCC), I(AO) = 1 mA | | | 0.3 | | 1.5 | V |
| 008 | Vc()lo | Clamp Voltage lo at AO, VCC, VDD, GND | Vc()lo = V() – V(AGND), I() = -1 mA | | | -1.5 | | -0.3 | V |
| **Photodiode Array** | | | | | | | | | |
| 201 | A() | Radiant Sensitive Area | 200 µm x 56.40 µm per Pixel | | | | 0.01128 | | mm² |
| 202 | S(λ)max | Spectral Sensitivity | λ = 680 nm | | | | 0.5 | | A/W |
| 203 | λar | Spectral Application Range | S(λar) = 0.25 x S(λ)max | | | 400 | | 980 | nm |
| **Analogue Output AO** | | | | | | | | | |
| 301 | Vs()lo | Saturation Voltage lo | I() = 1 mA | | | | | 0.5 | V |
| 302 | Vs()hi | Saturation Voltage hi | Vs()hi = VCC – V(), I() = -1 mA | | | | | 1 | V |
| 303 | K | Sensitivity | λ = 680 nm, package OLGA LF2C | | | | 2.88 | | V/pWs |
| 304 | V0() | Offset Voltage | integration time 1 ms, no illumination | | | | 400 | 800 | mV |
| 305 | ΔV0() | Offset Voltage Deviation during integration mode | ΔV0() = V(AO)t1 – V(AO)t2, Δt = t2 – t1 = 1 ms | | | -250 | | 50 | mV |
| 306 | ΔV() | Signal Deviation during hold mode | ΔV0() = V(AO)t1 – V(AO)t2, Δt = t2 – t1 = 1 ms | | | -150 | | 150 | mV |
| 307 | tp(CLK-AO) | Settling Time | Cl(AO) = 10 pF, CLK lo → hi until V(AO) = 0.98 x V(VCC) | | | | | 200 | ns |
| **Power-On Reset** | | | | | | | | | |
| 801 | VCCon | Power-On Release by VCC | | | | | | 4.4 | V |
| 802 | VCCoff | Power-Down Reset by VCC | | | | 1 | | | V |
| 803 | VCChys | Hysteresis | VCChys = VCCon – VCCoff | | | 0.4 | 1 | 2 | V |
| **Bias Current Adjust RSET** | | | | | | | | | |
| 901 | Ibias() | Permissible External Bias Current | | | | 20 | | 100 | µA |
| 902 | Vref | Reference Voltage | I(RSET) = Ibias | | | 2.5 | 3 | 3.5 | V |
| **Input Interface SI, CLK, DIS** | | | | | | | | | |
| B01 | Vt()hi | Threshold Voltage hi | | | 2 | 1.4 | | 1.8 | V |
| B02 | Vt()lo | Threshold Voltage lo | | | 2 | 0.9 | | 1.2 | V |
| B03 | Vt()hys | Hysteresis | Vt()hys = Vt()hi – Vt()lo | | 2 | 300 | | 800 | mV |
| B04 | I() | Pull-Down Current | | | | 10 | 30 | 50 | µA |
| B05 | fclk | Permissible Clock Frequency | | | | | | 5 | MHz |

## OPTICAL CHARACTERISTICS: Diagrams

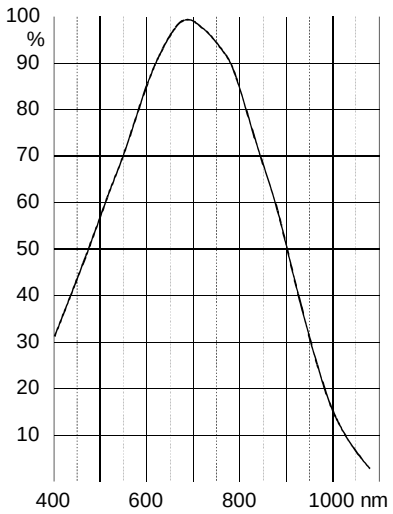



Figure 1: Relative spectral sensitivity

## OPERATING REQUIREMENTS: Logic

Operating Conditions: VCC = VDD = 5 V ±10 %, Tj = -25...85 °C
input levels lo = 0...0.45 V, hi = 2.4 V...VCC, see Fig. 2 for reference levels

| Item No. | Symbol | Parameter | Conditions | Fig. | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| I001 | tset | Setup Time:<br>SI stable before CLK lo → hi | | 3 | 50 | | ns |
| I002 | thold | Hold Time:SI stable after CLK lo → hi | | 3 | 50 | | ns |

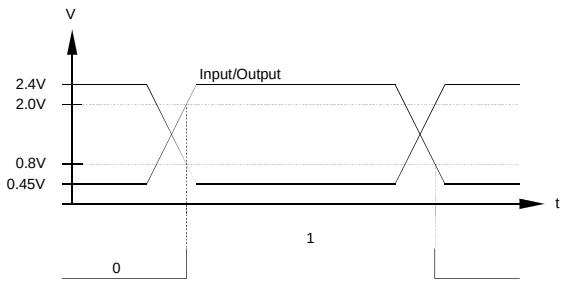



Figure 2: Reference levels

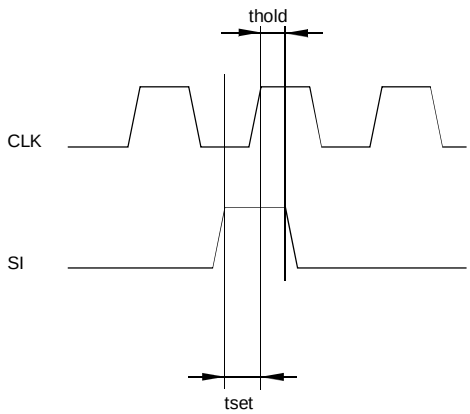



Figure 3: Timing diagram

## DESCRIPTION OF FUNCTIONS

**Normal operation**
Following an internal power-on reset the integration and hold capacitors are discharged and the sample and hold circuit is set to sample mode. A high signal at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle.

In this process the hold capacitors of pixels 1 to 127 are switched to hold mode immediately (SNH = 1), with pixel 128 (SNH128 = 1) following suit one clock pulse later. This special procedure allows all pixels to be read out with just 128 clock pulses. The integration capacitors are discharged by a one clock long reset signal (NRCI = 0) which occurs between the 2nd and 3rd falling edge of the readout clock pulse (cf. Figure 4). After the 127 pixels have been read out these are again set to sample mode (SNH = 0), likewise for pixel 128 one clock pulse later (SNH128 = 0).

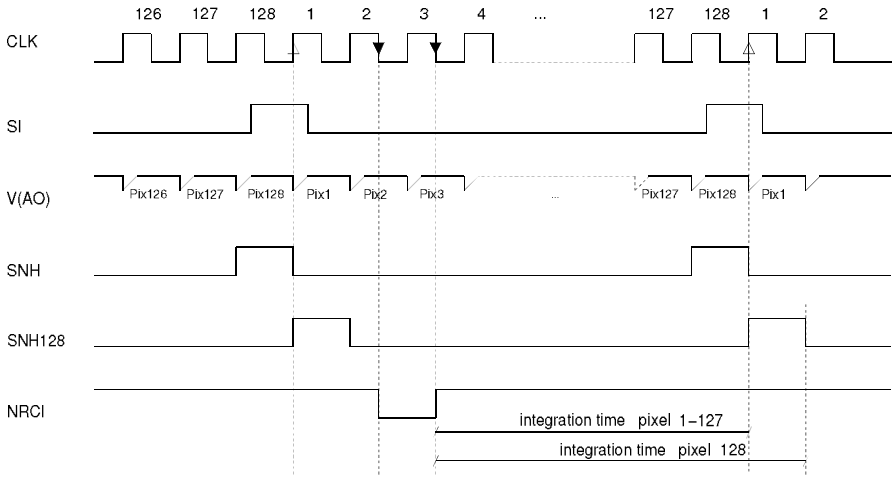



Figure 4: Readout cycle and integration sequence

If prior to the 128th clock pulse a high signal occurs at SI the present readout is halted and immediately reinitiated with pixel 1. In this instance the hold capacitors retain their old value i.e. hold mode prevails (SNH/SNH128 = 0).

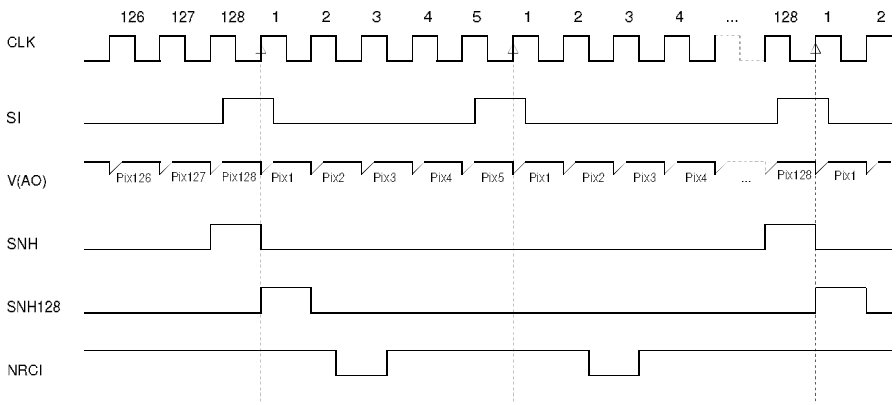



Figure 5: Restarting a readout cycle

With more than 128 clock pulses until the next SI signal, pixel 1 is output without entering hold mode; the output voltage tracks the voltage of the pixel 1 integration capacitor.

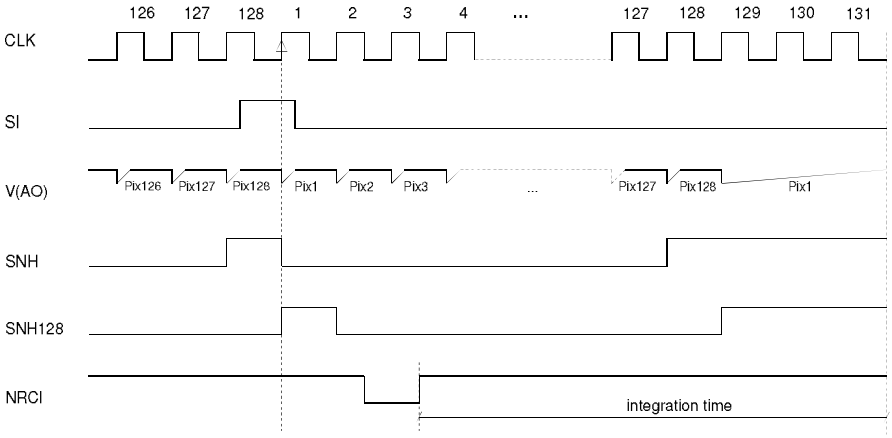



Figure 6: Clock pulse continued without giving a new integration start signal

**Operation with the shutter function**
Integration can be suspended at any time via pin DIS, i.e. the photodiodes are disconnected from their corresponding integration capacitor when DIS is high and the current integration capacitor voltages are maintained. If this pin is open or switched to GND the pixel photocurrents are summed up by the integration capacitors until the next successive SI signal follows.

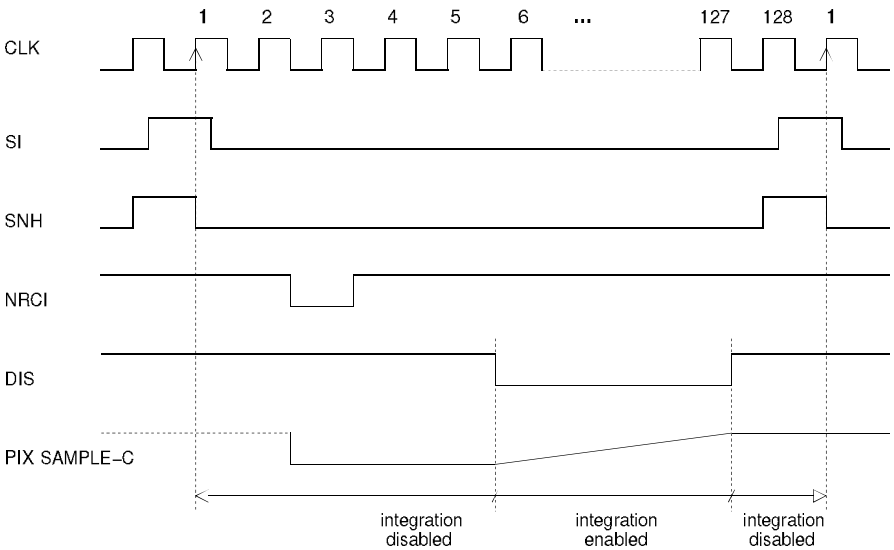



Figure 7: Defining the integration time via shutter input DIS

**External bias current setting**
In order to reduce the power consumption of the device an external reference current can be supplied to pin RSET which reduces the maximum readout frequency, however. To this end a resistor must be connected from VCC to RSET. If this pin is not used, it should be connected to GND.

## ORDERING INFORMATION

| Type | Package | Order Designation |
|---|---|---|
| iC-LF | OLGA LF2C<br>OBGA™ LF3C<br>- | iC-LF OLGA LF2C<br>iC-LF OBGA LF3C<br>iC-LF chip |

For information about prices, terms of delivery, other packaging options etc. please contact:

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