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MC145474/D
Rev. 1

MC145474
MC145475
ISDN S/T Interface Transceiver

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NOTICE
PRODUCT ENHANCEMENT AND DATA UPDATE

This notice outlines changes made to the first and second printings of the Advance Information MC145474/75 data sheet. Changes incorporated into this revision reflect enhancements made to the MC145474/75 ISDN S/T Transceiver as well as additional information gathered to keep up with recent standards and to ensure Motorola's commitment to Total Customer Satisfaction.

Product Enhancements

The following two enhancements are now incorporated into the MC145474/75. The enhanced MC145474 ISDN S/T Transceiver is fully compatible with all previous versions of the chip.

1. Far End Code Violation (FECV) detection
   This enhancement provides an additional interrupt (IRQ #6) that indicates when an FECV has occurred. The following sections of the MC145474/75 data sheet have been changed or added to support this enhancement:

Section 1.3	Features
Section 6.20	$\overline{\text{IRQ}}$ pin
Section 7.5.3.2	NR3(1) IRQ #6
Section 7.6.3	NR4(1) IRQ #6 Enable
Section 10.9	Multiframing — FECV Detection
Section 13.7	Interrupts — IRQ #6

2. Force IDL Transmit
   This enhancement is an additional SCP control bit which allows a TE configured MC145474/75 to continue transmission onto the IDL interface regardless of the state of its transmitter. The TE's receiver, though, must be synchronized to INFO 4 incoming from the NT. The following sections of the MC145474/75 data sheet have been changed or added to support this enhancement:

Section 7.2.2	NR0(2) Transmit Power Down
Section 8.15.7	BR13(1) Force IDL Transmit

General Data Sheet Updates

In addition to the data sheet changes made above due to product enhancement the following sections have also been changed or added:

Section 6.24
Crystal specification changed to include ±100 ppm requirement.

Section 14.3
Description of receive filter delay compensation added.

Section 14.4.1
Recommended transformer vendor addresses updated.

Section 14.4.4
New section added for PCB layout recommendations.

Section 15.9
SCP timing definitions 20, 22 and 23 updated in Figure 15-2.

This document replaces MC145474/D ADI1523.

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SECTION 1
INTRODUCTION

1.1 INTRODUCTION

The MC145474 and the MC145475 provide an economical VLSI layer 1 interface for the transportation of two 64 kpbs B channels and one 16 kbps D channel between the network termination or NT and terminal equipment applications or TEs. Both the MC145474 and the MC145475 conform to CCITT I.430 and ANSI T1.605 specifications.

The MC145474/75 provide the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145474/75 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145474/75 provides the control signals for the interface to the layer 2 devices. Complete multiframe capability is provided.

The MC145474/75 features the interchip digital link (IDL) for the exchange of the 2B+D channel information between ISDN components and systems. The MC145474/75 provides an industry standard serial control port (SCP) to program the operation of the transceiver.

1.2 ORGANIZATION OF DATA SHEET

This data sheet is comprised of fifteen sections. Section 1 is an introduction, serving to outline the features, package types, and pin assignments of the MC145474/75. Section 2 describes the various wiring configurations which are applicable to the MC145474/75, and the operational distances as recommended by CCITT I.430 and ANSI T1.605. Section 3 addresses the activation and deactivation procedures of the MC145474/75.

The MC145474 and MC145475 use the IDL. This is a four wire interface used for full duplex communication between ICs on the board level. Two 64 kbps B channels and one 16 kbps D channel are transmitted and received over this interface. Section 4 is a detailed description of the IDL.

The MC145474 and MC145475 incorporate an SCP interface. The SCP is a four wire interface conforming to an industry standard multi-drop serial link. The SCP is compatible with Motorola's serial peripheral interface (SPI). The SCP makes use of eight nibble registers and sixteen byte registers. Section 5 is a description of the SCP. A per bit description of the nibble and byte registers is as described in Sections 7 and 8, respectively. When the MC145474/75 is configured as a TE it is equipped with five interrupt modes. When configured as an NT, it is also equipped with five interrupt modes. Section 13 is a detailed description of all of these interrupts.

Section 6 contains pin descriptions of the MC145474 and the MC145475. The pin descriptions differentiate between the device configured for NT mode or TE mode of operation.

As mentioned previously, the MC145474/75 is used for the transmission of two 64 kbps B channels and one 16 kbps D channel. Access to the B channels is determined by the network. The TEs gain access to the D channel in accordance with CCITT I.430 and ANSI T1.605 recommendations. A description of the D channel operation is contained in Section 9.

In addition to the 2B+D channels, the S/T transceiver has a multiframing capability. Multiframing is a layer 1 signalling channel for use between the NT and the TE or TEs. Multiframing operation is described in Section 10.

Appendix B of ANSI T1.605 describes a configuration which can be used to support multiple T interfaces. This is known as the NT1 Star mode. This mode of operation is as described in Section 11.

Section 14 describes how to interface the MC145474/75 to the S/T bus. Section 15 contains electrical specifications and data relevant to the MC145474/75.

1.3 FEATURES

The features of the MC145474/75 are described below.

- Conforms to CCITT I.430 and ANSI T1.605 Specifications
- Detects Far-End Code Violations (FECVs) in the NT mode
- Incorporates the IDL
- Pin Selectable NT or TE Modes of Operation
- Industry Standard Microprocessor SCP
- Supports 1:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in all Configurations
- Complete Multiframing Capability Supported (SC1-SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL Loopbacks
- Supports Transmit Power Down and Absolute Minimum Power Mode
- Supports Crystal or External Clock Input Mode
- MC145475 Bonded Out for NT1 Star Mode of Operation
- CMOS Design for Low Power Operation

Note that the MC145475 has the additional feature of supporting the NT1 Star mode of operation. A block diagram of the MC145474/75 is shown in Figure 1-1.

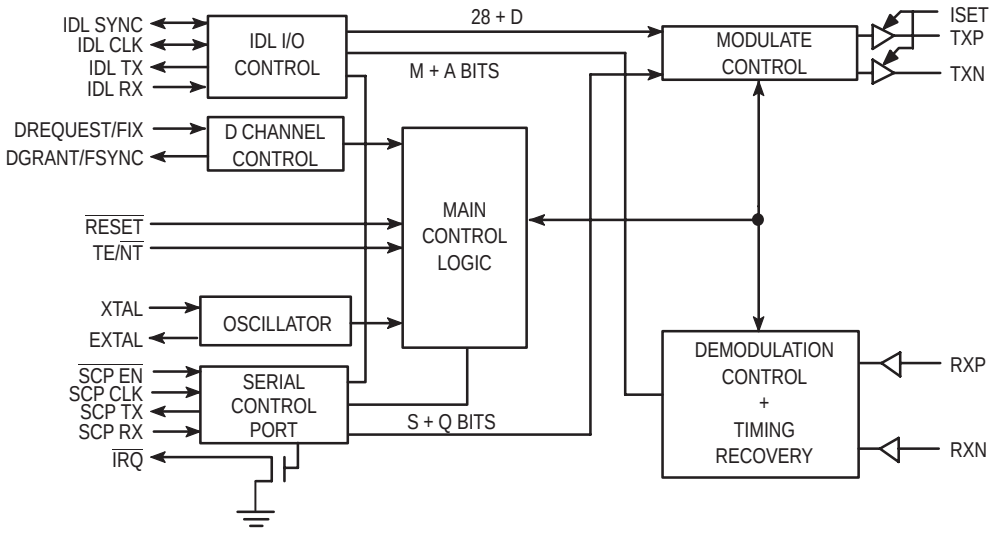


Figure 1-1. MC145474/75 Block Diagram

1.4 PACKAGING

The MC145474 and the MC145475 come in the following packages:

MC145474	22 pin 300 mil wide plastic DIP
MC145475	28 pin 600 mil wide plastic DIP
	28 lead 300 mil SOIC

Note that the only difference between the MC145474 and the MC145475 is that the MC145475 is bonded out for additional support of the NT1 Star mode of operation. The pinouts for the 28 pin MC145475 are identical for both package types. The pin assignments for both the MC145474 and the MC145475 are described in Section 6. Package dimensions are in Section 16.

SECTION 2
WIRING CONFIGURATIONS

2.1 INTRODUCTION

The MC145474/75 ISDN S/T transceiver conforms to CCITT I.430 and ANSI T1.605 specifications. It is a layer 1 S/T transceiver designed for use at the S and T reference points. It is designed for both point to point and multipoint operation. The S/T transceiver is designed for use in either the network terminating (NT) mode or in terminal equipment (TE) applications. Two 64 kbps B channels and one 16 kbps D channel are transmitted in a full duplex fashion across the interface.

Sections 2.2 through 2.6 contain suggested wiring configurations for use. These configurations are deemed to be the most common but by no means the only wiring configurations. Section 14 specifies the recommended circuitry for interfacing the MC145474/75 to the S/T bus. Note that when operating in the TE mode, only one TE has the 100 ohm termination resistors in the transmit and receive paths. Figures 2-1 through 2-4 illustrate where to connect the termination resistors for the described loop configurations.

A description of the most commonly used loop configurations is as described below.

2.2 POINT TO POINT OPERATION

In the point to point mode of operation one NT communicates with one TE. As such, 100 ohm termination resistors must be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 2-1 illustrates this wiring configuration.

When using the MC145474/75 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the DREQUEST/FIX pin low, i.e., connecting it to V_{SS}. Refer to Section 6 for a more detailed description of this pin function. CCITT I.430 and ANSI T1.605 specify that the S/T transceiver must be able to operate up to a distance of 1 km in the point to point mode. This is the distance D1 as shown in Figure 2-1.

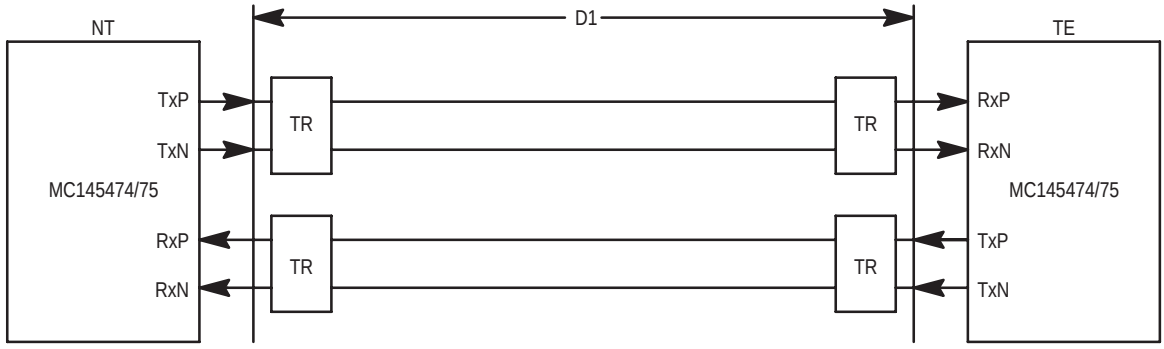


Figure 2-1. Point to Point

2.3 SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 2-2 illustrates this wiring configuration. CCITT I.430 and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2 as shown in Figure 2-2.

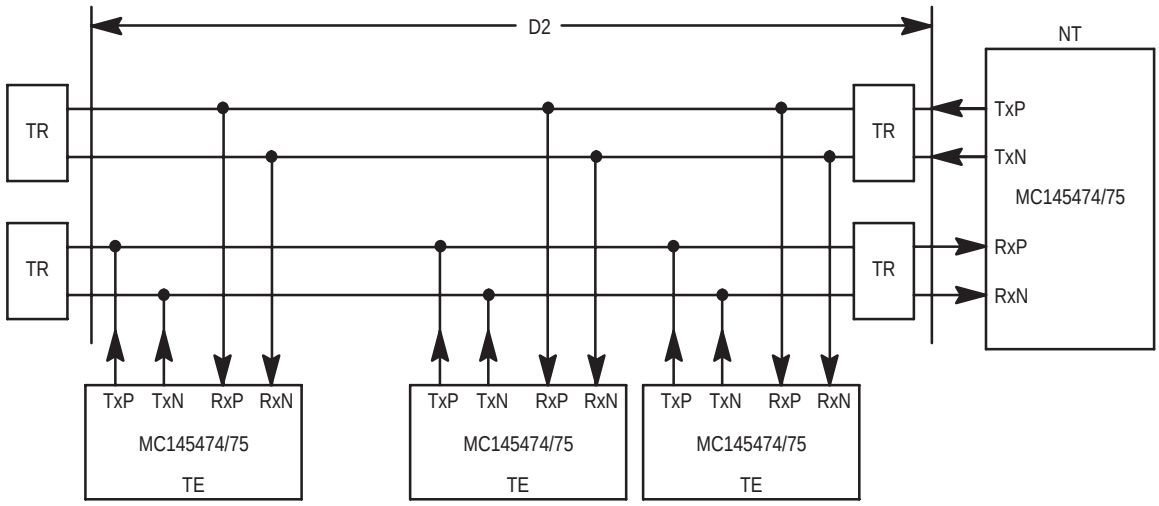


Figure 2-2. Short Passive Bus

2.4 EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the ‘‘Extended Passive Bus.’’ This configuration is as illustrated in Figure 2-3. The termination resistors are to be positioned as illustrated in the diagram.

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance D3 as illustrated in Figure 2-3 corresponds to the maximum distance between the grouping of TEs. CCITT I.430 and ANSI T1.605 specify a distance of 25 to 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4 as shown in Figure 2-3.

Note that the ‘‘NT configured’’ MC145474/75 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the DREQUEST/FIX pin low.

2.5 BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the ‘‘Extended Passive Bus’’ is known as the ‘‘Branched Passive Bus’’ and is illustrated in Figure 2-4. In this configuration the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

2.6 NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the ‘‘NT1 Star Mode of Operation.’’ This mode of operation is supported by the MC145475. This mode is described

in Section 11. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

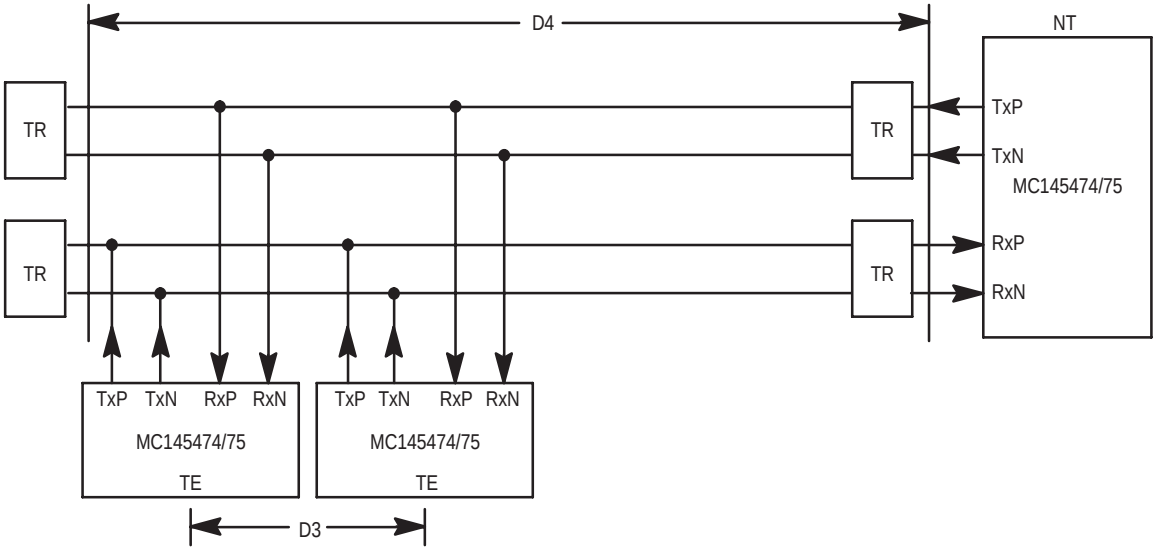


Figure 2-3. Extended Passive Bus

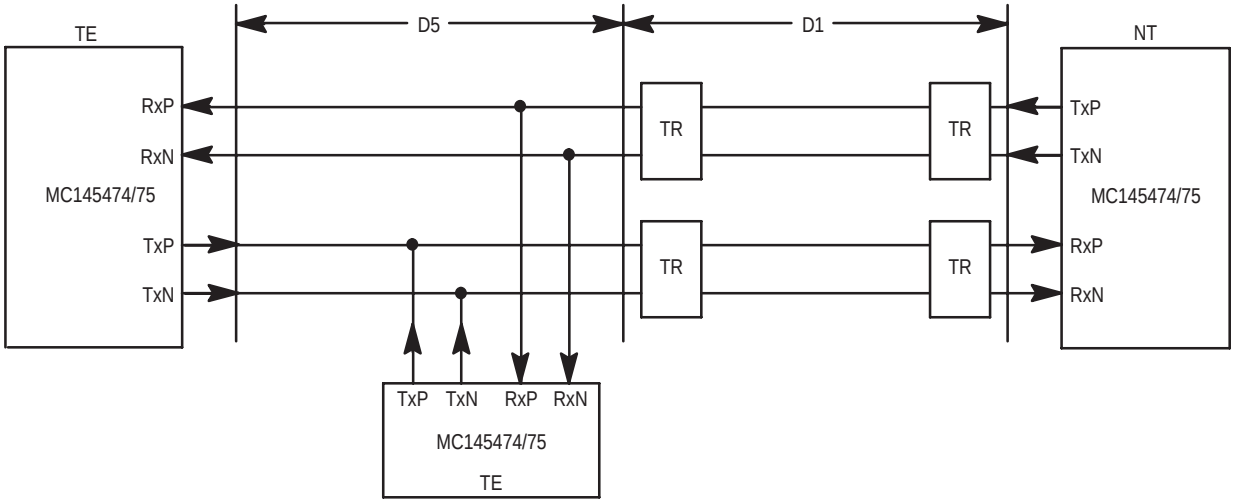


Figure 2-4. Branched Passive Bus

SECTION 3
ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER

3.1 INTRODUCTION

CCITT I.430 and ANSI T1.605 define five information states for the S/T transceiver. When the NT is in the fully operational state it transmits INFO 4. When the TE is in the fully operational state it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TEs transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

3.2 TRANSMISSION STATES FOR NT MODE S/T TRANSCEIVER

When configured as an NT, an S/T transceiver can be in any of the following transmission states shown in Table 3-1.

Table 3-1. NT Mode Transmission States

Information State	Description
INFO 0	The NT transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 2	The NT sets its B1, B2, D, and E channels to ‘0’. The A bit is set to ‘0’ (see Sections 3.11.1 and 3.11.2).
INFO 4	INFO 4 corresponds to frames containing operational data on the B1, B2, D, and E channels. The A bit is set to ‘1’.

3.3 TRANSMISSION STATES FOR TE MODE S/T TRANSCEIVER

When configured as a TE, an S/T transceiver can be in any of the following transmission states shown in Table 3-2.

Table 3-2. TE Mode Transmission States

Information State	Description
INFO 0	The TE transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 1	The TE transmits a continuous signal with the following pattern: positive zero, negative zero, six ones. This signal is asynchronous to the NT.
INFO 3	INFO 3 corresponds to frames containing operational data on the B1, B2, and D channels. If INFO 4 or INFO 2 is being received, INFO 3 will be synchronised to it.

3.4 ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE or TEs. This is accomplished in the MC145474/75 by setting NR2(3) to a ‘1’ (see Section 3.11.3). Note that this bit is internally reset to ‘0’ after the internal activation state machine has recognized its active transition.

The TE or TEs on receiving INFO 2 will synchronize to it and transmit back INFO 3 to the NT. The NT on receiving INFO 3 from the TE will respond with INFO 4, thus activating the loop.

3.5 ACTIVATION OF S/T LOOP BY TE

The TE can activate an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145474/75 by setting NR2(3) to a '1'. Note that this bit is internally reset to '0' after the internal activation state machine has recognized its active transition.

The NT upon detecting INFO 1 from the TE will respond with INFO 2. The TE upon receiving a signal from the NT will cease transmission of INFO 1, reverting to an INFO 0 state. After synchronizing to the received signal and having fully verified that it is INFO 2, the TE will respond with INFO 3, thus activating the loop.

3.6 ACTIVATION PROCEDURES IGNORED

The MC145474/75 has the capability of being forced into the highest transmission state. This is accomplished by setting BR7(7) to a '1'. Thus when this bit is set in the NT, it will force the NT to transmit INFO 4. Correspondingly, in the TE, setting this bit to '1' will force the TE to transmit INFO 3.

Note that CCITT I.430 and ANSI T1.605 specifications allow a TE to be activated by reception of INFO 4, without having to go through the intermediate handshaking. This is to allow for the situation where a TE is connected to an already active loop.

An NT, however, cannot be activated by a TE sending it INFO 3, without going through the intermediate INFO 1, INFO 2, INFO 3, INFO 4 states.

This ''Activation Procedures Ignored'' feature is provided for test purposes, allowing the NT to forcibly activate the TE or TEs. In the TE, the forced transmission of INFO 3 enables verification of the TEs operation.

3.7 FRAME SYNC

3.7.1 NT Mode

When the S/T transceiver in the NT mode is receiving INFO 3 from the TE or TEs and has achieved frame synchronization, it sets the FSYNC signal high. FSYNC is presented on pin 5, when either the MC145474 or the MC145475 is configured as an NT.

Note that FSYNC is also available from the SCP bit NR1(0).

3.7.2 TE Mode

When the TE is receiving either INFO 2 or INFO 4 from the NT, and has achieved frame synchronization, the MC145474/75 will internally set the SCP nibble bit, NR1(0). NR1(0) performs this function in both NT and TE modes, both for the MC145474 and for the MC145475.

When the MC145475 is configured as a TE, FSYNC is available on pin 8.

3.8 ACTIVATION INDICATION

NR1(3), the activation indication bit, is used to signify that the loop is fully active. When the MC145474/75 is configured as an NT this corresponds to the NT transmitting INFO 4 and receiving INFO 3. When the MC145474/75 is configured as a TE, this corresponds to it transmitting INFO 3 and receiving INFO 4. When the loop is in the fully active state, NR1(3) is internally set high.

3.9 DEACTIVATION PROCEDURES

CCITT I.430 and ANSI T1.605 specifications dictate that only an NT can deactivate the S/T loop. Intuitively, this has to be the case, because in a passive bus if one TE sends INFO 0, seeking to deactivate the loop, the other TEs INFO 3 will simply override it.

An NT will transmit INFO 0 to the TE or TEs when it wishes to deactivate the S/T loop. By setting NR2(2) (Deactivate Request) to '1', the NT will deactivate the S/T loop by sending INFO 0 to the TE or TEs. Note that this bit is internally reset to '0' after the internal activation state machine has recognized its active transition.

3.10 INITIAL STATE OF B1 AND B2 CHANNELS

3.10.1 NT

When the MC145474/75 is configured as an NT, NR5(3:2) correspond to ''IDLE B1 channel on S/T loop'', ''IDLE B2 channel on S/T loop'', respectively. The device comes out of a hardware or software reset with these two bits reset to '0'. Thus, the NT comes out of reset with the B1 and B2 channels enabled. When the NT is transmitting INFO 4, data on the B1 and B2 IDL timeslots will be modulated onto the S/T loop. Setting either of these nibble bits in the NT mode will idle the corresponding B channel on the S/T loop. Note that putting a B channel in the IDLE mode affects only the transmitted B channel. The demodulated B data is still transmitted out on IDL Tx, in accordance with the IDL specification.

3.10.2 TE

When the MC145474/75 is configured as a TE, NR5(3:2) corresponds to ''ENABLE B1 channel on S/T loop,'' ''ENABLE B2 channel on S/T loop,'' respectively. The device comes out of a hardware or software reset with these two bits reset to '0'. Thus, the TE comes out of reset with the B1 and B2 channels disabled. When the TE is transmitting INFO 3, data on the B1 and B2 IDL timeslots will not be modulated onto the S/T loop. Setting either of these bits will enable the modulation of the corresponding B channel onto the S/T loop.

Note that although the TE comes out of reset with both B channels in the IDLE mode, this only affects the modulation path. Demodulated data will still be transmitted out of IDL Tx.

3.11 ADDITIONAL NOTES

3.11.1 E Channel

The NT demodulates the 2B+D data received from the TE or TEs. In addition to passing this data onto the network the NT echoes the D channel data back to the TE or TEs using the E echo channel.

This E echo channel is monitored by the TEs and used in the D channel contention algorithm. For a detailed description refer to Section 9.

3.11.2 A Bit

An S/T frame consists of 48 bauds. In the NT to TE direction one of these bauds is for the A bit. The A bit is set to ‘1’ when the S/T loop is in the fully activated state and is set to ‘0’ at all other times. Thus, when the NT is transmitting INFO 2 the A bit is set to ‘0’. When the NT is transmitting INFO 4 the A bit is set to ‘1’.

3.11.3 SCP Nomenclature

There are eight nibble registers and sixteen byte registers in the MC145474/75. These registers are accessed by means of the SCP. NR1(2) refers to nibble register 1, bit 2. Likewise, BR3(4) refers to byte register 3, bit 4.

3.11.4 SCP Indication of Transmit and Receive States

Note that there are two SCP bits, BR11(5:4), used to signify what INFO state the MC145474/75 is receiving. In addition to this, BR11(3:2) are used to signify what INFO state the MC145474/75 is transmitting. Refer to Tables 8-2 and 8-3 for a detailed description of these bits.

SECTION 4
THE INTERCHIP DIGITAL LINK

4.1 INTRODUCTION

The interchip digital link (IDL) is a four-wire interface used for full-duplex communication between ICs on the board-level. The interface consists of a transmit path, a receive path, an associated clock and a sync signal. These signals are known as IDL Tx, IDL Rx, IDL CLK, and IDL SYNC, respectively. The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Five channels of data are exchanged in a 20-bit package every 8 kHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full-duplex communication between the NT and TE.

In addition to these 2B + D channels there are two 8 kbps channels. These two additional channels, known as the IDL A and IDL M channels, are for local communication only, i.e., they are not transmitted from NT to TE or vice versa. Use of these channels is optional. The IDL A and IDL M channels have no effect on the operation of the S/T transceiver. There are two modes of operation for an IDL device: IDL master and IDL slave. If an IDL device is configured as an IDL master, then IDL SYNC and IDL CLK are outputs from the device. Conversely, if an IDL device is configured as an IDL slave, then IDL SYNC and IDL CLK are inputs to the device. Ordinarily the MC145474/75 is configured as an IDL slave when acting as an NT, and as an IDL master when acting as a TE. The exception to this rule is the option to configure the NT as an IDL master. Note that an NT configured MC145474/75 comes out of reset in the IDL slave mode.

4.2 SIGNAL DESCRIPTION

A per-signal description of the four-wire interface follows.

4.2.1 IDL SYNC

This signal is a single positive polarity pulse one IDL CLK cycle in duration. It is periodic at an 8 kHz rate. IDL SYNC is synchronous with IDL CLK with a falling edge of IDL CLK occurring during the high period of IDL SYNC. If the IDL device is configured as an IDL master then IDL SYNC is an output from the device. If the device is an IDL slave then IDL SYNC is an input to the device. Since IDL SYNC is an 8 kHz signal, then in order to exchange two 64 kbps B channels, one 16 kbps D channel, one 8 kbps IDL A channel, and one 8 kbps IDL M channel, the IDL device is required to transmit and receive 20 bits of data every IDL frame. IDL SYNC defines when an IDL exchange is to take place, i.e., IDL SYNC marks the boundary of an IDL frame. Following the falling edge of IDL CLK while IDL SYNC is high, 20 bits of data are exchanged between two IDL devices.

Note that in order to achieve the 144 kbps full-duplex communication (two 64 kbps B channels and one 16 kbps D channel) required for CCITT I.430 and ANSI T1.605 compliance, IDL SYNC must be an 8 kHz signal. This 8 kHz requirement is independent of the choice of IDL CLK rate, the only requirement being that IDL SYNC and IDL CLK are synchronous and that one falling edge of IDL CLK occurs during the high period of IDL SYNC.

4.2.2 IDL CLK

This is a continuous clock used for the transmission and reception of data on the IDL bus. An IDL device will transmit data onto the IDL bus on the 20 rising edges of IDL CLK following the falling edge of IDL CLK that occurred during the high period of IDL SYNC. These 20 bits of data will present themselves to the IDL bus via the IDL Tx pin. An IDL device will accept data from the IDL bus via the IDL Rx pin on the 20 falling edges of IDL CLK that follow the falling edge of IDL CLK that occurred during the high period of IDL SYNC.

If the IDL device is configured as an IDL master, then IDL CLK is an output from the device. If the device is an IDL slave then IDL CLK is an input to the device. If the MC145474/75 is acting as an NT IDL slave (i.e., IDL SYNC and IDL CLK being inputs to the device) then it can accept any of the following ‘‘standard” clock frequencies: 1.536, 1.544, 2.048, 2.56, or 4.096 MHz. IDL CLK can be any frequency in the range 1.536 MHz to 4.1 MHz, the only requirement being that IDL SYNC by synchronous with IDL CLK, be one IDL CLK cycle in duration, and be phase aligned as indicated in Figure 4-1. If the MC145474/75 is acting as an NT IDL master it will output IDL CLK at one of the following frequencies: 1.536, 2.048, or 2.56 MHz. The IDL CLK rate is determined by the setting of BR7(2) and BR13(5) as shown in Table 4-1.

Table 4-1. IDL CLK Rates

BR13(5)	BR7(2)	IDL CLK	
		Rate	Duty Cycle
0	0	2.56 MHz	50%
0	1	2.048 MHz	53.3%
1	X	1.536 MHz	50%

If the MC145474/75 is operating as a TE it will output IDL CLK at either 2.048 or 2.56 MHz. The IDL CLK rate is determined by BR7(2). BR13(5) must be kept equal to ‘0’ in the TE mode.

4.2.3 IDL Tx

Data is transmitted onto the IDL bus via the IDL Tx pin. Once every IDL frame 20 bits of data are transmitted on IDL Tx on the rising edges of IDL CLK. Data is advanced on the first 20 rising edges of IDL CLK following the falling edge of IDL CLK that occurred during the high period of IDL SYNC. The order of transmission is as shown in Figure 4-1. Thus we see that the first eight rising edges of IDL CLK advance the B1 data. The ninth and the nineteenth rising edge transmit the two D bits. The eleventh through the eighteenth rising edge inclusive transmit the second B channel data. The tenth clock transmits the IDL A bit and the twentieth clock transmits the IDL M bit. IDL Tx goes high impedance after the twenty bits have been transmitted.

When the loop is inactive (NR1(3) = ‘0’), IDL Tx will output ‘‘idle ones’’ in the B1, B2, and D time slots. Data will still be output on the IDL A and IDL M time slots. If the MC145474/75 is programmed to enter any of the IDL loopback modes when the S/T loop is inactive, then IDL Tx will become active during the time associated with the channel affected by the loopback.

In normal operation the MC145474/75 S/T transceiver will output data on IDL Tx in the positive logic format, i.e., binary ‘1’ = V_{DD} and binary ‘0’ = V_{SS}. If the device is configured for NT1 Star mode operation (BR13(7) = ‘1’), IDL Tx will go high impedance when transmitting a binary ‘1’ and will continue to output V_{SS} when transmitting a binary ‘0’. This is to facilitate the fact that in NT1 Star mode multiple NTs will have the same IDL SYNC, and hence will output data onto IDL Tx at the same time. Refer to Section 11 for a more detailed discussion.

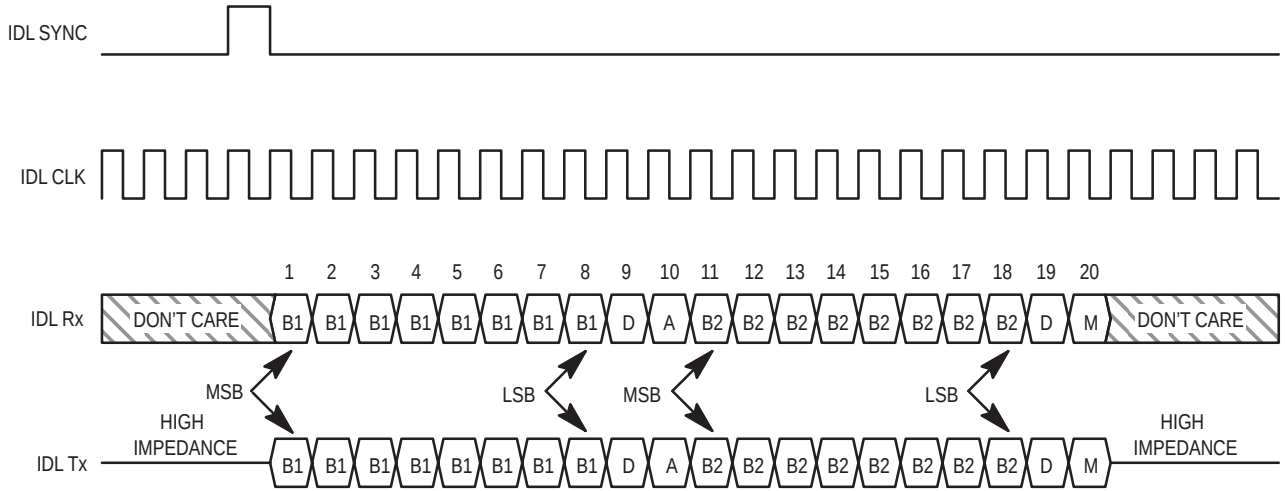


Figure 4-1. Interchip Digital Link

4.2.4 IDL Rx

Data is clocked into an IDL device from the IDL bus via the IDL Rx pin. Data is clocked into an IDL device on the falling edges of IDL CLK. The order in which data is clocked into the device is the same as the order in which it was transmitted, i.e., the first eight bits are B1 data, the ninth and the nineteenth bits are the two D bits, the eleventh through the eighteenth bits inclusive are B2 data, the tenth bit is the IDL A bit and the twentieth bit is the IDL M bit. The twenty bits are clocked into the IDL device on the first twenty falling edges of IDL CLK following the falling edge of IDL CLK which occurs during the high period of IDL SYNC.

4.3 NT IDL SLAVE

This is the normal mode of operation for the MC145474/75 when active as an NT. In this mode IDL SYNC and IDL CLK are inputs to the device. Typically the MC145474/75 when configured as an NT is situated on a line card or an NT1 box. As an IDL slave this allows the S/T chip to derive its timing from the backplane or from the MC145472 U chip. As mentioned previously, IDL SYNC must be 8 kHz while IDL CLK can be input to the device at any of the following frequencies: 1.536, 1.544, 2.048, 2.56, or 4.096 MHz.

When the MC145474/75 is configured as an NT, then BR7(3) determines whether the NT is acting as an IDL master or as an IDL slave. When BR7(3) is a ‘0’ the MC145474/75 when acting as an NT, is behaving as an IDL slave. Conversely, when BR7(3) is set to a ‘1’, the chip when acting as an NT behaves as an IDL master. Upon power up BR7(3) is a ‘0’, and thus the part powers up as an IDL slave if configured as an NT. Note also that a software reset, resets BR7(3) to a ‘0’.

4.4 NT IDL MASTER

As mentioned previously the normal configuration for the MC145474/75 when configured as an NT is as an IDL slave. However, in order to facilitate testing of the environment in which the MC145474/75 resides, the capability exists to configure the chip as an NT IDL master. In this mode of operation the chip outputs IDL SYNC and IDL CLK. These signals are divided down from the 15.36 MHz crystal input and hence are synchronous with it. The NT IDL master mode will also find use in testing PC based local area networks or in passive bus configurations. In these environments it may be required to configure one of the TEs to act as an NT. The NT IDL master enables the user to do this. Writing a ‘1’ to BR7(3) puts the NT into the IDL master mode. Note that a software or a hardware reset, resets this bit to a ‘0’ and hence reconfigures the NT as an IDL slave.

If the MC145474/75 is acting as an NT IDL master, then the IDL CLK can be one of three programmable speeds. The IDL CLK rate is determined by BR7(2) and BR13(5). In NT IDL master mode the IDL CLK is obtained by dividing down from the 15.36 MHz crystal. Application of a software or a hardware reset, resets BR7(2) and BR13(5) to ‘0’. Note that these bits have no application when the MC145474/75 is an NT IDL slave.

4.5 TE IDL MASTER

The MC145474/75 configured as a TE is always an IDL master. In this mode the MC145474/75 derives its timing from the inbound data from the NT. When the TE is receiving either INFO 2 or INFO 4 from the NT it will adaptively phase lock onto it. The TE will set the FSYNC bit (NR1(0)) high when this frame synchronization has been achieved. When this occurs the TE will output IDL SYNC, IDL CLK, and IDL Tx synchronous with the inbound INFO 2 or INFO 4. If the TE is receiving INFO 2 it

will output ‘‘idle ones’’ on IDL Tx in the B1, B2, and D channel timeslots. If the TE is receiving INFO 4 it will output valid data in these timeslots.

Note that when the TE has reached its fully active state (the active state for a TE is when it is receiving INFO 4 from the NT, has phase locked onto it and is transmitting back INFO 3 to the NT) it internally sets the activate indication bit (NR1(3)). In the TE IDL master mode BR7(2) determines the output IDL CLK rate. When BR7(2) is a ‘0’, IDL CLK is a 2.56 MHz 50% duty cycle clock synchronous with the inbound INFO 4. When BR7(2) is a ‘1’ the output IDL CLK is a 2.048 MHz 53.3% duty cycle clock synchronous with the inbound INFO 4.

4.6 TE IDL MASTER FREE RUN

The capability exists in the MC145474/75 to configure the chip as a TE operating in the IDL Master Free Run mode. This is done by setting BR7(3) to a ‘1’. In this mode the TE sends out an IDL CLK and IDL SYNC regardless of the state of the frame synchronization bit (NR1(0)). If NR1(0) is low then IDL SYNC and IDL CLK are derived from the crystal in the same way as in the NT IDL master mode. Upon achieving frame synchronization (i.e., the TE is receiving either INFO 2 or INFO 4 from the NT, has phase locked onto it and has set NR1(0)) IDL SYNC and IDL CLK will become synchronous to the inbound INFO 2 or INFO 4 from the NT. The TE IDL master mode has the capability of providing two clock rates, 2.56 and 2.048 MHz.

4.7 ADDITIONAL NOTES

4.7.1 IDL A and IDL M Bits

The IDL A and IDL M bits are distinct from the S/T A and M bits. The IDL A and IDL M bits are not transmitted from the NT to TE or vice versa. The operation and function of the IDL A and IDL M bits are described fully in Section 12.

4.7.2 Phase Relationship of NTs Transmit Signal with Respect to IDL SYNC

The MC145474/75 operating as an NT behaves as an IDL slave, IDL SYNC and IDL CLK being inputs to the device. IDL SYNC is a single positive polarity pulse one IDL CLK cycle in duration, and is periodic at an 8 kHz rate. The MC145474/75 operating as an NT uses IDL SYNC to correctly position its outbound waveform. Thus the IDL SYNC input to the NT and the NTs outbound INFO 2 or INFO 4 are synchronous. The phase relationship of these signals are shown in Figure 4-2 with a ‘‘close up shot’’ included.

4.7.3 Phase Relationship of TEs Transmit Signal with Respect to IDL SYNC

The MC145474/75 operating as a TE behaves as an IDL master, IDL SYNC, and IDL CLK are outputs from the device. The TE derives its timing from the inbound INFO 2 or INFO 4 from the NT. There is a two baud turn around in the TE in accordance with CCITT I.430 and ANSI T1.605 specifications, i.e., the time between the TEs received ‘‘F bit’’ and is transmitted ‘‘F bit’’ is equivalent to two bauds. This is indicated in Figure 4-3. The TE outputs IDL SYNC, IDL CLK, and IDL Tx when it has achieved frame synchronization. The phase relationship of the TEs transmitted INFO 3 and IDL SYNC is as shown in Figure 4-4 with a ‘‘close up shot’’ included.

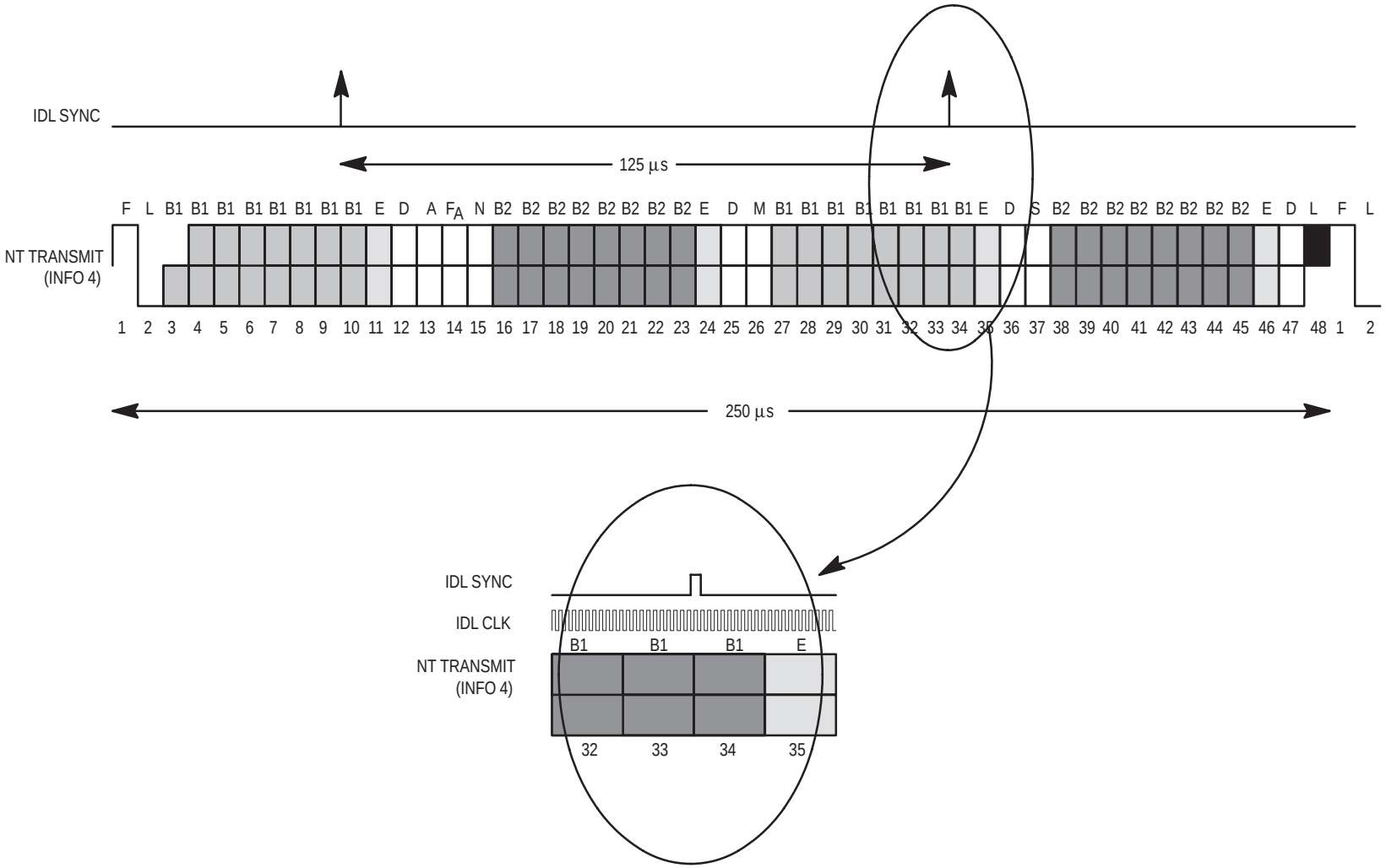


Figure 4-2. Phase Relationship of NT Transmit Signal

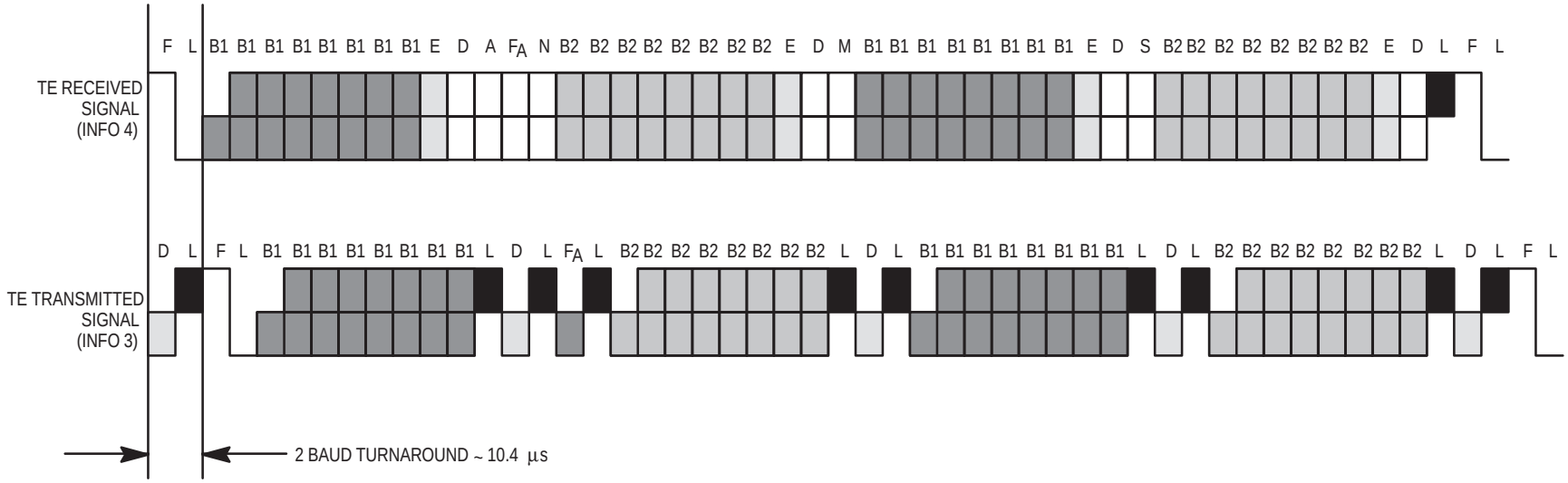


Figure 4-3. Two Baud Turnaround in TE

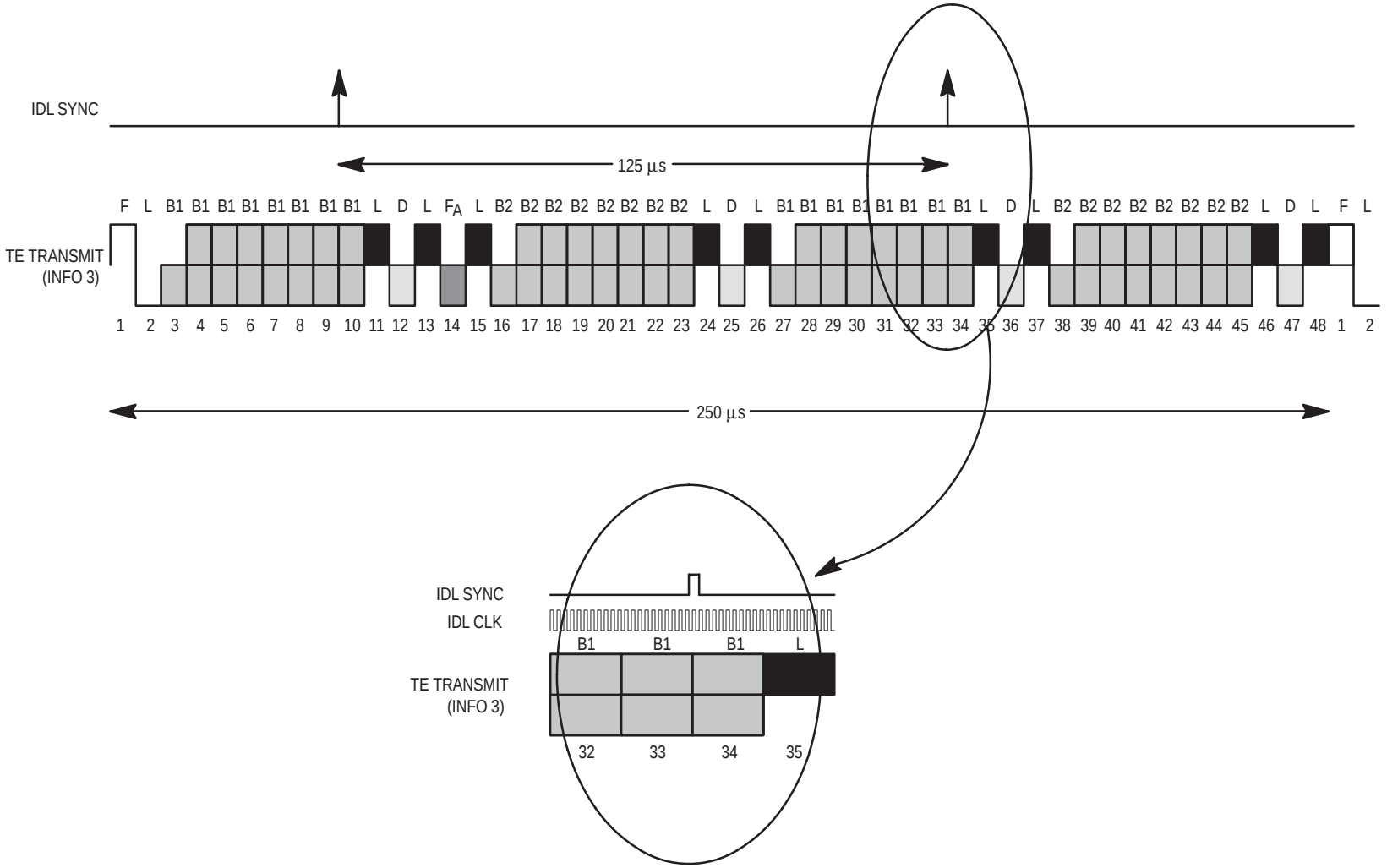


Figure 4-4. Phase Relationship of TE Transmit Signal

SECTION 5
THE SERIAL CONTROL PORT

5.1 INTRODUCTION

The MC145474/75 is equipped with a serial control port (SCP). This SCP is used by external devices (such as an MC145488 DDLC) to communicate with the S/T transceiver. The SCP is an industry standard serial control port and is compatible with Motorola's SPI used on several single chip MCUs.

The SCP is a four-wire bus with control and status bits as well as data being passed to and from the S/T transceiver in a full-duplex fashion. The SCP interface consists of a transmit path, a receive path, an associated clock, and an enable signal. These signals are known as SCP Tx, SCP Rx, SCP CLK, and $\overline{\text{SCP EN}}$. The clock determines the rate of exchange of data in both the transmit and receive directions, and the enable signal governs when this exchange is to take place.

The operation/configuration of the S/T transceiver is programmed by setting the state of the control bits within the S/T transceiver. The control, status, and data information reside in eight 4-bit wide nibble registers and sixteen 8-bit wide byte registers. The nibble registers are accessed via an 8-bit SCP bus transaction. The 16 byte-wide registers are accessed by first writing to a pointer register within the eight 4-bit wide nibble registers. This pointer register (NR(7)) will then contain the address of the byte wide register to be read from or written to, on the following SCP transaction. Thus, an SCP byte access is in essence a 16-bit operation. Note that this 16-bit operation can take place by means of two 8-bit accesses or a single 16-bit access.

5.2 SCP TRANSACTIONS

There are four types of SCP transactions. These are:

1. SCP nibble read
2. SCP nibble write
3. SCP byte read
4. SCP byte write

The following sections contain a discussion on each type of SCP transaction.

5.2.1 SCP Nibble Read

A nibble read is an 8-bit SCP transaction. Figure 5-1 illustrates this process. To initiate an SCP nibble read the $\overline{\text{SCP EN}}$ pin must be brought low. Following this, a Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit followed by three primary address bits (A0-A3), are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCP CLK, following the high to low transition of $\overline{\text{SCP EN}}$. If a read operation is to be performed then R/$\overline{\text{W}}$ should be a '1'. The three address bits clocked in after the R/$\overline{\text{W}}$ bit select which nibble register is to be read. The contents of this nibble register are shifted out on SCP Tx on the subsequent four falling edges of SCP CLK, i.e., the four falling edges of SCP

CLK after the rising edge of SCP CLK which clocked in the last address bit (LSB). $\overline{\text{SCP EN}}$ should be brought back high after the transaction, before another falling edge of SCP CLK is encountered. Note that SCP Rx is ignored during the time that SCP Tx is being driven. Also note that SCP Tx comes out of high impedance only when it is transmitting data.

5.2.2 SCP Nibble Write

A nibble write is an eight bit SCP transaction. Figure 5-2 illustrates this process. To initiate an SCP nibble write the $\overline{\text{SCP EN}}$ pin must be brought low. Following this an R/$\overline{\text{W}}$ bit followed by three primary address bits are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCP CLK following the high to low transition of $\overline{\text{SCP EN}}$. If a write operation is to be performed then R/$\overline{\text{W}}$ should be a '0'. The three address bits clocked in after the R/$\overline{\text{W}}$ bit select the nibble register to be written to. The data shifted in on the next four rising edges of SCP CLK is then written to the selected register. Throughout this whole operation the SCP Tx pin remains in high-impedance state. Note that if a selected register or bit in a selected register is ''read only'' then a write operation has no effect.

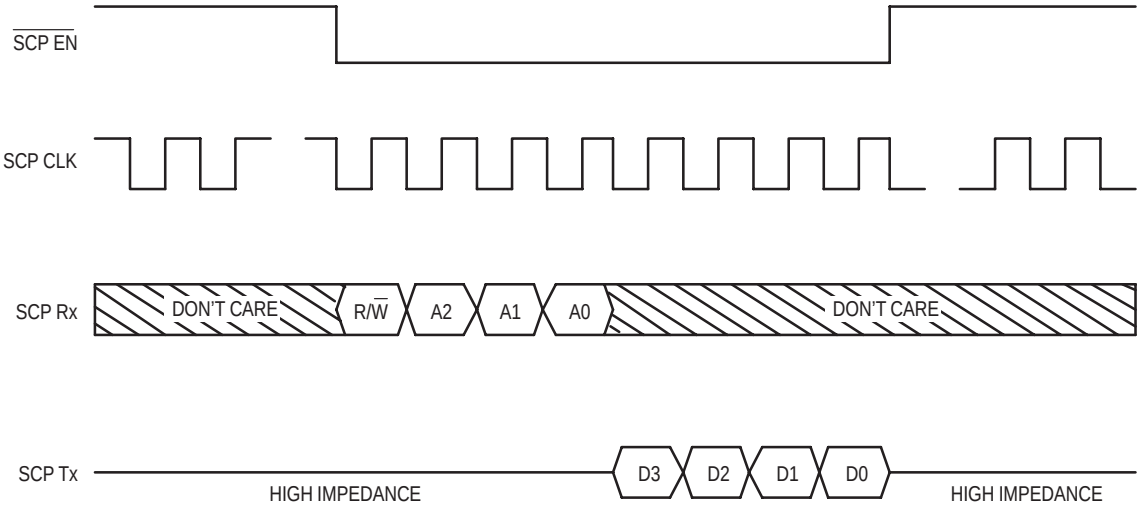
5.2.3 SCP Byte Read

A byte read is a 16-bit SCP transaction. Figure 5-3 illustrates this process. To initiate an SCP byte read the $\overline{\text{SCP EN}}$ must be brought low. Following this an R/$\overline{\text{W}}$ bit is shifted in from SCP Rx on the next rising edge of SCP CLK. This bit determines the operation to be performed, read or write. If R/$\overline{\text{W}}$ is a '1' then a read operation is selected. Conversely, if R/$\overline{\text{W}}$ is a '0' then a write operation is selected. The next three bits shifted in from SCP Rx on the three subsequent rising edges of SCP CLK are primary address bits as mentioned previously. If all three bits are '1' then nibble register 7 is selected (NR7). This is a pointer register, selection of which informs the device that a byte operation is to be performed. When NR7 is selected, the following four bits shifted in from SCP Rx on the following four rising edges of SCP CLK, are automatically written to NR7. These four bits are the address bits for the byte operation. In a read operation the next eight falling edges of SCP CLK will shift out the data from the selected byte register on SCP Tx.

As mentioned previously, an SCP byte access is a 16-bit transaction. This can take place in one 16-bit exchange (Figure 5-3) or two 8-bit exchanges (Figure 5-4). If the transaction is performed in two 8-bit exchanges the $\overline{\text{SCP EN}}$ should be returned high after the first eight bits have been shifted into the part. When $\overline{\text{SCP EN}}$ comes low again the MSB of the selected byte will present itself on SCP Tx. The following eight falling edges of SCP CLK will shift out the remaining eight bits of the byte register. Note that the order in which data is written into the part and read out of the part is independent of whether the byte access is done in one 16-bit exchange or in two 8-bit exchanges.

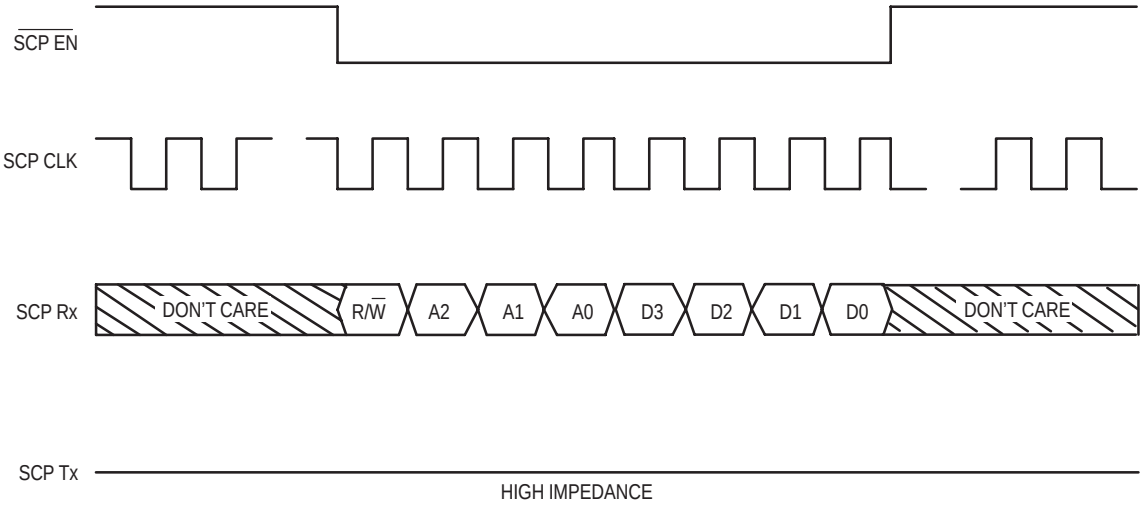
5.2.4 SCP Byte Write

A byte write is also a 16-bit SCP transaction. Figure 5-5 illustrates this process. To initiate an SCP byte write the $\overline{\text{SCP EN}}$ must be brought low. As before, the next bit determines whether the operation is to be read or write. If the first bit is a '0' then a write operation is selected. Again the next three bits read in from SCP Rx on the subsequent three rising edges of SCP CLK must all be '1' in order to select the pointer nibble register (NR7). The following four bits shifted in are automatically written into NR7. As in an SCP byte read these bits are the address bits for the



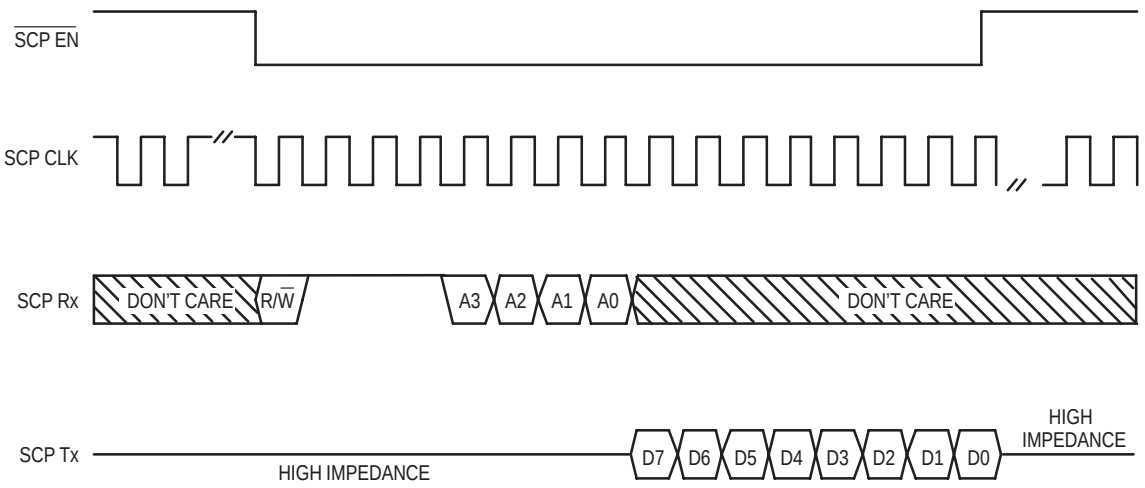
NOTES:
1. R/W = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCP CLK, MSB first.

Figure 5-1. Serial Control Port Nibble Read Operation



NOTES:
1. R/W = 0 for a write operation.
2. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCP CLK, MSB first.

Figure 5-2. Serial Control Port Nibble Write Operation



NOTES:
1. R/W = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCP CLK, MSB first.

Figure 5-3. Serial Control Port Byte Read Operation

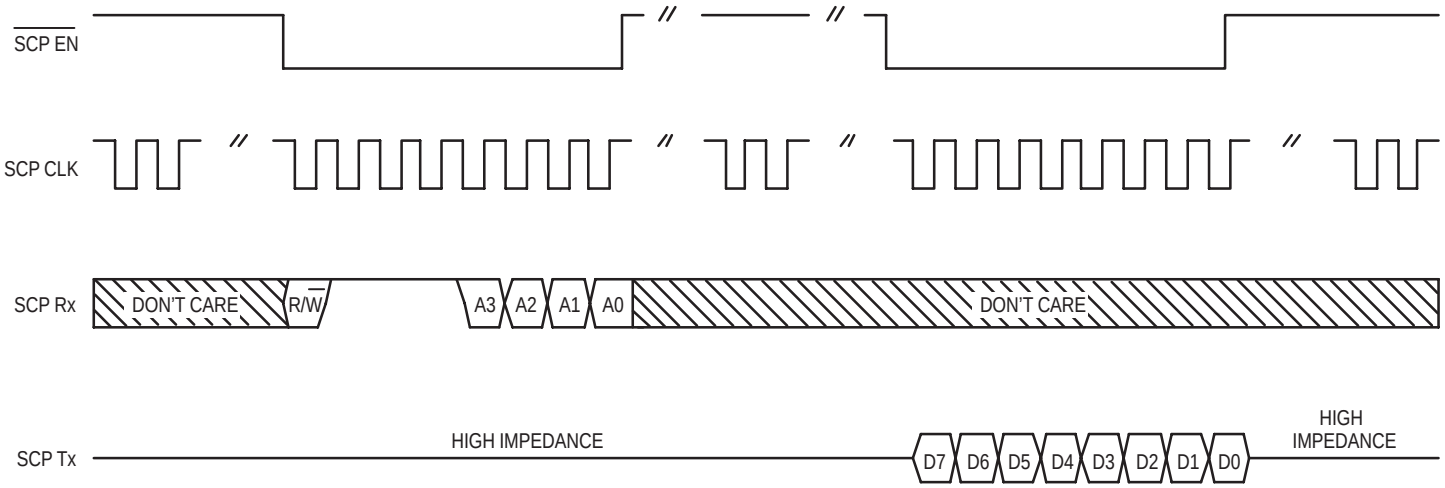
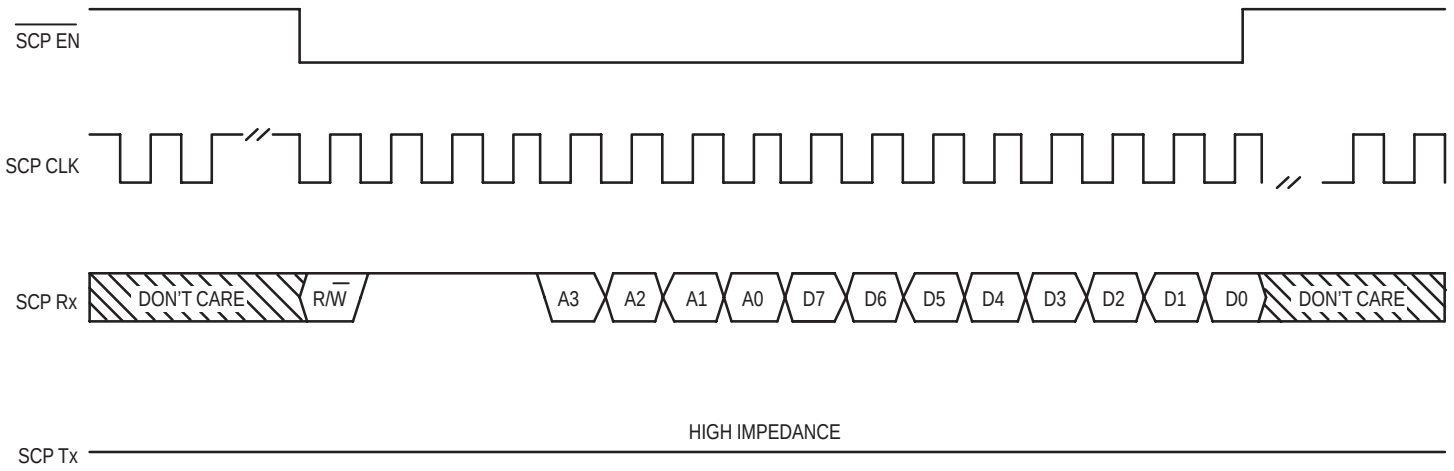


Figure 5-4. Serial Control Port Byte Read Operation
Double 8-Bit Transaction



NOTES
1. R/W = 0 for a write operation.
2. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCP CLK, MSB first.

Figure 5-5. Serial Control Port Byte Write Operation

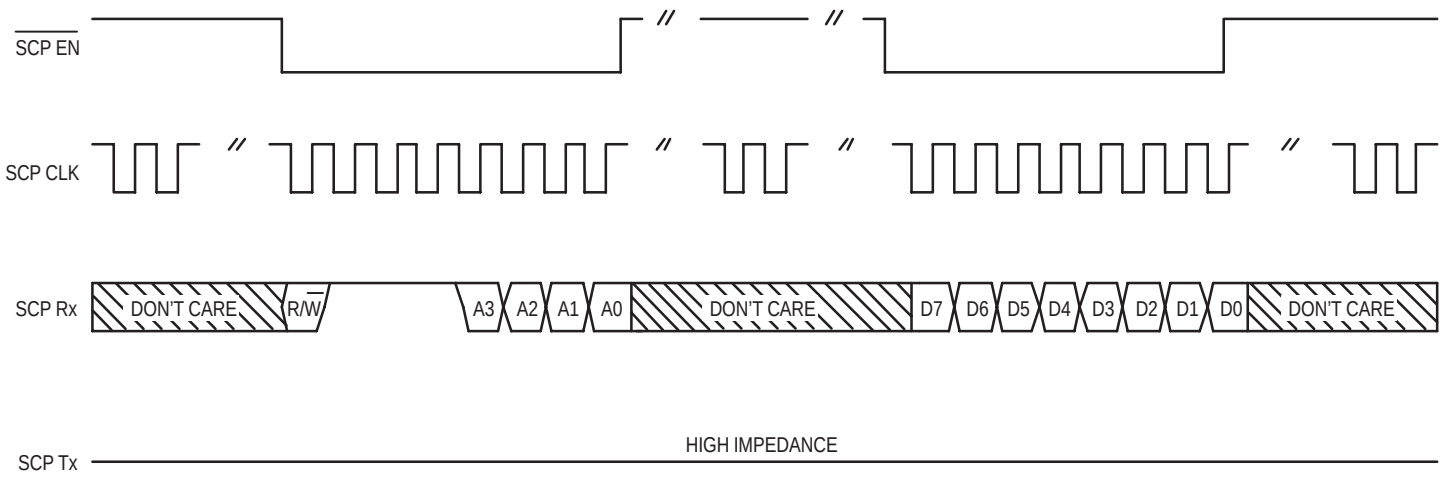


Figure 5-6. Serial Control Port Byte Write Operation
Double 8-Bit Transaction

selected byte register operation. The next eight rising edges of SCP CLK shift in the data from the SCP Rx. This data is then stored in the selected byte register. Throughout this operation SCP Tx will be in a high-impedance state. Note that if the selected byte is ‘‘read only,’’ then this operation will have no effect.

As mentioned previously an SCP byte access is a 16-bit transaction. This can take place in one 16-bit exchange (Figure 5-5) or two 8-bit exchanges (Figure 5-6). If the transaction is performed in two 8-bit exchanges, then $\overline{\text{SCP EN}}$ should be returned high after the first eight bits have been shifted into the part. When $\overline{\text{SCP EN}}$ comes low again, the next eight rising edges of SCP CLK shift data in from SCP Rx. This data is then stored in the selected byte. Figure 5-6 illustrates this process.

5.3 SIGNAL DESCRIPTION

The four signals which constitute the SCP bus are:

1. SCP Tx
2. SCP Rx
3. SCP CLK
4. $\overline{\text{SCP EN}}$

A description of each signal follows

5.3.1 SCP Tx

SCP Tx is used to output control, status, and data information from the MC145474/75 S/T transceiver. The data is output in either 4-bit nibble or 8-bit byte groupings. The data is output in 4-bit nibble groupings during a nibble read and in 8-bit byte groupings during a byte read. Data is shifted out on SCP Tx on the falling edges of SCP CLK, MSB first.

In a nibble read transaction the fourth rising edge of SCP CLK after $\overline{\text{SCP EN}}$ goes low shifts the LSB of the 3-bit nibble address into the MC145474/75. The following falling edge of SCP CLK shifts out the first bit of the selected nibble register (MSB) and takes SCP Tx out of the high-impedance state. The next three falling edges of SCP CLK shift out the other three bits of the selected nibble register. When the last bit has been shifted out (LSB), $\overline{\text{SCP EN}}$ should be returned high. This action returns SCP Tx to a high-impedance state.

In a byte read transaction the eighth rising edge of SCP CLK after $\overline{\text{SCP EN}}$ goes low shifts in the LSB of the 4-bit byte address. The following falling edge of SCP CLK (provided $\overline{\text{SCP EN}}$ is still low) shifts out the first bit (MSB) of the selected byte register and takes SCP Tx out of high-impedance. The next seven falling edges of SCP CLK shift out the remaining seven bits of the selected byte register. When the last bit (LSB) has been shifted out $\overline{\text{SCP EN}}$ should be returned high. This action returns SCP Tx to the high-impedance state.

5.3.2 SCP Rx

SCP Rx is used to input control, status, and data information to the S/T transceiver. Data is shifted into the device on rising edges of SCP CLK. The format for the input of data is as follows: the first bit is the R/$\overline{\text{W}}$ bit (1 = read, 0 = write). This bit selects the operation to be performed on the selected registers within the MC145474/75 S/T transceiver. The next three bits address one of eight specific nibble registers within the MC145474/75 S/T transceiver that the read or write operation is to be

performed on. The address bits are shifted in MSB first. The last four bits are either the data bits (MSB first) that are to be written to the S/T transceiver nibble register (NR0 through NR6), or are four additional address bits (if NR7 had been addressed). These address bits address one of 16 byte wide registers (which are accessed during the next eight cycles of the SCP CLK or a second 8-bit access). SCP Rx is ignored when data is being shifted out on SCP Tx, or when $\overline{\text{SCP EN}}$ is high.

5.3.3 SCP CLK

This is an input to the device used for controlling the rate of transfer of data into and out of the SCP. Data is shifted into the part from SCP Rx on rising edges of SCP CLK. Data is shifted out of the part on SCP Tx on falling edges of SCP CLK. SCP CLK can be any frequency up to 4.096 MHz. An SCP transaction takes place when $\overline{\text{SCP EN}}$ is brought low. Note that SCP CLK is ignored when $\overline{\text{SCP EN}}$ is high, i.e., it may be continuous or it can operate in the burst mode.

5.3.4 $\overline{\text{SCP EN}}$

This signal when held low, selects the SCP for the transfer of control, status, and data information into and out of the MC145474/75 S/T transceiver. $\overline{\text{SCP EN}}$ should be held low for 8 or 16 periods of the SCP CLK signal, in order for information to be transferred into or out of the MC145474/75 S/T transceiver. The phase relationship of $\overline{\text{SCP EN}}$ with respect to SCP CLK is as shown in Figures 5-1 through 5-6 inclusive.

The transition of $\overline{\text{SCP EN}}$ going high will abort any SCP operation in progress, and will force the SCP Tx pin into the high-impedance state.

5.4 SCP HIGH-IMPEDANCE DIGITAL OUTPUT MODE (SCP HIDOM)

The MC145474/75 S/T transceiver has the capability of forcing all output pins of the MC145474/75 (both analog and digital) to the high-impedance state. This feature, known as the ‘‘The Serial Control Port High-Impedance Digital Output Mode’’ or SCP HIDOM is provided to allow ‘‘in circuit’’ testing of other circuits or devices resident on the same PCB, without requiring the removal of the MC145474/75.

The SCP HIDOM mode is entered by holding $\overline{\text{SCP EN}}$ low for a minimum of 33 consecutive rising edges of SCP CLK while SCP Rx is high. After entering this mode, if $\overline{\text{SCP EN}}$ goes high or if SCP Rx goes low the device will exit the SCP HIDOM mode and return to normal operation.

5.5 ADDITIONAL NOTES

5.5.1 Independence of Crystal

The MC145474/75 S/T transceiver operates with a 15.36 MHz crystal frequency. Details of the crystal circuit can be found in Section 6. The SCP operates independently of the 15.36 MHz crystal, i.e., the SCP can be accessed in the presence or absence of the 15.36 MHz input.

5.5.2 SCP Slave

The SCP in the MC145474/75 always operates in the SCP slave mode. The SCP slave mode is defined as having SCP CLK and $\overline{\text{SCP EN}}$ as inputs to the device. Thus any device which communicates with the MC145474/75 via the SCP must be able to operate in the SCP master mode where SCP CLK and $\overline{\text{SCP EN}}$ are outputs. Note that the MC145488 dual data link controller (DDLC) operates in the SCP master mode.

SECTION 6
PIN DESCRIPTIONS

6.1 INTRODUCTION

The Motorola MC145474/75 ISDN S/T transceiver is available in both 22- and 28-pin versions, MC145474 being the 22-pin version (see Figure 6-1) and MC145475 the 28-pin version (see Figure 6-2).

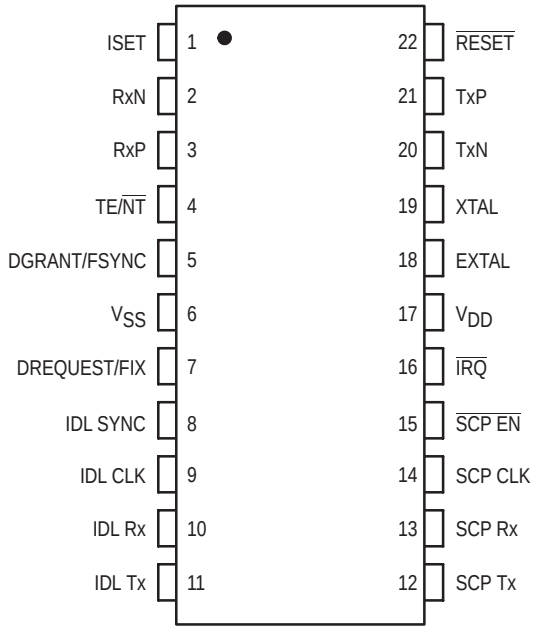


Figure 6-1. MC145474 Pin Assignment

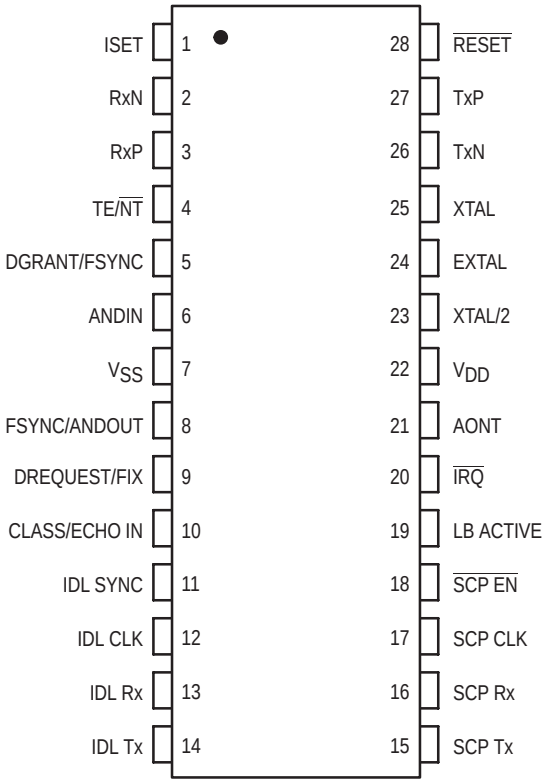


Figure 6-2. MC145475 Pin Assignment

6.2 ISET

In both NT and TE modes of operation, a current programming reference resistor of value 29.4 kilohms accurate to 1% should be connected between this pin and V_{SS}. This resistor provides biasing and programs the current limit for the TxP and TxN driver circuit.

Note that this resistor is not user programmable and must be 29.4 kilohms for CCITT I.430 and ANSI T1.605 compatibility.

6.3 RxN, RxP

In both NT and TE modes these pins are high-impedance differential inputs (>10 kilohm seen at dc looking into the pins differentially) used for coupling the received line signal through a

transformer. The data detection thresholds for logical zeroes and ones are adaptively adjusted by circuitry within the MC145474/75. The receive circuitry of the MC145474/75 S/T transceiver is designed to operate with a 1:1 turns ratio transformer.

6.4 TE/$\overline{\text{NT}}$

This pin is always an input. The setting of this pin determines whether the chip is in NT or TE mode of operation. When this pin is held high the chip is in TE mode. Conversely, when this pin is held low the chip is configured as an NT.

6.5 DGRANT/FSYNC

This pin is always an output from the MC145474/75 S/T transceiver. When the MC145474/75 is configured as a TE this pin performs the DGRANT function. Conversely, when the device is configured as an NT this pin performs the FSYNC function. A description of both functions is as follows.

6.5.1 DGRANT

In the TE mode DGRANT operates as a D channel grant or clear indication. When high this output serves to indicate that the D channel is clear for the programmed priority class and that a layer 2 frame may begin on the next IDL cycle. A high level on the TEs DGRANT output signifies that the TE configured MC145474/75 has counted the appropriate number of consecutive '1' E channel echo bits from the NT for the programmed priority class. This low to high transition of DGRANT is independent of DREQUEST. The DGRANT low to high transition is synchronous with the demodulation of the received E echo bits from the NT. Note that this will always occur prior to an IDL data transfer cycle. Also note that the DGRANT signal actually goes high one received E channel echo bit prior to the programmed priority class selection. This is to accommodate the delay between the input of D channel data via the IDL interface and the line transmission of those bits towards the NT. If at the time of the IDL SYNC pulse falling edge, the DGRANT and the DREQUEST signals are both detected high, the TE mode transceiver will begin FIFO buffering of the input D channel bits from the IDL interface. The control of the FIFO (output of the bits from the FIFO) is governed as illustrated in CCITT recommendation I.430 and ANSI T1.605 specifications.

If the DGRANT signal transitions from high to low while a layer 2 frame is being transmitted (as indicated by the DREQUEST input signal being high) the most recently demodulated E channel echo bit from the NT did not match the previously transmitted D bit, thus indicating that a collision has occurred on the D channel. In such an event the MC145474/75 S/T TE transceiver will automatically force future D channel bits to the ''idle ones'' state until the DGRANT output is again high as well as the DREQUEST being high as discussed previously. NR3(1) is a ''D channel collision'' interrupt. This bit is set every time a collision occurs on the TEs D channel. This will cause an external interrupt to occur if NR4(1) (Enable IRQ #1) is set to '1'.

If the DGRANT line does not transition from high to low while the DREQUEST input is high, the layer 2 frame is assumed to have been transmitted successfully and the DGRANT output will transition from high to low following the transition of the DREQUEST signal from high to low. The MC145474/75 TE mode S/T transceiver will wait until the complete layer 2 frame is transmitted to the NT before forcing the D channel bits to the ''idle ones'' state. The MC145474/75 interprets the transition of DREQUEST from high to low as signalling the end of the layer 2 frame. Following this,

the DGRANT output will return low and the D bit FIFO will be emptied of the remaining layer 2 D channel bits before the transmitted D channel bits are forced to the ‘‘idle ones’’ state. Note that the active polarity of the DREQUEST and DGRANT signals may be reversed by setting the LAPD polarity control bit (BR7(1)) in the SCP. When BR7(1) is a ‘0’ the active polarity is as described above. Conversely when BR7(1) is a ‘1’ the MC145474/75 will drive DGRANT to a logic ‘0’ when DGRANT is active and to a logic ‘1’ when DGRANT is inactive.

6.5.2 FSYNC

When the MC145474/75 is configured as an NT the DGRANT/FSYNC output pin performs the FSYNC output function. The FSYNC function serves to indicate that the MC145474/75 configured as an NT has achieved frame synchronization. Thus when the MC145474/75 is acting as an NT the DGRANT/FSYNC pin will be held high when frame synchronization has been achieved and will be held low when the device has lost frame synchronization.

Frame synchronization is gained and lost in full compliance with CCITT I.430 and ANSI T1.605. The FSYNC output function is also available in the MC145475 when it is configured as a TE. In this case the FSYNC output function is available on the FSYNC/ANDOUT output pin.

6.6 ANDIN

This pin is always an input to the MC145475. This function is only available in the 28-pin MC145475 and is only applicable when the device is configured as an NT. When the device is configured as a TE this pin is ignored.

When the MC145475 is configured as an NT, this pin in conjunction with the demodulated D channel data and the ANDOUT and ECHO IN pins provide the information required to perform the NT1 Star mode operation. When NT1 Star mode is enabled (BR13(7)=1), the demodulated ‘‘D channel’’ data (D channel data received from the TE/TEs) is internally logically ANDed with data on the ANDIN pin. The output from this AND gate presents itself on the ANDOUT pin. Refer to Figure 11-1 for details on how to configure for the NT1 Star mode.

If the MC145475 is not configured for NT1 Star mode of operation, i.e. BR13(7)=‘0’, then the ANDIN pin is pulled low by an internal pull down resistor.

6.7 V_{SS}

This pin is the most negative power supply pin and digital logic ground. It is normally 0 V.

6.8 FSYNC/ANDOUT

This pin is always an output from the MC145475 S/T transceiver. This function is only available in the 28-pin MC145475. When the MC145475 is configured as an NT this pin performs the ANDOUT function. Conversely, when the device is configured as a TE this pin performs the FSYNC function. A description of both functions follows.

6.8.1 FSYNC

When the MC145475 is configured as a TE the FSYNC/ANDOUT output pin performs the FSYNC output function. The FSYNC function serves to indicate that the MC145475 configured as a TE has

achieved frame synchronization. Thus, when the MC145475 is acting as a TE the FSYNC/ANDOUT pin will be held high when frame synchronization has been achieved, and will be held low when the device has lost frame synchronization.

Frame synchronization is gained and lost in full compliance with CCITT I.430 and ANSI T1.605. The FSYNC output function is also available in the MC145474 when it is configured as an NT. When the MC145474 is configured as an NT the FSYNC output function is available on the DGRANT/FSYNC output pin.

6.8.2 ANDOUT

When the MC145475 is configured as an NT the FSYNC/ANDOUT output pin performs the ANDOUT output function. The ANDOUT function in conjunction with the demodulated D channel data and the ANDIN and ECHO IN pins provide the information required to perform the NT1 Star mode of operation. When NT1 Star mode is enabled (BR13(7)=1) the demodulated D channel data (D channel data received from the TE or TEs) is internally logically ANDed with the data on the ANDIN pin. The ANDOUT pin is the resultant output of the AND gate.

6.9 DREQUEST/FIX

This pin is always an input to the MC145474/75 S/T transceiver. When the MC145474/75 is operating as a TE this pin performs the DREQUEST input function. Conversely, when the device is operating as an NT this pin performs the FIX function.

6.9.1 DREQUEST

When the MC145474/75 is configured as a TE the DREQUEST/FIX input pin performs the DREQUEST function. In the TE mode, this pin is used to indicate to the MC145474/75 that an external device wishes to transmit a layer 2 frame to the NT on the D channel. The MC145474/75 internally samples DREQUEST on the falling edge of IDL SYNC. If the DGRANT output and the DREQUEST input are both high at this point in time, the TE configured transceiver will assume that D channel information input on that same IDL cycle is the beginning of a layer 2 frame, and will begin the FIFO buffering of the input D channel bits from the IDL interface. This FIFO is four bits deep. The control of the FIFO (output of the bits from the FIFO) is governed as diagrammed in Annex B of the CCITT I.430 recommendation and Appendix D of the ANSI T1.605 specification.

Upon the commencement of D channel FIFO buffering the MC145474/75 continues to monitor the DREQUEST input by sampling it every falling edge of IDL SYNC. When DREQUEST has been sampled to have returned low again the TE configured MC145474/75 will assume that the last bit or bits of the layer 2 frame were contained in the previous IDL data transfer and will ignore future D channel bits input on the IDL interface (i.e., D bits following the end of the layer 2 frame), forcing the transmitted D bits to the ‘‘idle ones’’ state. The MC145474/75 will then prepare for the next layer 2 frame according to the priority class procedures outlined in CCITT I.430 and ANSI T1.605. Note that the active polarity of the DREQUEST and DGRANT signals may be reversed by setting the LAPD polarity control bit (BR7(1)) in the SCP. When BR7(1) is a ‘0’ the active polarity is as described above. Conversely, when BR7(1) is a ‘1’ the MC145474/75 interprets a ‘0’ on DREQUEST as being active.

6.9.2 FIX

When the MC145474/75 is configured as an NT the DREQUEST/FIX input pin performs the FIX function. The MC145474/75 S/T transceiver configured as an NT can use either an adaptive timing

or a fixed timing scheme as the timing recovery method used by the transceiver's demodulator to sample the incoming transmission from the TE/TEs.

In adaptive timing a digital phase locked loop (DPLL) is employed to optimally position the demodulator clock relative to the incoming baud from the S/T interface. In fixed timing mode the demodulator clock is maintained at a fixed position relative to the transmitted baud from the NT. When the MC145474/75 is configured as an NT a logic '1' on the DREQUEST/FIX pin selects the fixed timing mode and a logic '0' selects the adaptive timing mode.

The MC145474/75 configured as a TE always uses the adaptive timing scheme. When the device is acting as an NT in point to point and extended passive bus arrangements, the adaptive timing scheme must be employed. The fixed timing mode is provided as an optional timing scheme for use in the point to multipoint short passive bus wiring configuration. However, the performance of the DPLL and choice of timing recovery algorithm employed in the MC145474/75 S/T transceiver allows the use of adaptive timing in the NT for all wiring configurations, including the point to multipoint short passive bus arrangement. Thus, it is recommended that adaptive timing always be used.

6.10 CLASS/ECHO IN

This pin is always an input to the MC145475 S/T transceiver. When the MC145475 is operating as an NT this pin performs the ECHO IN function. Conversely, when the MC145475 is operating as a TE this pin performs the CLASS function. A description of both functions follows.

6.10.1 CLASS

When the MC145475 is configured as a TE the CLASS/ECHO IN pin performs the CLASS function. In this mode, the class input pin is internally logically ORed with NR2(0). The output of this internal OR gate determines the class of the TE for D channel operation. Thus, if CLASS/ECHO IN is held low the class selection is determined via NR2(0). Alternatively, if an application calls for changing the class of the TE without having to do an SCP access, then NR2(0) should be left in the logic '0' state and the class can then be determined via the CLASS/ECHO IN input pin.

When the output of the internal OR gate is '0' the priority class for D channel messages sent by a TE configured device is set to the signalling or highest priority class (i.e., Class 1 operation). When the output of the internal OR gate is a '1', Class 2 operation is selected. The definition and functionality of the class configuration of the MC145474/75 is fully compliant with CCITT I.430 and ANSI T1.605. Note that the CLASS/ECHO IN pin is not available in the 22-pin MC145474. Using this device the class can be chosen for D channel operation when operating as a TE via NR2(0). Refer to Section 9 for a detailed description of the D channel operation.

6.10.2 ECHO IN

When the MC145475 is configured as an NT the CLASS/ECHO IN pin performs the ECHO IN input function. The ECHO IN function in conjunction with the demodulated D channel data and the ANDIN and the ANDOUT pins provides the information required to perform the NT1 Star mode of operation. When NT1 Star mode is enabled (BR13(7)=1), data on the CLASS/ECHO IN pin is used by the NT (instead of the demodulated D bits) to send back to the TE/TEs as the E channel.

6.11 IDL SYNC

This pin is part of the IDL. The IDL SYNC pin is bi-directional. When the MC145474/75 is operating as an IDL slave, this pin is an input to the device. Conversely, when the device is operating as an IDL master, this pin is an output. The MC145474/75 configured as an NT comes out of reset as an IDL slave. The NT configured device can be programmed to act as an IDL master by setting BR7(3). The MC145474/75 acting as a TE is always an IDL master. IDL SYNC is a single positive polarity pulse, one full IDL CLK cycle in duration. IDL SYNC occurs in the bit period immediately preceding the IDL data transaction.

The IDL SYNC signal is to be periodic at 125 μs intervals. The IDL SYNC input in combination with the IDL CLK input conveys the networks timing information to the NT IDL slave device. Data is shifted into the MC145474/75 via IDL Rx on the first 20 falling edges of IDL CLK after the falling edge of IDL CLK which occurred during the high period of IDL SYNC. Data is shifted out of the device on the first 20 rising edges of IDL CLK after falling edge of IDL CLK which occurred during the high period of IDL SYNC.

In the TE configured MC145474/75, IDL SYNC is leading edge aligned with IDL CLK, is one IDL CLK period in duration and is periodic at a 125 μs rate. The position of the TEs IDL SYNC relative to the TEs transmitted INFO 3 is phase locked to the incoming transmission from the NT, when the TE device is receiving either INFO 2 or INFO 4. When the TE device has no timing information from the NT (i.e., it has not recognized either INFO 2 or INFO 4) it's IDL SYNC output has the option of free running or to be held low, as programmed by the IDL FREE RUN bit in the SCP (BR7(3)).

6.12 IDL CLK

This pin is part of the IDL. The IDL CLK pin is bi-directional. When the MC145474/75 is operating as an IDL slave, this pin is an input to the device. Conversely, when the device is operating as an IDL master, this pin is an output. The MC145474/75 configured as an NT comes out of reset as an IDL slave. The NT configured device can be programmed to act as an IDL master by setting BR7(3). The MC145474/75 acting as a TE is always an IDL master. IDL CLK is used for the input and output of digital data. Twenty bits of data are input simultaneous with the output of 20 bits via the IDL Rx and IDL Tx pins, respectively. The data transfers take place on the 20 IDL CLK cycles immediately following the IDL SYNC pulse. Data is clocked into the MC145474/75 via the IDL Rx pin on the first 20 falling edges of IDL CLK following IDL SYNC. Data is shifted out of the device on the first 20 rising edges of IDL CLK following IDL SYNC.

When the MC145474/75 S/T transceiver is operating as an NT IDL slave it can accept any of the following frequencies for IDL CLK: 1.536,1.544, 2.048, 2.56 or 4.096 MHz. IDL SYNC should be 8 kHz and be one IDL CLK cycle in duration. When the MC145474/75 S/T transceiver is operating as an NT IDL master it will output IDL CLK at one of the following frequencies: 1.536, 2.048 or 2.56 MHz. The IDL CLK rate is determined by the setting of BR7(2) AND BR13(5). IDL SYNC will be one IDL CLK period in duration and will be at an 8 kHz rate. When the MC145474/75 S/T transceiver is operating as a TE IDL master it will output IDL CLK at one of the following frequencies: 2.048 or 2.56 MHz. The IDL CLK rate is determined by BR7(2). IDL SYNC will be one IDL CLK period in duration and will be at an 8 kHz rate.

6.13 IDL Rx

This pin is part of the IDL and is always an input to the MC145474/75 S/T transceiver. Data is read into the MC145474/75 from the IDL bus via the IDL Rx pin. Data is read into the device on the first

20 falling edges of IDL CLK following the falling edge of IDL CLK that occurred during the high period of IDL SYNC. IDL Rx is ignored at all other times. The data read into the MC145474/75 is interpreted as follows: V_{SS} corresponds to binary '0', V_{DD} corresponds to binary '1'.

6.14 IDL Tx

This signal is part of the IDL and is always an output from the MC145474/75 S/T transceiver. Data is transmitted onto the IDL bus via the IDL Tx pin. The IDL Tx pin is active (i.e., drives the pin with data) during the 20 IDL clock cycles following the IDL SYNC pulse. Data is transmitted out on IDL Tx on the first 20 rising edges of IDL CLK following the falling edge of IDL CLK that occurred during the high period of IDL SYNC. At all other times IDL Tx is held in a high-impedance state.

An active loop is one where an NT is transmitting INFO 4 and receiving INFO 3 and one or more TEs are receiving INFO 4 and transmitting INFO 3. (When the loop is active, NR1(3) the activate indication bit in the SCP, will be set high). When the loop is active IDL Tx will output 20 bits of data every IDL frame. When the loop is inactive IDL Tx will only output the IDL M and IDL A bits. IDL Tx will be in the ''idle ones'' state in the B1, B2, and D channel slots, and will be high-impedance elsewhere. If the MC145474/75 is programmed to enter any of the IDL loopback modes when the loop is inactive then IDL Tx will be active during the time associated with the channel affected by the IDL loopback.

When the MC145474/75 S/T transceiver is configured as a TE, the device behaves as an IDL master, i.e., IDL SYNC and IDL CLK are outputs. In this case, IDL SYNC and IDL CLK will not be output until an active loop condition has been reached. IDL Tx will remain in the high-impedance state until this time. An exception to this is when the TE is programmed for the IDL FREE RUN mode (BR7(3) = 1), where IDL SYNC and IDL CLK free run until an active loop condition has been reached. In this situation IDL Tx will output ''idle ones'' in the B1, B2, and D channel timeslots. In normal operation the MC145474/75 S/T transceiver will output data on IDL Tx in the positive logic format, i.e., binary '1' = V_{DD} and binary '0' V_{SS}. If the device is configured for NT1 Star mode operation (BR13(7) = '1'), IDL Tx will go high-impedance when transmitting a binary '1' and will continue to output V_{SS} when transmitting a binary '0'. This is to facilitate the fact that in NT1 Star mode multiple NTs have the same IDL SYNC, and hence will output data onto IDL Tx at the same time. Refer to Section 11 for a more detailed discussion.

6.15 SCP Tx

The serial control port transmit line is used to output control, status, and data information from the MC145474/75 S/T transceiver. The information is output in either 4-bit nibble or 8-bit byte groupings. The data is output on falling edges of SCP CLK, MSB first. The SCP Tx line is only driven to the valid logic state during the timeslot associated with that data during a read operation. The SCP Tx line is in the high-impedance state at all other times.

6.16 SCP Rx

The serial control port receive line is used to input control, status, and data information into the MC145474/75 S/T transceiver. The format for the input of data is as follows: the first bit is the Read/$\overline{\text{Write}}$ bit (1 = read, 0 = write). This bit selects the operation to be performed on the selected registers within the MC145474/75 S/T transceiver. The next three bits address one of eight specific nibble registers within the device that the read or write operation is to be performed on. The address

bits are shifted in MSB first. The last four bits are either the data bits that are to be written to the S/T transceiver's nibble registers (NR0 to NR6) or four additional address bits, if nibble register 7 (NR7) had been addressed. If NR7 has been addressed, these four bits address one of the 16-bit wide registers. These byte registers are then accessed during the next eight cycles of the SCP CLK or on a second 8-bit SCP access. Data is shifted into the device on rising edges of SCP CLK. Data on SCP Rx is ignored while data is being shifted out on SCP Tx during a read access. SCP Rx is ignored while $\overline{\text{SCP EN}}$ is high.

6.17 SCP CLK

The serial control port clock is used to clock control, status, and data information into and out of the MC145474/75 S/T transceiver. The SCP CLK signal may be continuous or be operated in the burst mode. SCP CLK may be any frequency up to 4.1 MHz. Data is serially shifted out of the MC145474/75 via the SCP Tx line on falling edges of SCP CLK. Data is serially shifted into the device via the SCP Rx line on rising edges of SCP CLK.

6.18 $\overline{\text{SCP EN}}$

This signal when held low selects the SCP for the transfer of control, status, and data information into and out of the MC145474/75 S/T transceiver. The $\overline{\text{SCP EN}}$ input is to be held low for 8 or 16 periods of the SCP CLK signal in order for information to be transferred into and out of the device. $\overline{\text{SCP EN}}$ transitions low to initiate an SCP access.

6.19 LOOPBACK ACTIVE

This pin always an output from the device. If any of the loopbacks are invoked, or any combination of the loopbacks are invoked then this pin will be held high, i.e., if any of the IDL loopbacks and/or any of the T loopbacks and/or if the analog loopback is enabled, this pin will be at the logic '1' level. The loopback active pin will be held low when all loopbacks are disabled, i.e., normal operation. This function is independent of whether the device is configured as an NT or as a TE. Note that this ''loopback active'' feature is available only in the MC145475 28-pin version.

6.20 $\overline{\text{IRQ}}$

The interrupt request active low pin is an active low open drain output used to signal MPU or MCU devices that an interrupt condition exists in the MC145474/75 S/T transceiver. On clearing the interrupt condition the $\overline{\text{IRQ}}$ pin is returned to the high-impedance state. IRQ #3 is cleared by writing a '0' to NR3(3). IRQ #2 is cleared by reading BR3. IRQ #1 is cleared by writing a '0' to NR3(1) in the TE mode. Writing a '0' to NR3(1) in the NT mode will clear IRQ #6. Refer to Table 7-1, Table 7-2 and Section 13 for a more detailed analysis. Note also that all interrupt conditions are maskable.

6.21 AONT

This pin is always an input to the device. The active only NT feature is applicable only to the NT mode of operation and is available only in the MC145475 28-pin version of the device. When using the MC145475 configured as NT, this input pin is essentially an external AR (activate request). Logically, this pin is internally ''ORed'' with NR2(3) to form the activate request function. Thus, if this pin is brought high the NT will transmit INFO 2 onto the line if it had been transmitting INFO 0. AONT

is internally sampled once every 250 μs in the MC145475. Thus, AONT should be held high for at least 250 μs to initiate an activate request.

The MC145475 will continue to transmit INFO 2 and will only cease to do so if it receives a DR (deactivate request NR2(2)), an activation timer #1 expire input (NR2(1)), or if it receives INFO 3. This is in keeping with CCITT I.430 and ANSI T1.605. If INFO 3 is returned to the ''NT configured'' MC145475 in response to INFO 2, then the NT will cease transmission of INFO 2 and respond with INFO 4. The AONT pin essentially enables the MC145475 to activate the S/T loop without necessitating a microprocessor. The AONT function is ignored when the MC145474/75 is configured as a TE.

6.22 V_{DD}

This pin is the positive power supply input to the MC145474/75 and is 5.0 V ± 10% with respect to V_{SS}.

6.23 XTAL/2

This pin is always an output from the device. The MC145474/75 S/T transceiver requires a 15.36 MHz clock source for operation. This 15.36 MHz clock is internally divided by two and the output of this divider (7.68 MHz) presents itself on the XTAL/2 pin. Note that this feature is only available on the 28-pin MC145475 device. Using the MC145475 device, this pin function is independent of the mode of operation, i.e., whether the device is configured as an NT or as a TE. As long as power is supplied to the MC145474/75, this function is operational, i.e., this function is unaffected by any of the power down or reset modes.

6.24 XTAL AND EXTAL

The MC145474/75 S/T transceiver requires a 15.36 MHz clock source for operation. This can be provided by a 15.36 MHz resonant crystal circuit using XTAL and EXTAL as the terminals of the circuit, or an external 15.36 MHz clock source can be input to the device via the XTAL pin. An inverter is internally connected between XTAL and EXTAL with XTAL as the input to the inverter and EXTAL as the output.

When the parallel resonant crystal circuit option is employed the crystal should be connected across the XTAL and EXTAL pins. The crystal should be a 15.36 MHz AT cut quartz crystal, cut for an 18 pF load capacity. The frequency tolerance of this crystal should be at most ± 100 ppm. The MC145474/75 has been optimized for an M-TRON crystal cut to the mentioned specifications. This then requires that both XTAL and EXTAL be decoupled to V_{SS} by 30 pF capacitors. In addition, a 10 megohm resistor should be connected between XTAL and EXTAL. Figure 6-3 is an illustration of this crystal circuit. This crystal resonant circuit is optimized for minimum RF emissions and power dissipation.

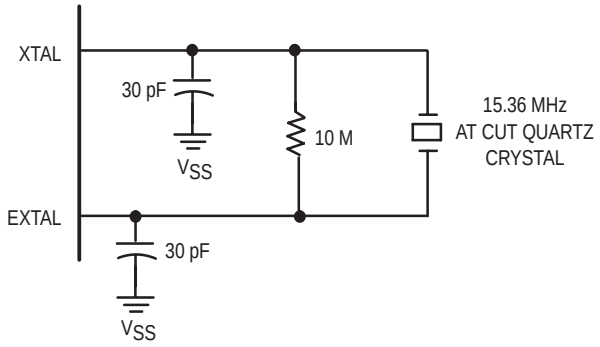


Figure 6-3. Crystal Circuit

6.25 TxP, TxN

In both NT and TE modes of operation these pins act as differential current limited voltage source drive pairs for creating the logical line signals. When a logical one line signal is to be created, these lines present a high-impedance source (> 60 kilohms seen differentially at dc). In multipoint wiring configurations the wiring polarity in the TE to NT direction must be maintained. (Note that the TxP/TxN drive pair will supply current such that a positive potential is created between the TxP and TxN pair, respectively, when transmitting the F bit of each frame). The TxP/TxN drive pair operate as a 1.17 V current limited voltage source. As such, two series resistors of 1% tolerance should be inserted in the line interface circuit so that the combined resistance of these two resistors and the winding resistance of the transformer is 26.4 ohms. The drive circuitry of the MC145474/75 S/T transceiver is designed to interface to the transmission pair via a 1:1 transformer.

The TxP and TxN line drive circuit of the MC145474/75 is designed such that the device will continue to provide a high-impedance circuit to the transmit pair of the S/T loop when power is removed from the part (i.e., when the circuit between V_{DD} and V_{SS} becomes a short circuit).

6.26 $\overline{\text{RESET}}$

This pin is always an input to the MC145474/75 and is independent of whether the device is configured as an NT or as a TE. When the $\overline{\text{RESET}}$ pin is held low, a hardware reset is applied to the MC145474/75. A hardware reset places and holds the MC145474/75 in the deactivated state and forces the NT or TE configured device to transmit INFO 0. Thus, the TxP/TxN driver pair is held in high-impedance state when this pin is held low.

A hardware reset forces the SCP Tx and the $\overline{\text{IRQ}}$ output pins to the high-impedance state, forces the DGRANT/FSYNC digital output pin low, and causes the IDL SYNC and IDL CLK digital output pins in TE configured devices to go high-impedance. A hardware reset also causes all internal state machines to return to their initial states and forces all nibble and byte registers in the SCP to their default value.

Note that BR4 and BR5 are unaffected by a hardware reset. These registers must have ‘00’ written to them in order to clear them. The $\overline{\text{RESET}}$ pin should be held high for normal operation. Upon application of power to the part, the MC145474/75 should be reset. This can be accomplished by holding the $\overline{\text{RESET}}$ pin low or by connecting an optional ‘‘RC’’ power on reset circuit to the $\overline{\text{RESET}}$ pin. The $\overline{\text{RESET}}$ pin is connected to an internal Schmitt trigger. The output of this Schmitt trigger is then connected to the internal reset of the device.

6.27 ADDITIONAL NOTES

6.27.1 TTL Level Inputs

The MC145474/75 S/T transceiver can be programmed to accept TTL level inputs on all digital input pins instead of the default CMOS levels. This mode is entered by setting BR13(6) in the SCP to a '1'.

6.27.2 SCP HIDOM

The MC145474/75 S/T transceiver has the capability of forcing all outputs (both analog and digital) to the high-impedance state. This feature, known as the ''serial control port high-impedance digital output mode'' is provided to allow ''in circuit'' testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145474/75.

The SCP HIDOM mode is entered by holding $\overline{\text{SCP EN}}$ low for a minimum of 33 consecutive rising edges of the SCP CLK while SCP Rx is high. If $\overline{\text{SCP EN}}$ goes high or if SCP Rx goes low the device will exit the SCP HIDOM mode and return to normal operation.

SECTION 7
NIBBLE MAP DEFINITION

7.1 INTRODUCTION

There are eight nibble registers (NR0 through NR7) in the MC145474/75. Control and status information reside in these nibble registers. These nibble registers are accessed via the SCP. For a detailed description of access procedures refer to Section 5. The nomenclature used in this data sheet is such that NR2(3) refers to nibble register 2, bit 3.

7.2 NIBBLE REGISTER 0

This register is a read/write register and can be reset by a hardware reset. A per bit description of nibble register 0, ‘‘NR0’’ is as follows.

7.2.1 NR0(3) — Software Reset

When NR0(3) is ‘0’, the MC145474/75 functions normally. When this bit is set to ‘1’, a software reset is applied to the internal circuits of the S/T transceiver. The effect of the software reset is the equivalent of holding the external reset input low (hardware reset), except that NR0(3:0) is not reset. Thus, when this bit is set, all internal registers (except NR0) are returned to their initial state. Note that BR4 and BR5 are exceptions to this, a reset has no effect on these registers. Although application of either a hardware or software reset has the effect of re-initializing all the internal registers, it does not prevent access to the SCP. Note that NR0(3) is a read/write bit.

7.2.2 NR0(2) — Transmit Power Down

When NR0(2) is ‘0’, the S/T transceiver functions normally. When NR0(2) is set to ‘1’, the S/T transceiver enters a power conservation mode. In this mode the transmit section of the transceiver is held in the INFO 0 state and IDL Tx is held in the ‘‘idle one’’ condition. Note that if NR0(2) = ‘1’, BR13(1) = ‘1’ and the S/T transceiver is in the TE mode then IDL Tx presents demodulated data. See Section 8.15.7 for a complete description of BR13(1). When NR0(2) = ‘1’, the receive circuitry of the transceiver is still functional, allowing an interrupt to be generated in the event of a change in state of the received signal. Note that NR0(2) is a read/write bit. This bit has no effect on the operation of the SCP.

7.2.3 NR0(1) — Absolute Minimum Power

When this bit is ‘0’, the MC145474/75 functions normally. When this bit is set to ‘1’, the chip enters a power conservation mode. In this mode a software reset is applied to the chip, all circuits are initialized, all nonessential clocking of the device is blocked and the nonessential bias to the analog functions of the transceiver is removed such that the device consumes the absolute minimum amount of power. The transmit section of the chip is held in the INFO 0 state and IDL Tx is held in the ‘‘idle one’’ condition. Note that NR0(1) is a read/write bit. This bit has no effect on the operation of the SCP.

7.2.4 NR0(0) — Return to Normal

When this bit is ‘0’, the MC145474/75 functions normally. When this bit is ‘1’, the following bits are reset:

BR11(0)	98 kHz test tone
BR11(1)	External analog loopback
BR6(7:0)	

Note that NR0(0) is a read/write bit.

7.3 NIBBLE REGISTER 1

This register is a read only register and can be reset by application of either a hardware or software reset. A per bit description of nibble register 1, ‘‘NR1’’ is as follows.

7.3.1 NR1(3) — Activation Indication (AI)

This bit is set by the MC145474/75 when the loop is fully activated. Thus if the chip is configured as an NT, this bit is set when it is transmitting INFO 4 and receiving INFO 3. Conversely, if the chip is configured as a TE, this bit is set when it is transmitting INFO 3 and receiving INFO 4. Note that NR1(3) is a read only bit.

7.3.2 NR1(2) — Error Indication (EI)

NR1(2) is set by the MC145474/75 S/T transceiver to indicate an error condition has been detected by the activation state machine of the transceiver, as outlined in CCITT I.430 and ANSI T1.605. The low to high level transition of the EI bit corresponds to the EI1 error indication reporting, while the high to low level transition of the EI bit corresponds to the EI2 error indication reporting recovery. Note that NR1(2) is a read only bit.

7.3.3 NR1(1) — TE: Multiframing Detection (MD) NT: Not Applicable

In the TE mode of operation this bit is set by the MC145474/75 S/T transceiver whenever it detects multiframing from the NT. This bit will be set low if multiframing synchronization is lost and will return high when synchronization is re-acquired. This bit applies only to TE configured devices. Note that NR1(1) is a read only bit.

7.3.4 NR1(0) — Frame Sync (FS)

NR1(0) is set high by the MC145474/75 S/T transceiver when frame synchronization is achieved. NR1(0) is reset by the MC145474/75 whenever frame synchronization is lost. Note that NR1(0) is a read only bit.

7.4 NIBBLE REGISTER 2

This register is a read/write register and can be cleared by application of either a hardware or software reset. A per bit description of nibble register 2, ‘‘NR2’’ is as follows.

7.4.1 NR2(3) — Activate Request (AR)

When NR2(3) is set to '1' an activate request input is passed to the activate state machine within the MC145474/75 S/T transceiver as outlined in CCITT I.430 and ANSI T1.605. If the transceiver is in the idle state (i.e., transmitting and receiving INFO 0) and is configured as an NT, then AR causes INFO 2 to be sent out on the transmit side of the S/T interface. Alternatively, if the chip is configured as a TE and is in the idle state, then writing a '1' to NR2(3) causes INFO 1 to be sent out. Note that this bit will be returned low by the MC145474/75 S/T transceiver after its active transition (low to high) has been recognized by the activation/deactivation state machine of the transceiver. This action indicates that the requested action has been recognized. Note that NR2(3) is a read/write bit.

7.4.2 NR2(2) — NT: Deactivate Request (DR)
TE: Not Applicable

When NR2(2) is set to '1' a deactivate request input is passed to the activation state machine within the MC145474/75 S/T transceiver, as outlined in CCITT I.430 and ANSI T1.605. The deactivate request input is used to initiate deactivation of the transmission loop. Note that this bit will be returned low by the MC145474/75 S/T transceiver after its active transition (low to high) has been recognized by the activation/deactivation state machine of the transceiver. This action indicates that the requested action has been recognized, and deactivation is proceeding. Note that NR2(2) is a read/write bit.

7.4.3 NR2(1) — Activation Timer Expired Input
NT: Timer #1
TE: Timer #3

When NR2(1) is set to '1', an activation timer expired input is passed to the activation state machine of the MC145474/75 S/T transceiver. If the transceiver is configured as an NT, this bit corresponds to the timer #1 expire input. If the transceiver is configured as a TE, this bit corresponds to the timer #3 expire input. These timers correspond to the activation timers outlined in CCITT I.430 and ANSI T1.605. The timer expire input informs the activation/deactivation state machine that sufficient time has elapsed since the request to activate the loop and that attempts to do so should be abandoned. This bit is normally set by the controlling device and then cleared prior to any further attempts to activate the loop. This bit can be reset by hardware or a software reset. Note that NR2(1) is a read/write bit.

7.4.4 NR2(0) — TE: Class
NT: Not Applicable

When the MC145474/75 is configured as a TE this bit sets the class for D channel operation. When this bit is '0' the chip is set for class 1 operation. Alternatively, when this bit is '1' the chip is configured for class 2 operation. Class 1 and class 2 operations are as per CCITT I.430 and ANSI T1.605 (i.e., class 1 is the higher class, used for signalling information and class 2 is the lower class). The class can also be chosen externally when using the MC145475 by means of the CLASS/ECHO IN pin. In this case the class is chosen by the logical 'OR' of the external pin and NR2(0). NR2(0) can be reset by a hardware or a software reset. This bit has no function when the chip is configured as an NT. Refer to Section 9 for a detailed description of the D channel. Note that NR2(0) is a read/write bit.

7.5 NIBBLE REGISTER 3

This register is a read/write register and can be reset by application of either a hardware or software reset. A per bit description of nibble register 3, ‘‘NR3’’ is as follows.

7.5.1 NR3(3) — Change in Rx Info State IRQ #3

The interrupt request condition IRQ #3 is generated whenever a change occurs in the received information state of the transceiver. In the NT mode this corresponds to a change in the receiving INFO 0, INFO 1, INFO 3, or INFO X state. Alternatively, in the TE mode this corresponds to a change in the receiving INFO 0, INFO 2, INFO 4, or INFO X state. Thus when a change occurs in one of these states the MC145474/75 internally sets this bit. An external interrupt will occur if Enable IRQ #3 (NR4(3)) is set. IRQ #3 can be cleared by writing a ‘0’ to NR3(3). This bit is reset by a software reset or a hardware reset.

Note that the transmission states for the NT (INFO 0, INFO 2, and INFO 4) and for the TE (INFO 0, INFO 1, INFO 3) are as defined in Section 3. INFO X is defined as any transmission state other than those states. An example of such a state would be when the MC145474/75 is programmed to transmit a 96 kHz test tone (BR11(0) = ‘1’). Note that NR3(3) is a read/write bit.

7.5.2 NR3(2) — Multiframe Reception IRQ #2

This bit is for multiframe detection indication. Multiframing is initiated by the NT by setting BR7(5). A multiframe is 20 basic frames or 5 ms in duration. If this interrupt is enabled by setting NR4(2) and if multiframing is in progress, then an interrupt will be generated on multiframe boundaries, i.e., every 5 ms. Alternatively an ‘‘NT configured’’ MC145474/75 can be programmed to generate an interrupt only in the event of a new Q channel nibble having been received. Similarly a ‘‘TE configured’’ MC145474/75 can be programmed to generate an interrupt only in the event of a new SC1 subchannel having been received. Refer to Section 10 for a detailed description of these features.

A mutiframing interrupt is cleared by reading BR3. Reading BR3 will clear the interrupt in both the NT and TE modes of operation, regardless of whether the MC145474/75 is configured to generate an interrupt in the event of a new nibble or every multiframe. Note that NR3(2) is a read only bit.

7.5.3 NR3(1)

7.5.3.1 TE: D CHANNEL COLLISION IRQ #1. In the TE mode NR3(1) is an interrupt bit used to indicate to external devices that a collision has occurred on the D channel. A D-channel collision is considered to have occurred when the TE is transmitting on the D channel (both DREQUEST and DGRANT being high) and the received E echo bit from the NT does not match the previously modulated D bit. The interrupt condition is cleared by writing a ‘0’ to NR3(1). Note that this bit is maskable by means of NR4(1). Note that NR3(1) is a read/write bit.

7.5.3.2 NT: FECV DETECTION IRQ #6. In the NT mode of operation NR3(1) is an interrupt bit used to indicate to external devices that a Far-End Code Violation (FECV) has occured. An FECV occurs when a previous multiframe incoming from the TE(s) contains one or more illegal S/T line code violations. To an NT device which implements the maintenance procedures as specified in ANSI T1.605 this interrupt signals that an FECV message should be sent in the SC1 multiframing subchannel. The interrupt condition is cleared by writing a ‘0’ to NR3(1). Note that this bit is maskable by means of NR4(1). Note that NR3(1) is a read/write bit.

7.5.4 NR3(0) IRQ #0

This interrupt is unassigned and is available for future use.

7.6 NIBBLE REGISTER 4

This register is a read/write register and can be reset by application of either a hardware or software reset. A per bit description of nibble register 4, ‘‘NR4’’ is as follows.

7.6.1 NR4(3) — Enable IRQ #3

NR4(3) is an interrupt mask bit for IRQ #3. When this bit is set high and IRQ #3 is pending (i.e., NR3(3) having been internally set to a one) an interrupt is given to an external device by holding the $\overline{IRQ}$ pin low. The $\overline{IRQ}$ pin will be held low until the interrupt condition is cleared by writing a ‘0’ to NR3(3). When the interrupt mask bit NR4(3) is a ‘0’, NR3(3) cannot cause an interrupt to the external device. This bit can be reset by either a software or hardware reset. Note that NR4(3) is a read/write bit.

7.6.2 NR4(2) — Enable IRQ #2

NR4(2) is an interrupt mask bit for IRQ #2. When this bit is set high and IRQ #2 is pending (i.e., NR3(2) having been internally set to a one) an interrupt is given to an external device by holding the $\overline{IRQ}$ pin low. The $\overline{IRQ}$ pin will be held low until the interrupt condition is cleared by reading BR3. When the interrupt mask bit (NR4(2)) is a ‘0’, NR3(2) cannot cause an interrupt to the external device. This bit can be reset by either a software or a hardware reset. Note that NR4(2) is a read/write bit.

7.6.3 NR4(1)

7.6.3.1 TE: ENABLE IRQ #1. NR4(1) is an interrupt mask bit for IRQ #1. When this bit is set high and IRQ #1 is pending (i.e., NR3(1) having been internally set to a ‘1’) an interrupt is given to an external device by holding the $\overline{IRQ}$ pin low. The $\overline{IRQ}$ pin will be held low until the interrupt condition is cleared by writing a ‘0’ to NR3(1). When the interrupt mask bit NR4(1) is a ‘0’, NR3(1) cannot cause an interrupt to the external device. This bit can be reset by either a software or a hardware reset. Note that NR4(1) is a read/write bit.

7.6.3.2 NT: ENABLE IRQ #6. NR4(1) is an interrupt mask bit for IRQ #6. When this bit is set high and IRQ #6 is pending (i.e., NR3(1) having been internally set to a ‘1’) an interrupt is given to an external device by holding the $\overline{IRQ}$ pin low. The $\overline{IRQ}$ pin will be held low until the interrupt condition is cleared by writing a ‘0’ to NR3(1). When the interrupt mask bit NR4(1) is a ‘0’, NR3(1) cannot cause an interrupt to the external device. This bit can be reset by either a software or a hardware reset. Note that NR4(1) is a read/write bit.

7.7 NIBBLE REGISTER 5

This register is a read/write register and can be reset by application of either a hardware or software reset. A per bit description of nibble register 5, ‘‘NR5’’ is as follows.

7.7.1 NR5(3)

7.7.1.1 NT: IDLE B1 CHANNEL. In the NT mode NR5(3) functions as a B1 channel idle bit. When NR5(3) is zero the MC145474/75 functions normally where data received in the B1 channel time

slot via the IDL is modulated onto the S/T interface in the B1 channel timeslot. When NR5(3) is '1', data input on the IDL Rx pin in the B1 channel timeslot is ignored, and the idle ones condition exists on the B1 channel timeslot on the S/T interface. Note that the default condition (i.e., power-up or after a reset) for NR5(3) is zero, thereby allowing the data received via the IDL interface to be modulated onto the transmission loop. Note that NR5(3) is a read/write bit in the NT mode.

7.7.1.2 TE: ENABLE B1 CHANNEL. In the TE mode of operation NR5(3) functions as a B1 channel enable bit. In the TE mode B1 channel data is forced to the ''idle ones'' condition on the S/T transmission loop when NR5(3) is zero. When NR5(3) is one (ENABLED) B1 channel data input via the IDL interface is modulated and transmitted onto the S/T transmission loop in the B1 channel timeslot. The default condition (i.e., upon power up or after reset) for TE mode devices forces the B1 channel bits to the ''idle ones'' condition. This is to avoid B channel interference until the B channels are assigned by the network. This function may be used in multidrop configurations or in applications where the output B channel transmission must be held in the ''idle ones'' condition. Note that NR5(3) is a read/write bit in the TE mode.

7.7.2 NR5(2)

7.7.2.1 NT: IDLE B2 CHANNEL. In the NT mode NR5(2) functions as a B2 channel idle bit. When NR5(2) is zero the MC145474/75 functions normally, where data received in the B2 channel timeslot via the IDL is modulated onto the S/T transmission loop in the B2 channel timeslot. When NR5(2) is one, data input on the IDL Rx pin in the B2 channel timeslot is ignored, and the ''idle ones'' condition exists on the B2 channel timeslot on the S/T transmission loop. Note that the default condition (i.e., after power-up or after a reset) for NR5(2) is zero, thereby allowing the data received via the IDL interface to be modulated onto the transmission loop. Note that NR5(2) is a read/write bit in the NT mode.

7.7.2.2 TE: ENABLE B2 CHANNEL. In the TE mode of operation NR5(2) functions as a B2 channel enable bit. In the TE mode B2 channel data is forced to the ''idle ones'' condition on the S/T transmission loop when NR5(2) is zero. When NR5(2) is '1' (ENABLED) B2 channel data input via the IDL interface is modulated and transmitted onto the S/T transmission loop in the B2 channel timeslot. The default condition (i.e., upon power-up or after reset) for TE mode devices forces the B2 channel bits to the ''idle ones'' condition. This is to avoid B channel interference until the B channels are assigned by the network. This function may be used in multidrop configurations or in applications where the output B channel transmission must be held in the ''idle ones'' condition. Note that NR5(2) is a read/write bit in the TE mode.

7.7.3 NR5(1) — Invert B1 Channel

When NR5(1) is zero the B1 channel data received via the IDL interface is transmitted normally on the transmission loop. When NR5(1) is set to '1' the B1 channel data received via the IDL interface is inverted before entering the modulator portion of the MC145474/75 S/T transceiver, prior to transmission on the S/T loop in the B1 timeslot. The selected B1 channel data received via the transmission loop is also inverted before being output on the IDL Tx pin when this function is invoked. This feature is useful in applications where it is required to use inverted data. Note that NR5(1) is a read/write bit.

7.7.4 NR5(0) — Invert B2 Channel

When NR5(0) is zero the B2 channel data received via the IDL interface is transmitted normally on the transmission loop. When NR5(0) is set the B2 channel data received via the IDL interface is

inverted before entering the modulator portion of the MC145474/75 S/T transceiver prior to transmission on the S/T loop in the B2 timeslot. The selected B2 channel data received via the transmission loop is also inverted before being output on the IDL Tx pin when this function is invoked. This feature is useful in applications where it is required to use inverted data. Note that NR5(0) is a read/write bit.

7.8 NIBBLE REGISTER 6

This register is a read/write register and can be reset by application of either a hardware or software reset. A per bit description of nibble register 6, ‘‘NR6’’ is as follows.

7.8.1 NR6(3) — 2B + D IDL Non-Transparent Loopback

When NR6(3) is zero the MC145474/75 S/T transceiver functions normally. When NR6(3) is set to one the B1, B2 and D channel data input on the IDL Rx input pin are buffered and returned to the IDL Tx output pin on the next IDL cycle. The output B1, B2, and D channel data is changed to the all ones idle state before entering the modulator portion of the transceiver and being transmitted onto the S/T loop (i.e., the loopback is non-transparent). Note that NR6(3) is a read/write bit.

7.8.2 NR6(2) — Activate IDL M Channel Input

When NR6(2) is zero the IDL M channel bits received via the IDL interface are ignored and are not transferred to the IDL M channel FIFO registers (byte register 0) regardless of the state of the IDL M channel hunt on zero (HOZ) bit (BR8(5)). When NR6(2) is set the IDL M channel bits received via the IDL interface are allowed to flow into the IDL M channel FIFO buffer registers. Note that further qualification of the input of IDL M channel data may be achieved by using the IDL M channel HOZ bit (BR8(5)). Note that NR6(2) is a read/write bit. Refer to Section 12 for a detailed description of the IDL FIFOs.

7.8.3 NR6(1) — Activate IDL A Channel Input

When NR6(1) is zero the IDL A channel bits received via the IDL interface are ignored and are not transferred to the IDL A channel FIFO registers (byte register 1) regardless of the state of the IDL A channel HOZ bit (BR8(4)). When NR6(1) is set the IDL A channel bits received via the IDL interface are allowed to flow into the IDL A channel FIFO buffer registers. Note that further qualification of the input of IDL A channel data may be achieved by using the IDL A channel HOZ bit (BR8(4)). Note that NR6(1) is a read/write bit. Refer to Section 12 for a detailed description of the IDL FIFOs.

7.8.4 NR6(0) — Exchange B1 and B2 at IDL

When NR6(0) is zero the timeslot assigned positions of the B1 and B2 channel data input and output via the IDL interface functions normally. When NR6(0) is set to one the timeslot positions of the B1 and B2 channels are reversed, i.e., data entering the device on IDL Rx in the B1 timeslot is modulated onto the B2 timeslot on the S/T loop. Data demodulated from the B2 timeslot from the S/T loop is output on IDL Tx in the B1 timeslot. The situation is analogous for B2 data entering the device on IDL Rx. This feature is useful in applications where a particular device (such as a codec/filter) is hard wired to a particular IDL timeslot and needs to gain access to the opposite B

channel timeslot. NR6(0) has no effect during a 2B + D IDL loopback. Note that NR6(0) is a read/write bit.

Tables 7-1 and 7-2 show an SCP nibble map for NT and TE operations, respectively.

Table 7-1. SCP Nibble Map for NT Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Activation Indication (AI)	Error Indication (EI)		Frame Sync (FS)
NR2	Activation Request (AR)	Deactivate Request (DR)	Activation Timer #1 Expire	
NR3	IRQ #3 Change in Rx INFO	IRQ #2 Multiframe Reception	IRQ #6 FECV Detection	
NR4	IRQ #3 Enable	IRQ #2 Enable	IRQ #6 Enable	
NR5	Idle B1 Channel on S/T Loop	Idle B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B + D IDL Non-Tranparent Loopback	Activate IDL M FIFO	Activate IDL A FIFO	Exchange B1 & B2 at IDL

Table 7-2. SCP Nibble Map for TE Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Activation Indication (AI)	Error Indication (EI)	Multiframing Detect	Frame Sync (FS)
NR2	Activation Request (AR)		Activation Timer #3 Expire	Class
NR3	IRQ #3 Change in Rx INFO	IRQ #2 Multiframe Reception	IRQ #1 D Channel Collision	
NR4	IRQ #3 Enable	IRQ #2 Enable	IRQ #1 Enable	
NR5	Enable B1 Channel on S/T Loop	Enable B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B + D IDL Non-Tranparent Loopback	Activate IDL M FIFO	Activate IDL A FIFO	Exchange B1 & B2 at IDL

SECTION 8
BYTE MAP DESCRIPTION

8.1 INTRODUCTION

There are sixteen byte registers (BR0 through BR15) in the MC145474/75. Control, status, and maintenance information reside in these byte registers. These byte registers are accessed via the SCP. For a detailed description of access procedures refer to Section 5. The nomenclature used in this data sheet is such that BR2(3) refers to byte register 2, bit 3.

8.2 BYTE REGISTER 0

BR0(7:0) is for use with the IDL M channel FIFOs. BR0 is a read only/write only register (data read from BR0 is independent of data written to BR0). When reading BR0 it appears as the top level of a 4-byte deep input FIFO register file for input IDL M channel data received via the IDL interface. This input FIFO is reset to the all zero state by application of either a hardware or software reset. When writing to BR0 it appears as the top level of a 4-byte deep output FIFO register file for output IDL M channel data. This data is output via the IDL interface in the IDL M channel timeslot (refer to Section 4 for a detailed description of the IDL). The output FIFO is reset to the all ones state by application of either a hardware or software reset. Writing to the output IDL FIFO when it is full will override the byte residing in the top of the FIFO.

Reading BR0 clears IRQ #5 (caused by the IDL M channel FIFO top full condition). After reading BR0 the next byte of IDL M channel data is allowed to ‘‘pop’’ to the top of the input IDL M channel FIFO, if it is available. BR8(7) is set to ‘1’ by the MC145474/75 when the output IDL M channel FIFO is less than or equal to the half full state (this corresponds to there being either 0, 1, or 2 bytes in the FIFO). If the output IDL M channel FIFO is allowed to empty, the last byte written to the IDL M channel FIFO will be repeated until new information is written to the output IDL M channel FIFO. BR0(7) is the MSB of both the input and output FIFOs. BR0(0) is the LSB of both the input and output FIFOs. Refer to Section 12 for a detailed description of the IDL FIFO operation.

8.3 BYTE REGISTER 1

BR1(7:0) is for use with the IDL A channel FIFOs. BR1 is a read only/write only register (data read from BR1 is independent of data written to BR1). When reading BR1 it appears as the top level of a 4-byte deep input FIFO register file for input IDL A channel data received via the IDL interface. This input FIFO is reset to the all zero state by application of either a hardware or software reset. When writing to BR1 it appears as the top level of a 4-byte deep output FIFO register file for output IDL A channel data. This data is output via the IDL interface in the IDL A channel timeslot (refer to Section 4 for a detailed description of the IDL). This output FIFO is reset to the all ones state by application of either a hardware or software reset. Writing to the output IDL FIFO when it is full will override the byte residing in the top of the FIFO.

Reading BR1 clears IRQ #4 (caused by the IDL A channel FIFO top full condition). After reading BR1 the next byte of IDL A channel data is allowed to ‘‘pop’’ to the top of the input IDL A channel

FIFO, if it is available. BR8(6) is set to '1' by the MC145474/75 when the output IDL A channel FIFO is less than or equal to the half full state (this corresponds to there being either 0, 1, or 2 bytes in the FIFO). If the output IDL A channel FIFO is allowed to empty, the last byte written to the IDL A channel FIFO will be repeated until new information is written to the output IDL A channel FIFO. BR1(7) is the MSB of both the input and output FIFOs. BR1(0) is the LSB of both the input and output FIFOs. Refer to Section 12 for a detailed description of the IDL FIFO operation.

8.4 BYTE REGISTER 2

8.4.1 BR2(7:4)

8.4.1.1 NT: SUBCHANNEL 1 (SC1) TO S/T LOOP. BR2(7:4) is used for multiframing. In the NT mode of operation these four bits correspond to subchannel 1 for transmission to the TE/TEs. Multiframing is initiated by the NT by setting BR7(5). When multiframing is enabled, the NT will transmit the bits in BR2(7:4) as subchannel 1, in accordance with CCITT I.430 and ANSI T1.605. BR2(7:4) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe) and its contents are interpreted as subchannel 1. If multiframing is enabled and the contents of BR2(7:4) have not been updated, then the subchannel is re-transmitted as is. BR2(7:4) can be updated any time between the 5 ms interrupts. BR2(7:4) are read/write bits. Application of either a software or hardware reset, resets these bits to all zeros. Note that BR2(7) is the MSB of SC1 and BR2(4) is the LSB. Refer to Section 10 for a more detailed description of this feature.

8.4.1.2 TE: Q NIBBLE TO S/T LOOP. BR2(7:4) is used for multiframing. In the TE mode of operation these four bits correspond to the Q channel data for transmission to the NT. When multiframing is enabled, the TE will transmit the bits in BR2(7:4) as Q channel data in accordance with CCITT I.430 and ANSI T1.605. BR2(7:4) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe) and its contents are interpreted as Q channel data. If multiframing is enabled and the contents of BR2(7:4) have not been updated, then the Q channel is re-transmitted as is. BR2(7:4) can be updated any time between the 5 ms interrupts. BR2(7:4) are read/write bits. Application of either a software or hardware reset sets these bits to all ones. Note that BR2(7) is the MSB of the Q channel and BR2(4) is the LSB. Refer to Section 10 for a more detailed description of this feature.

8.5 BYTE REGISTER 3

8.5.1 BR3(7:4)

8.5.1.1 NT: Q NIBBLE FROM S/T LOOP. BR3(7:4) are used in the multiframing mode of operation. When the device is configured as an NT and multiframing has been enabled, these bits correspond to the received Q channel nibble from the TE/TEs. These bits are updated once every multiframe. The NT configured device can give an interrupt once every multiframe (see BR3(2) and NR4(2)) or just every time a new Q channel nibble is received. BR3(7:4) are read only bits. Application of either a hardware or software reset will set these bits to the all ones state. Note that BR3(7) is the MSB of the received Q channel nibble and BR3(4) is the LSB. Refer to Section 10 for a more detailed description of this feature. Reading BR3 clears the multiframe interrupt.

8.5.1.2 TE: SC1 FROM S/T LOOP. BR3(7:4) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 1 nibble from the NT. These bits are updated once every multiframe. The TE configured device can give an interrupt once every multiframe or just every time a new subchannel nibble (SC1) is received (see BR3(2) and NR4(2)). BR3(7:4) are read only bits. Application of either a hardware or software reset will reset these bits to the all zeros state. Note that BR3(7) is the MSB of the received SC1 subchannel nibble and BR3(4) is the LSB. Refer to Section 10 for a more detailed description of this feature.

8.5.2 BR3(3) — NT: Q Bit Quality Indicate
TE: Not Applicable

In the NT mode this bit corresponds to the Q bit quality indication. When multiframing has been initiated by the NT, the TE/TEs will respond by sending Q data once every five frames. This Q data will be transmitted in the Fa bit position. During the other four frames (i.e., when the TE/TEs are not transmitting Q data) the Fa bit should be a zero. BR3(3) being high indicates that the Fa bits in the frames where multiframing data was not being transmitted were indeed zeros. This bit is a read only bit and is reset to '0' by application of either a hardware or software reset.

8.5.3 BR3(2)

8.5.3.1 NT: INTERRUPT EVERY MULTIFRAME. Programming of BR3(2) dictates whether an interrupt will be given every multiframe (assuming multiframing has been enabled and IRQ #2 enable (NR4(2)) has been set) or only on the receipt of a new Q channel nibble from the TE/TEs. When BR3(2) is '1', an interrupt is given every multiframe. When BR3(2) is '0', an interrupt is given only on the receipt of a new Q channel nibble. Refer to Section 10 for a more detailed description. BR3(2) is a read/write bit and is reset to '0' by application of either a hardware or software reset.

8.5.3.2 TE: INTERRUPT EVERY MULTIFRAME. Programming of BR3(2) dictates whether an interrupt will be given every multiframe (assuming multiframing has been enabled and IRQ #2 enable (NR4(2)) has been set) or only on the receipt of a new SC1 subchannel nibble from the NT. When BR3(2) is '1', an interrupt is given every multiframe. When BR3(2) is '0', an interrupt is given only on the receipt of a new SC1 subchannel nibble. Refer to Section 10 for a more detailed description. BR3(2) is a read/write bit and is reset to '0' by application of either a hardware or software reset.

8.6 BYTE REGISTER 4 — FRAMING VIOLATION COUNTER

Recommendation CCITT I.430 and ANSI T1.605 specifications state that there must be two AMI violations in every S/T frame. The F bit is the first violation and the succeeding violation must occur within 13 or 14 bauds, depending on the configuration of the transceiver as either an NT or TE. BR4(7:0) is the output of an 8-bit binary counter. This counter counts the number of frames which do not contain the correct number of AMI violations. Note that in multiframing it is possible to have a frame which does not contain the correct number of violations (Fa = 1, B1 = 1). The MC145474/75 when in multiframe mode, will not count these frames. Thus, in essence this counter is a ''frame error'' counter, counting the number of frames which did not contain the correct number of AMI violations. BR4(7:0) will only count frames not containing the correct number of AMI violations after FSYNC has been achieved, and will cease counting whenever FSYNC is lost.

BR4(7:0) is applicable to both NT and TE modes of operation. It is a read/write register, thereby allowing the user to program the counter to a predetermined value. To initialize or reset the counter, the user must write '00' to BR4. Note that the counter upon reaching a value of ''FF'' will not roll over, i.e., it will remain at ''FF'' until the user rewrites a starting value. Note that BR4(7) is the MSB of the counter and BR4(0) is the LSB.

8.7 BYTE REGISTER 5 — BPV COUNTER

BR5(7:0) is the output of an 8-bit binary counter. This counter counts the number of unbalanced frames. A frame in which the total number of positive pulses is different from the total number of negative pulses constitutes an unbalanced frame. BR5(7:0) is applicable to both NT and TE modes of operation. It is a read/write register, thereby allowing the user to program the counter to a predetermined value. To initialize or reset the counter, the user must write '00' to BR5. Note that the counter upon reaching a value of ''FF'' will not roll over, i.e., it will remain at ''FF'' until the user rewrites a starting value. Note that BR5(7) is the MSB of the counter and BR5(0) is the LSB.

8.8 BYTE REGISTER 6

8.8.1 BR6(7) — B1 S/T Loopback Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the device functions normally. When this bit is '1' the device enters a ''B1 S/T Loopback Transparent Mode''. In this mode, data entering the device from RxP/RxN in the B1 timeslot is demodulated and remodulated back out on TxP/TxN in the B1 timeslot. The demodulated B1 data continues to present itself on IDL Tx in the B1 timeslot (hence, the term transparent). Data entering the part from IDL Rx in the B1 timeslot is ignored. This bit is reset to '0' by either a software reset, a hardware reset, or in the ''return to normal'' mode, (NR0(0) = 1).

8.8.2 BR6(6) — B1 S/T Loopback Non-Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the device functions normally. When this bit is '1' the device enters a ''B1 S/T Loopback Non-Transparent Mode''. In this mode, data entering the device from RxP/RxN in the B1 timeslot is demodulated and remodulated back out on TxP/TxN in the B1 timeslot. Data entering the part from IDL Rx in the B1 timeslot is ignored. IDL Tx ignores the demodulated B1 data, presenting in its stead the ''idle ones'' condition in the IDL Tx B1 timeslot (hence, the term non-transparent). This bit is reset to '0' by either a software reset, a hardware reset, or in the ''return to normal'' mode, (NR0(0) = 1).

8.8.3 BR6(5) — B2 S/T Loopback Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the device functions normally. When this bit is '1' the device enters a ''B2 S/T Loopback Transparent Mode''. In this mode, data entering the device from RxP/RxN in the B2 timeslot is demodulated and remodulated back out on TxP/TxN in the B2 timeslot. The demodulated B2 data continues to present itself on IDL Tx in the B2 timeslot (hence, the term transparent). Data entering the part from IDL Rx in the B2 timeslot is ignored. This bit is reset to '0' by either a software reset, a hardware reset, or in the ''return to normal'' mode, (NR0(0) = 1).

8.8.4 BR6(4) — B2 S/T Loopback Non-Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is ‘0’ the device functions normally. When this bit is ‘1’ the device enters a ‘‘B2 S/T Loopback Non-Transparent Mode’’. In this mode, data entering the device from RxP/RxN in the B2 timeslot is demodulated and remodulated back out of TxP/TxN in the B2 timeslot. Data entering the part from IDL Rx in the B2 timeslot is ignored. IDL Tx ignores the demodulated B2 data, presenting in its stead the ‘‘idle ones’’ condition in the IDL Tx B2 timeslot (hence, the term non-transparent). This bit is reset to ‘0’ by either a software reset, a hardware reset, or in the ‘‘return to normal’’ mode, (NR0(0) = 1).

8.8.5 BR6(3) — IDL B1 Loopback Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is ‘0’ the device functions normally. When this bit is ‘1’ the device enters an ‘‘IDL B1 Loopback Transparent Mode’’. In this mode, data entering the device from IDL Rx in the B1 timeslot is retransmitted back out on IDL Tx in the B1 timeslot on the subsequent IDL frame. The demodulated B1 data from RxP/RxN is ignored. Data entering the device from IDL Rx as well as being transmitted back out on IDL Tx, will also continue to be modulated onto the B1 timeslot on TxP/TxN (hence, the term transparent). This bit is reset to ‘0’ by either a software reset, a hardware reset, or in the ‘‘return to normal’’ mode, (NR0(0) = 1).

8.8.6 BR6(2) — IDL B1 Loopback Non-Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is ‘0’ the device functions normally. When this bit is ‘1’ the device enters the ‘‘IDL B1 Loopback Non-Transparent Mode’’. In this mode, data entering the device from IDL Rx in the B1 timeslot is retransmitted back out on IDL Tx in the B1 timeslot, on the subsequent IDL frame. The demodulated B1 data from RxP/RxN is ignored. The modulator core of the MC145474/75 ignores the data received from IDL Rx, modulating in its stead the ‘‘idle ones’’ condition in the B1 timeslot on TxP/TxN (hence, the term non-transparent). This bit is reset to ‘0’ by either a software reset, a hardware reset, or in the ‘‘return to normal’’ mode, (NR0(0) = 1).

8.8.7 BR6(1) — IDL B2 Loopback Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is ‘0’ the device functions normally. When this bit is ‘1’ the device enters an ‘‘IDL B2 Loopback Transparent Mode’’. In this mode, data entering the device from IDL Rx in the B2 timeslot is retransmitted back out on IDL Tx in the B2 timeslot on the subsequent IDL frame. The demodulated B2 data from RxP/RxN is ignored. Data entering the device from IDL Rx as well as being transmitted back out of IDL Tx, will also continue to be modulated onto the B2 timeslot on TxP/TxN (hence, the term transparent). This bit is reset to ‘0’ by either a software reset, a hardware reset, or in the ‘‘return to normal’’ mode, (NR0(0) = 1).

8.8.8 BR6(0) — IDL B2 Loopback Non-Transparent

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is ‘0’ the device functions normally. When this bit is ‘1’ the device enters an ‘‘IDL B2 Loopback Non-Transparent Mode’’. In this mode, data entering the device from IDL Rx in the B2 timeslot is retransmitted back out on IDL Tx in the B2 timeslot on the subsequent IDL frame. The demodulated

B2 data from RxP/RxN is ignored. The modulator core of the MC145474/75 ignores the data received from IDL Rx, modulating in its stead the ‘‘idle ones’’ condition in the B2 timeslot on TxP/TxN (hence, the term non-transparent). This bit is reset to ‘0’ by either a software reset, a hardware reset, or in the ‘‘return to normal’’ mode, (NR0(0) = 1).

8.9 BYTE REGISTER 7

8.9.1 BR7(7) — Activation Procedures Disabled

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is ‘0’ the MC145474/75 functions normally. When this bit is set to ‘1’ the transmit section of the transceiver is forced into the highest information state. Thus, if the device is operating as NT, INFO 4 will be forced out on the transmit side of the device. INFO 4 will be forced out regardless of what is being received on RxP/RxN. If the device is operating as a TE, then the transceiver will transmit INFO 3 on TxP/TxN.

Note that if activation procedures are disabled as a TE, causing INFO 3 to be transmitted, then this state may or may not be commensurate with receiving INFO 0 from the NT. In the event that INFO 0 is being received, the transmitted INFO 3 will be transmitted asynchronously. If either INFO 2 or INFO 4 are subsequently received then the TEs INFO 3 will align itself to the received signal in accordance with CCITT I.430 and ANSI T1.605. Note also that a TE will be woken up if it receives either INFO 2 or INFO 4 from the NT. However, an NT transmitting INFO 0 will not wake up to the reception of INFO 3 from the TE. For an NT to be woken up by a TE it must first receive INFO 1 from the TE and then proceed to go through the subsequent handshaking. BR7(7) is reset to ‘0’ by application of either a hardware or software reset.

8.9.2 BR7(6)

8.9.2.1 TE: D CHANNEL PROCEDURES IGNORED. When the MC145474/75 is configured as a TE this bit is used to enable/disable D channel contention procedures in accordance with CCITT I.430 and ANSI T1.605. When this bit is ‘0’ the D channel procedures are adhered to as per the DREQUEST, DGRANT, and CLASS pin descriptions. When this bit is ‘1’ the D channel procedures are ignored, allowing the data present in the D channel on IDL Rx to be modulated regardless of the status of DREQUEST and DGRANT. BR7(6) = ‘1’ causes the TE to disregard the demodulated E echo bits. The TEs D data will be modulated regardless. This bit is a read/write bit and is reset to ‘0’ by application of either a software or a hardware reset.

8.9.2.2 NT. When the MC145474/75 is configured as an NT this bit is reserved for Motorola use only and must always be reset to a ‘0’. This bit is a read/write bit and is reset to ‘0’ by application of either a software or a hardware reset.

8.9.3 BR7(5) — NT: Enable Multiframing
TE: Not Applicable

When the MC145474/75 is configured as an NT, this bit is used to enable/disable multiframing in accordance with CCITT I.430 and ANSI T1.605. When this bit is ‘0’, multiframing is disabled. In this mode, the M, Fa, and S bauds transmitted from the NT will be binary ‘0’. When this bit is ‘1’, multiframing is enabled. In this mode, the M, Fa, and S bauds will adhere to the multiframing coding rules as outlined in I.430 and ANSI T1.605. Since the TE cannot initiate multiframing, this bit has no application in this mode. This bit is a read/write bit and is reset to ‘0’ by application of either a software or a hardware reset.

8.9.4 BR7(4)

8.9.4.1 NT: INVERT E CHANNEL. When the MC145474/75 is configured as an NT, this bit is used to determine the polarity of the transmitted E echo channel from the NT to the TE. When this bit is a ‘0’, the transmitted E bit is the same as the previously demodulated D bit from the TE/TEs. When this bit is ‘1’, the transmitted E bit is the logical inverse of the previously demodulated D bit. This bit is a read/write bit and is reset to ‘0’ by application of either a software or hardware reset.

8.9.4.2 TE: MAP E BITS TO IDL. With the MC145474/75 configured as a TE and this bit a ‘0’, the TE outputs the demodulated D channel data in the D timeslot on the IDL Tx. When this bit is set to ‘1’, the TE will output the demodulated E channel in the D timeslot on IDL Tx, neglecting the demodulated D channel data. This bit is a read/write bit and is reset to ‘0’ by application of either a software or a hardware reset.

8.9.5 BR7(3)

8.9.5.1 NT: IDL MASTER MODE. With the MC145474/75 configured as an NT this bit determines whether the device operates in IDL slave or IDL master mode. When this bit is ‘0’, the NT operates in the IDL slave mode, IDL SYNC and IDL CLK being inputs to the device. When this bit is ‘1’, the NT operates in the NT IDL master mode, IDL SYNC and IDL CLK being outputs from the device. This bit is a read/write bit and is reset to ‘0’ by application of either a software or hardware reset.

8.9.5.2 TE: IDL FREE RUN. When the MC145474/75 is configured as a TE and the loop is active, the device will output IDL SYNC and IDL CLK synchronous to the inbound data from the NT. When the loop is inactive and this bit is ‘0’, the TE will not output IDL SYNC or IDL CLK. If this bit is ‘1’, the TE will output IDL SYNC and IDL CLK regardless of the status of the loop. If the loop is inactive these signals will be free-running (derived from the crystal). If the loop is active then these signals will be synchronous to the inbound data. This bit is a read/write bit and is reset to ‘0’ by application of either a software or a hardware reset.

8.9.6 BR7(2) — IDL Clock Speed (LSB)

This bit is a read/write bit and is applicable to both NT and TE modes of operation. BR7(2) in conjunction with BR13(5) determines the IDL CLK frequency when operating in the IDL master mode. BR7(2) is the LSB and BR13(5) is the MSB. The code corresponding to each IDL clock frequency is shown in Table 8-1.

Table 8-1. IDL Clock Speed Codes

BR13(5)	BR7(2)	IDL CLK	
		Rate	Duty Cycle
0	0	2.56 MHz	50%
0	1	2.048 MHz	53.3%
1	X	1.536 MHz	50%

Application of either a hardware or a software reset will reset this bit to ‘0’. Note that 1.536 MHz is not applicable in the TE mode of operation. Refer to Section 4 for a more detailed description.

8.9.7 BR7(1) — TE: LAPD Polarity Control
NT: Not Applicable

When the MC145474/75 is configured as a TE this bit performs the ‘‘LAPD Polarity Control’’ function. When this bit is ‘0’, the active state of DREQUEST and DGRANT signals is defined to be the logic one or high state. When this bit is ‘1’, the active state of these signals is defined to be the logic zero or low state. This bit is a read/write bit and is reset to ‘0’ by application of either a hardware or software reset.

8.9.8 BR7(0) — NT: Activation Timer #2 Expired
TE: Not Applicable

When the MC145474/75 is configured as an NT, this bit performs the ‘‘Activation Timer #2 Expired’’ function. When this bit is ‘0’, the NT configured S/T transceiver uses a value of 50 ms for the timer #2 value outlined in CCITT I.430 and ANSI T1.605 (i.e., the device unambiguously detects INFO 1). When this bit is ‘1’, a value of 100 ms is used for the value of timer #2. This bit is a read/write bit and is reset to ‘0’ by application of either a hardware or software reset.

8.10 BYTE REGISTER 8

8.10.1 BR8(7) — IDL M Channel FIFO ≤ 1/2 Full

This bit is a read only bit and is applicable to both NT and TE modes of operation. When the IDL M channel transmit FIFOs are less than or equal to half full (i.e., they contain 0, 1, or 2 bytes) this bit is internally set. This feature informs the user when it is appropriate to reload the FIFOs for transmission out on IDL Tx. As soon as the FIFOs have been reloaded to a capacity of greater than two bytes, this bit is internally cleared. Since a hardware or software reset resets the IDL M channel retransmit FIFOs, then it will also set this status bit to ‘1’.

8.10.2 BR8(6) — IDL A Channel FIFO ≤ 1/2 Full

This bit is a read only bit and is applicable to both NT and TE modes of operation. When the IDL A channel transmit FIFOs are less than or equal to half full (i.e., they contain 0, 1, or 2 bytes) this bit is internally set. This feature informs the user when it is appropriate to reload the FIFOs for retransmission out on IDL Tx. As soon as the FIFOs have been reloaded to a capacity of greater than two bytes, this bit is internally cleared. Since a hardware or software reset resets the IDL A channel transmit FIFOs, then it will also set this status bit to ‘1’.

8.10.3 BR8(5) — Activate IDL M Channel FIFO ‘‘Hunt on Zero’’

This bit is applicable to both NT and TE modes of operation. This bit in conjunction with the ‘‘Activate IDL M FIFO (NR6(2))’’ bit control the flow of data into the input FIFOs from IDL Rx. Setting the ‘‘HOZ’’ bit followed by the ‘‘Activate’’ bit will cause the first zero received on IDL Rx in the IDL M bit position to trigger the loading of the input FIFOs. The first zero and the subsequent seven IDL M bits from IDL Rx will form the first byte loaded into the input FIFOs. Thereafter, the FIFOs will load on 8-bit boundaries of received IDL M data. This bit is internally cleared once the first zero has been recognized on IDL Rx in the IDL M bit position. BR8(5) is a read/write bit and is reset to ‘0’ by application of either a hardware or software reset.

8.10.4 BR8(4) — Activate IDL A Channel FIFO "Hunt on Zero"

This bit is applicable to both NT and TE modes of operation. This bit in conjunction with the ''Activate IDL A FIFO (NR6(1))'' bit control the flow of data into the input FIFOs from IDL Rx. Setting the ''HOZ'' bit followed by the ''Activate'' bit will cause the first zero received on IDL Rx in the IDL A bit position to trigger the loading of the input FIFOs. The first zero and the subsequent seven IDL A bits from IDL Rx will form the first byte loaded into the input FIFOs. Thereafter, the FIFOs will load on 8-bit boundaries of received IDL A data. This bit is internally cleared once the first zero has been recognized on IDL Rx in the IDL A bit position. BR8(4) is a read/write bit and is reset to '0' by application of either a hardware or software reset.

8.10.5 BR8(3) — Enable IDL A Channel FIFO Interrupt (IRQ #4)

BR8(3) is an interrupt mask bit for IRQ #4. When this bit is set high and IRQ #4 is pending (i.e., BR8(1) having been internally set to '1') an interrupt is given to an external device by holding the $\overline{IRQ}$ pin low. The $\overline{IRQ}$ pin will be held low until the interrupt is cleared by reading the IDL A channel FIFO. When this bit is '0', BR8(1) cannot cause an interrupt to the external device. This bit is a read/write bit and is reset to '0' by application of either a hardware or software reset.

8.10.6 BR8(2) — Enable IDL M Channel FIFO Interrupt (IRQ #5)

BR8(2) is an interrupt mask bit for IRQ #5. When this bit is set high and IRQ #5 is pending (i.e., BR8(0) having been internally set to '1') an interrupt is given to an external device by holding the $\overline{IRQ}$ pin low. The $\overline{IRQ}$ pin will be held low until the interrupt is cleared by reading the IDL M channel FIFO. When this bit is '0', BR8(0) cannot cause an interrupt to the external device. This bit is a read/write bit and is reset to '0' by application of either a hardware or software reset.

8.10.7 BR8(1) — IDL M Channel FIFO Interrupt (IRQ #4)

The interrupt request condition IRQ #4 is generated whenever an IDL A channel byte is present at the top of the A channel input FIFOs. This byte will have been loaded into the IDL A channel input FIFOs from IDL Rx in the IDL A channel timeslot. IRQ #4 is cleared by reading BR1. This bit is cleared by application of either a hardware or software reset.

8.10.8 BR8(0) — IDL M Channel FIFO Interrupt (IRQ #5)

The interrupt request condition IRQ #5 is generated whenever an IDL M channel byte is present at the top of the M channel input FIFOs. This byte will have been loaded into the IDL M channel input FIFOs from IDL Rx in the IDL M channel timeslot. IRQ #5 is cleared by reading BR0. This bit is cleared by application of either a hardware or software reset.

8.11 BYTE REGISTER 9

8.11.1 BR9(7:4)

8.11.1.1 NT: SC2 TO LOOP. BR9(7:4) is used for multiframing. In the NT mode of operation, these four bits correspond to subchannel 2 for transmission to the TE/TEs. Multiframing is initiated by the NT by setting BR7(5). When multiframing is enabled, the NT will transmit the bits in BR9(7:4) as

subchannel 2, in accordance with CCITT I.430 and ANSI T1.605. BR9(7:4) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe) and its contents are interpreted as subchannel 2. If multiframing is enabled and the contents of BR9(7:4) have not been updated then the subchannel is re-transmitted as is. BR9(7:4) can be updated any time between the 5 ms interrupts. In the NT mode of operation BR9(7:4) are write only bits. These bits are reset to '0' by application of either a software or hardware reset. Note that BR9(7) is the MSB of SC2 and BR9(4) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

8.11.1.2 TE: SC2 FROM LOOP. BR9(7:4) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 2 nibble from the NT. These bits are updated once every multiframe. BR9(7:4) are read only bits and are reset to '0' by application of either a software or hardware reset. Note that BR9(7) is the MSB of SC2 and BR9(4) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

8.11.2 BR9(3:0)

8.11.2.1 NT: SC3 TO LOOP. BR9(3:0) is used for multiframing. In the NT mode of operation these four bits correspond to subchannel 3 for transmission to the TE/TEs. When multiframing is enabled, the NT will transmit the bits in BR9(3:0) as subchannel 3, in accordance with CCITT I.430 and ANSI T1.605. BR9(3:0) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe) and its contents are interpreted as subchannel 3. If multiframing is enabled and the contents of BR9(3:0) have not been updated then the subchannel is re-transmitted as is. BR9(3:0) can be updated any time between the 5 ms interrupts. In the NT mode of operation BR9(3:0) are write only bits. These bits are reset to '0' by application of either a software or hardware reset. Note that BR9(3) is the MSB of SC3 and BR9(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

8.11.2.2 TE: SC3 FROM LOOP. BR9(3:0) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 3 nibble from the NT. These bits are updated once every multiframe. BR9(3:0) are read only bits and are reset to '0' by application of either a software or hardware reset. Note that BR9(3) is the MSB of SC2 and BR9(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

8.12 BYTE REGISTER 10

8.12.1 BR10(7:4)

8.12.1.1 NT: SC4 TO LOOP. BR10(7:4) is used for multiframing. In the NT mode of operation these four bits correspond to subchannel 4 for transmission to the TE/TEs. When multiframing is enabled, the NT will transmit the bits in BR10(7:4) as subchannel 4, in accordance with CCITT I.430 and ANSI T1.605. BR10(7:4) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed to give an interrupt at the start of every multiframe) and its contents are interpreted as subchannel 4. If multiframing is enabled and the contents of BR10(7:4) have not been updated, then the subchannel is re-transmitted as is. BR10(7:4) can be updated any time between the 5 ms interrupts. In the NT mode of operation BR10(7:4) are write only bits. These bits

are reset to ‘0’ by application of either a software or hardware reset. Note that BR10(7) is the MSB of SC4 and BR10(4) is the LSB. Refer to Section 10 for a detailed description of the multiframing procedure.

8.12.1.2 TE: SC4 FROM LOOP. BR10(7:4) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 4 nibble from the NT. These bits are updated once every multiframe. BR10(7:4) are read only bits and are reset to ‘0’ by either a software or hardware reset. Note that BR10(7) is the MSB of SC4 and BR10(4) is the LSB. Refer to Section 10 for a detailed description of multiframe procedures.

8.12.2 BR10(3:0)

8.12.2.1 NT: SC5 TO LOOP. BR10(3:0) is used for multiframing. In the NT mode of operation these four bits correspond to subchannel 5 for transmission to the TE/TEs. When multiframing is enabled, the NT will transmit the bits in BR10(3:0) as subchannel 5, in accordance with CCITT I.430 and ANSI T1.605. BR10(3:0) is internally polled at the start of every multiframe (this occurs every 5 ms and the device can be programmed via NR4(2) to give an interrupt at the start of every multiframe) and its contents are interpreted as subchannel 5. If multiframing is enabled and the contents of BR10(3:0) have not been updated then the subchannel is re-transmitted as is. BR10(3:0) can be updated any time between the 5 ms interrupts. In the NT mode of operation BR10(3:0) are write only bits. These bits are reset to ‘0’ by application of either a software or hardware reset. Note that BR10(3) is the MSB of SC5 and BR10(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

8.12.2.2 TE: SC5 FROM LOOP. BR10(3:0) are used in the multiframing mode of operation. When the device is configured as a TE and multiframing has been enabled, these bits correspond to the received subchannel 5 nibble from the NT. These bits are updated once very multiframe. BR10(3:0) are read only bits and are reset to ‘0’ by either a software or hardware reset. Note that BR10(3) is the MSB of SC5 and BR10(0) is the LSB. Refer to Section 10 for a detailed description of the multiframe procedure.

8.13 BYTE REGISTER 11

8.13.1 BR11(7) — NT: Do Not React to INFO 1
TE: Not Applicable

This bit is only applicable to the NT mode of operation. When this bit is ‘0’ the part functions normally. When this bit is ‘1’ the NT will not react to INFO 1 from the TE. (Note, however, that the NT will give an interrupt indicating a change in received information state.) Only when the NT resets this bit to ‘0’ will it react to INFO 1. This feature is used in the NT in applications where it is necessary to delay activation of the S/T loop until the U link has reached its active state. This bit is a read/write bit and is reset to ‘0’ by application of either a hardware or software reset.

8.13.2 BR11(6) — NT: Do Not React to INFO 3
TE: Not Applicable

This bit is only applicable to the NT mode of operation. When this bit is ‘0’, the part functions normally. When this bit is ‘1’, the NT will not react to INFO 3 from the TE (this INFO 3 from the TE

being the response of the TE to INFO 2 from the NT). Only when the NT resets this bit to ‘0’ will it react to INFO 3. In the meantime the NT will continue to transmit INFO 2. This feature is used in the NT in applications where it is necessary to delay activation of the S/T loop until the U link has reached its active state. This bit is a read/write bit and is reset to ‘0’ by application of either a hardware or software reset.

8.13.3 BR11(5), BR11(4) — Rx INFO State B1 and B0

These bits are read/write bits and are applicable to both NT and TE modes of operation. The MC145474/75 will internally set these bits to indicate the status of the received signal, i.e., is it INFO 0, 1, 2, 3, 4, or X, where INFO X is none of the above. An example of INFO X would be when it is receiving the 96 kHz test tone. Another example of INFO X would be where the transceiver is not receiving INFO 0, but it has not yet determined whether it is INFO 1, 2, 3, or 4.

The code corresponding to the different states is shown in Table 8-2.

Table 8-2. BR11(5), BR11(4) Rx INFO State Codes

BR11(5)	BR11(4)	Receive Information State
0	0	INFO 0
0	1	INFO LOW
1	0	INFO HIGH
1	1	INFO X

Note: When configured as an NT, receiving INFO LOW corresponds to receiving INFO 1, and receiving INFO HIGH corresponds to receiving INFO 3. Conversely, when the device is operating as a TE, receiving INFO LOW corresponds to receiving INFO 2, and receiving INFO HIGH corresponds to receiving INFO 4. The device internally sets these bits and this internal write overrides any external write. These bits are reset to ‘0’ by application of either a hardware or software reset.

8.13.4 BR11(3), BR11(2) — Tx INFO State B1 and B0

These bits are read/write bits and are applicable to both NT and TE modes of operation. The MC145474/75 will internally set these bits to indicate the status of the transmitted signal, i.e., is it INFO 0, 1, 2, 3, 4, or X where INFO X is none of the above. An example of INFO X would be when it is transmitting the 96 kHz test tone. The code corresponding to the different states is shown in Table 8-3.

Table 8-3. BR11(3), BR11(2) Tx INFO State Codes

BR11(3)	BR11(2)	Transmit Information State
0	0	INFO 0
0	1	INFO LOW
1	0	INFO HIGH
1	1	INFO X

Note: When configured as an NT, transmitting INFO LOW corresponds to transmitting INFO 2, and transmitting INFO HIGH corresponds to transmitting INFO 4. Conversely, when the device is operating as a TE, transmitting INFO LOW corresponds to transmitting INFO 1, and transmitting INFO HIGH corresponds to transmitting INFO 3. The device internally sets these bits and this internal write overrides any external write. These bits are reset to '0' by application of either a hardware or software reset.

8.13.5 BR11(1) — External S/T Loopback

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the MC145474/75 functions normally. If the transmit pair is shorted to the receive pair while this bit is '1', then the device will perform an external or ''analog'' loopback. In an analog loopback the device demodulates its own transmitted data. The transceiver should have its activation procedures disabled (BR7(7) = '1') and be configured for the IDL master mode (BR7(3) = '1'). This feature is useful for test purposes. In external loopback, the B1 and B2 channels are looped back. In the NT mode the D channel is also looped back. The D channel is not looped back in the TE mode. Application of a hardware or software reset will reset this bit to '0'.

8.13.6 BR11(0) — Transmit 96 kHz Test Signal

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the MC145474/75 functions normally. When this bit is '1', the device transmits a 96 kHz square wave test tone on TxP/TxN. This test tone can be used for test purpose. This 96 kHz test tone will qualify as a ''Transmit INFO X'' state. Correspondingly, the MC145474/75 receiving the 96 kHz test tone will be in the ''Receive INFO X'' state. Application of a hardware or software reset will reset this bit to '0'.

8.14 BYTE REGISTER 12

Byte register 12 is a read/write register. It is reserved for Motorola use only.

8.15 BYTE REGISTER 13

8.15.1 BR13(7) — NT: NT1 Star Mode
TE: Not Applicable

This bit is a read/write bit and is only applicable to the NT mode of operation. When this bit is '0', the device functions normally. When this bit is '1', the device is configured for NT1 Star mode operation. Refer to Section 11 for a detailed description of this mode. This bit is reset to '0' by application of either a hardware or software reset.

8.15.2 BR13(6) — TTL Input Levels

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0', the device accepts CMOS levels on all digital input pins. When this bit is '1', the device accepts TTL levels on all digital input pins. This feature allows the device to be connected to either TTL or CMOS logic devices without any additional interfacing required. Application of either a hardware or software reset will reset this bit to '0'.

8.15.3 BR13(5) — IDL Clock Speed (MSB)

This bit is a read/write bit and is applicable to both NT and TE modes of operation BR13(5) in conjunction with BR7(2) determine the IDL CLK frequency, when operating in the IDL master mode. BR7(2) is the LSB and BR13(5) is the MSB. The code corresponding to each IDL clock frequency is as shown in the description for BR7(2). Application of either a hardware or a software reset will reset this bit to '0'. See Table 8-1.

8.15.4 BR13(4) — Mute B2 on IDL

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the device functions normally. When this bit is '1', the data transmitted on the B2 channel on IDL Tx will be forced to the ''idle ones'' condition. This feature is primarily used in the NT1 Star mode operation. Refer to Section 11 for a detailed description of this mode. Application of a hardware or software reset will reset this bit to '0'.

8.15.5 BR13(3) — Mute B1 on IDL

This bit is a read/write bit and is applicable to both NT and TE modes of operation. When this bit is '0' the device functions normally. When this bit is '1', the data transmitted on the B1 channel on IDL Tx will be forced to the ''idle ones'' condition. This feature is primarily used in the NT1 Star mode operation. Refer to Section 11 for a detailed description of this mode. Application of a hardware or software reset will reset this bit to '0'.

8.15.6 BR13(2) — NT: Force Echo Channel to Zero
TE: Not Applicable

This bit is a read/write bit and is only applicable to the NT mode of operation. When the MC145474/75 is configured as an NT and this bit is '0', the device functions normally. When this bit is '1', the NT will force the transmitted E bits to be '0'. This feature is used for test purposes when the NT wishes to communicate to the TEs on the passive bus that they should disengage from the D channel. Application of either a hardware or a software reset will reset this bit to '0'.

8.15.7 BR13(1) — TE: Force IDL Transmit
NT: Not Applicable

This bit is a read/write bit and is only applicable in the TE mode of operation. When the MC145474/75 is configured as a TE and this bit is '0', the device functions normally. When this bit is '1' data is presented on IDL Tx in the special case where the TE is synchronized to INFO 4 incoming from the NT but its transmitter is not fully active (i.e. not transmitting INFO 3). This feature is useful when the MC145474/75 is in the ''Transmit Power Down Mode'' (NR0(2) = '1') and it is desired to continue to process data from the NT. This bit has no effect when the device is fully active (transmitting INFO 3 and receiving INFO 4). When BR13(1) = '0' and the device is not fully active ''idle ones'' will be presented on IDL Tx. Application of either a hardware or a software reset will reset this bit to '0'.

8.15.8 BR13(0)

This bit is reserved.

8.16 BYTE REGISTER 14

Byte register 14 is a read/write register. It is reserved for Motorola use only.

8.17 BYTE REGISTER 15

Byte register 15 is a read/write register. It is reserved for Motorola use only.

An SCP byte map for NT operations is shown in Table 8-4. The byte map for TE operations is shown in Table 8-5.

Table 8-4. SCP Byte Map for NT Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0	M7	M6	M5	M4	M3	M2	M1	M0
BR1	A7	A6	A5	A4	A3	A2	A1	A0
BR2	SC1.1 to Loop	SC1.2 to Loop	SC1.3 to Loop	SC1.4 to Loop				
BR3	Q1 from Loop	Q2 from Loop	Q3 from Loop	Q4 from Loop	Q Bit Quality Indicate	INT Every M. Frame		
BR4	Fr. Viol. Count B7	Fr. Viol. Count B6	Fr. Viol. Count B5	Fr. Viol. Count B4	Fr. Viol. Count B3	Fr. Viol. Count B2	Fr. Viol. Count B1	Fr. Viol. Count B0
BR5	BPV Count B7	BPV Count B6	BPV Count B5	BPV Count B4	BPV Count B3	BPV Count B2	BPV Count B1	BPV Count B0
BR6	B1 S/T LB Transparent	B1 S/T LB Non-Trans.	B2 S/T LB Transparent	B2 S/T LB Non-Trans.	IDL B1 LB Transparent	IDL B1 LB Non-Trans.	IDL B2 LB Transparent	IDL B2 LB Non-Trans.
BR7	Act. Proc. Disabled	Reserved	Enable Multiframing	Invert E Channel	IDL Master Mode	IDL CLK Speed LSB		Act. Timer #2
BR8	IDL M FIFO ≤ 1/2 Full	IDL A FIFO ≤ 1/2 Full	Act. IDL M FIFO HOZ	Act. IDL A FIFO HOZ	Enable IRQ #4	Enable IRQ #5	IRQ #4 IDL A FIFO	IRQ #5 IDL M FIFO
BR9	SC2.1 to Loop	SC2.2 to Loop	SC2.3 to Loop	SC2.4 to Loop	SC3.1 to Loop	SC3.2 to Loop	SC3.3 to Loop	SC3.4 to Loop
BR10	SC4.1 to Loop	SC4.2 to Loop	SC4.3 to Loop	SC4.4 to Loop	SC5.1 to Loop	SC5.2 to Loop	SC5.3 to Loop	SC5.4 to Loop
BR11	Do Not React to INFO 1	Do Not React to INFO 3	Rx INFO State B1	Rx INFO State B0	Tx INFO State B1	Tx INFO State B0	EXT S/T Loopback	Tx 96 kHz Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	NT1 Star Mode	TTL Input Levels	IDL CLK Speed MSB	Mute B2 on IDL	Mute B1 on IDL	Force E to Zero		
BR14					Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 8-5. SCP Byte Map for TE Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0	M7	M6	M5	M4	M3	M2	M1	M0
BR1	A7	A6	A5	A4	A3	A2	A1	A0
BR2	Q1 to Loop	Q2 to Loop	Q3 to Loop	Q4 to Loop				
BR3	SC1.1 from Loop	SC1.2 from Loop	SC1.3 from Loop	SC1.4 from Loop		INT Every M Frame		
BR4	Fr. Viol. Count B7	Fr. Viol. Count B6	Fr. Viol. Count B5	Fr. Viol. Count B4	Fr. Viol. Count B3	Fr. Viol. Count B2	Fr. Viol. Count B1	Fr. Viol. Count B0
BR5	BPV Count B7	BPV Count B6	BPV Count B5	BPV Count B4	BPV Count B3	BPV Count B2	BPV Count B1	BPV Count B0
BR6	B1 S/T LB Transparent	B1 S/T LB Non-Trans.	B2 S/T LB Transparent	B2 S/T LB Non-Trans.	IDL B1 LB Transparent	IDL B1 LB Non-Trans.	IDL B2 LB Transparent	IDL B2 LB Non-Trans.
BR7	Act. Proc. Ignored	D Channel Proc. Ignored		Map E to IDL on D Channel	IDL Free Run	IDL CLK Speed LSB	LAPD Pol. Cont.	
BR8	IDL M FIFO ≤ 1/2 Full	IDL A FIFO ≤ 1/2 Full	Act. IDL M FIFO HOZ	Act. IDL A FIFO HOZ	Enable IRQ #4	Enable IRQ #5	IRQ #4 IDL A FIFO	IRQ #5 IDL M FIFO
BR9	SC2.1 from Loop	SC2.2 from Loop	SC2.3 from Loop	SC2.4 from Loop	SC3.1 from Loop	SC3.2 from Loop	SC3.3 from Loop	SC3.4 from Loop
BR10	SC4.1 from Loop	SC4.2 from Loop	SC4.3 from Loop	SC4.4 from Loop	SC5.1 from Loop	SC5.2 from Loop	SC5.3 from Loop	SC5.4 from Loop
BR11			Rx INFO State B1	Rx INFO State B0	Tx INFO State B1	Tx INFO State B0	EXT S/T Loopback	Tx 96 kHz Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13		TTL Input Levels	IDL CLK Speed MSB	Mute B2 on IDL	Mute B1 on IDL		Force IDL Transmit	
BR14					Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

SECTION 9
D CHANNEL OPERATION

9.1 INTRODUCTION

The S/T interface is designed for full duplex transmission of two 64 kbps B channels and one 16 kbps D channel, between one NT device and one or more TEs. The TEs gain access to the B channels by sending layer 2 frames to the network over the D channel. CCITT I.430 and ANSI T1.605 specify a D channel access algorithm for TEs to gain access to the D channel. The MC145474/75 S/T transceiver is fully compliant with the D channel access algorithm as defined in CCITT I.430 and ANSI T1.605. The SCP bits and pins directly pertaining to D channel operation are shown in Tables 9-1 and 9-2.

Table 9-1. D Channel SCP Bit Description

MC145474/75 NT Mode		MC145474/75 TE Mode	
SCP Bit	**Description**	**SCP Bit**	**Description**
BR7(4)	Invert the Echo Channel	NR2(0)	Class
BR13(2)	Force the Echo Channel to '0'	NR3(1)	Interrupt on D Channel Collision
BR13(7)	NT1 Star Mode	NR4(1)	Interrupt Enable for NR3(1)
		BR7(1)	LAPD Polarity Control
		BR7(4)	Map Echo Bits to D Timeslots on IDL Tx
		BR7(6)	D Channel Procedures Ignored

Table 9-2. D-Channel Operation Pin Description

MC145474	MC145475
Pin 5 DGRANT	Pin 5 DGRANT
Pin 7 DREQUEST	Pin 6 ANDIN
	Pin 8 ANDOUT
	Pin 9 DREQUEST
	Pin 10 CLASS/ECHO IN

D channel data is clocked into the MC145474/75 via IDL Rx on the falling edges of IDL CLK. Data is clocked out onto IDL Tx on the rising edges of IDL CLK. This is in accordance with the IDL specification as outlined in Section 4. For a detailed description of the above pins, refer to Section 6. For a detailed description of the above SCP bits, refer to Sections 7 and 8.

9.2 GAINING ACCESS TO THE D CHANNEL IN THE TE MODE

The pins DREQUEST and DGRANT are used in the TE mode of operation to request and grant access to the D channel. An external device wishing to send a layer 2 frame should bring

DREQUEST high, and maintain it high for the duration of the layer 2 frame. DGRANT is an output signal used to indicate to an external device that the D channel is clear. Note that the DGRANT signal actually goes high one received E echo bit prior to the programmed priority class selection. DGRANT goes high at a count of (n – 1) to accommodate the delay between the input of D channel data via the IDL interface and the line transmission of those bits towards the NT. If at the time of the IDL SYNC pulse falling edge, the DGRANT and the DREQUEST signals are both detected high, the TE mode transceiver will begin FIFO buffering of the input D channel bits from the IDL interface. This FIFO is four bits deep. Note that DGRANT goes high on the boundaries of the demodulated E bits. In order for the contention algorithm to work on the D channel, HDLC data must be used. The MC145474/75 modulates the D channel data onto the S/T bus in the form that it is received from the IDL bus. Thus, the data must be presented to it in HDLC format. Note that one of the applications of the MC145488 DDLC is for use with the MC145474/75 in the terminal mode. The MC145488 will perform the HDLC conversion and perform the necessary D channel handshaking.

Note that the active polarity of the DREQUEST and DGRANT signals may be reversed by setting the LAPD polarity control bit (BR7(1)) in the SCP. When BR7(1) is a '0' the active polarity is as described above. Conversely, when BR7(1) is a '1' the MC145474/75 will drive DGRANT to a logic '0' when DGRANT is active and to a logic '1' when DGRANT is inactive. Also, when BR7(1) is '1', DREQUEST will be considered to be ''active low''.

9.3 SETTING THE CLASS FOR TE MODE OF OPERATION

Recommendation CCITT I.430 and ANSI T1.605 specifications mandate two classes of operation for a TE, with respect to D channel operation. These two classes of operation are class 1 and class 2. Each of these classes have two associated priorities, high priority and low priority. These classes and their associated priorities pertain to the number of demodulated E bits required to be '1', before the D channel is deemed to be clear for use. Using the MC145474 in the TE mode of operation, the user programs the device for class 1 or class 2 operation via the SCP bit NR2(0). Using the MC145475 in the TE mode of operation, the user programs the device for class 1 or class 2 operation by either NR2(0) or pin 10. Table 9-3 illustrates how to configure either the MC145474 or the MC145475 for either class 1 or class 2 operation. This table also illustrates when DGRANT will go high. Note that although DGRANT goes high one E bit before the required count, data will not be modulated onto the D bit timeslots in the S/T frame until the required number of E bits = '1' are received. Thus, data gets modulated onto the D channel if the E bit following the low to high transition of DGRANT is '1'.

Table 9-3. MC145474/75 Class Operations

	MC145474	MC145475	Number of E Bits = '1' Required for DGRANT to go High
Class 1	NR2(0) = '0'	NR2(0) = '0' and Pin 10 = '0'	DGRANT goes high after seven E bits = '1' in high priority, and after eight in low priority
Class 2	NR2(0) = '1'	NR2(0) = '1' or Pin 10 = '1'	DGRANT goes high after nine E bits = '1' in high priority, and after ten in low priority.

The device will automatically switch from high to low priority and back, within each class of operation, in accordance with CCITT I.430 and ANSI T1.605.

9.4 GENERATION OF AN INTERRUPT IN THE TE MODE

The MC145474/75 in the TE mode of operation generates an interrupt every time a collision occurs on the D channel. CCITT I.430 and ANSI T1.605 define a collision as having occurred when the demodulated E bit from the NT does not match the previously modulated D bit from the TE. Since the NT reflects back its received D data in the E echo channel, the TE knows that a collision occurring indicates that another TE has gained access to the D channel. When a collision occurs NR3(1) gets set. If the corresponding interrupt enable bit (NR4(1)) is set high, then $\overline{IRQ}$ will go low. The D channel collision interrupt is cleared by writing a '0' to NR3(1).

9.5 GAINING ACCESS TO THE D CHANNEL IN THE NT MODE

When configured as an NT the MC145474/75 has automatic access to the D channel. This is because the S/T interface is designed for communication between a single NT and one or more TEs. As such, the NT does not have to compete for access to the D channel. Thus, there is no DREQUEST or DGRANT functions associated with the NT mode of operation. Data present in the D bit positions of the IDL frame on IDL Rx are modulated onto the D bit timeslots on the S/T loop. Demodulated D channel data from the TE/TEs is transmitted onto IDL Tx in accordance with the IDL specification. The ECHO function of an NT configured S/T transceiver is performed internally in the MC145474/75. To assist in testing an S/T loop the MC145474/75 features the SCP test bits BR7(4) and BR13(2). Setting BR7(4) in the NT mode will invert the E echo channel (i.e., the logical inverse of the demodulated D channel data from the TE/TEs is transmitted in the E channel). Setting BR13(2) to a '1' will force the E channel to all 0s. Refer to Section 8 for a more detailed description of these test bits. Setting BR13(7) to a '1' puts the ''NT configured'' MC145474/75 S/T transceiver into the NT1 Star mode of operation. In this mode, the bits to be ECHOed back to the TE/TEs are obtained from the ECHO IN pin. Refer to Section 11 for a more detailed description of this function.

SECTION 10
MULTIFRAMING

10.1 INTRODUCTION

A layer 1 signalling channel between the NT and TE is provided in the MC145474/75 in accordance with CCITT I.430 and ANSI T1.605. In the NT to TE direction, this layer 1 channel is the S channel. In the TE to NT direction it is the Q channel. The S channel is subdivided into five subchannels: SC1, SC2, SC3, SC4, and SC5. In normal operation the NT sets its Fa bit (bit 14) to a binary zero every frame. The ‘‘wrapping’’ action of the TE/TEs as outlined in CCITT I.430 and ANSI T1.605, causes the Fa bit of the TE/TEs to be a ‘0’ also. This is to ensure the existence of two line code violations per frame, enabling fast synchronization.

Multiframing is activated by the NT by setting the M bit (bit 26) in the NT and TE frame to a binary one, once every 20 frames. In addition to this, the Fa bit (bit 14) in the NT to TE direction is set to a binary one, once every five frames. When multiframing is enabled, the NT sends its S channel data (SC1 through SC5) in the S timeslot (bit 37) every frame. Table 10-1 shows the order in which the S channel data is transmitted. Note that the M bit = ‘1’ sets the multiframe boundary. Once every five frames the Fa bit is set to ‘1’ in the NT to TE direction. This serves as a Q bit identifier for the TE/TEs, who send their Q data in their Fa bit position in the corresponding frames. In order to avoid Q data collision, those TEs who have not been addressed for multiframing, must send ‘1s’ in the Q bit timeslots.

10.2 ACTIVATION/DETECTION OF MULTIFRAMING IN THE MC145474/75

Multiframing is initiated by the NT. Detection and compliance with the multiframe structure is mandatory in the TE/TEs, and is automatic in the MC145474/75. BR7(5) is set to ‘1’ to initiate multiframing in an NT configured MC145474/75. This causes the M bit to be set to ‘1’ in the next frame. Henceforth, the M, S, and Fa bits will automatically comply with the structure as outlined in CCITT I.430 and ANSI T1.605. This format is as shown in Table 10-1. When the TE configured MC145474/75 has detected multiframing, it sets NR1(1) (multiframing detect). Henceforth, it automatically complies with the multiframe format.

10.3 WRITING S CHANNEL DATA TO AN NT CONFIGURED MC145474/75

Data written to BR2(7:4), BR9(7:4), BR9(3:0), BR10(7:4), and BR10(3:0) is transmitted in subchannels SC1, SC2, SC3, SC4, and SC5, respectively. The NT configured MC145474/75 polls these internal registers once every 5 ms (a multiframe is 5 ms in duration). If no new data has been written to these registers, the old data is re-transmitted. When multiframing is disabled, the data in these registers is ignored and the Fa bit is ‘0’. Note that in the NT mode, these registers come out of reset in the all zeros state.

10.4 MULTIFRAME INTERRUPTS IN AN NT CONFIGURED MC145474/75

The NT will generate an interrupt either once every multiframe, or only in the event of a new Q channel nibble having been received. A new Q channel nibble is defined as one which differs from the previous Q nibble.

Table 10-2 illustrates how to configure an NT for either of these options.

Table 10-1. S Channel Data Transmission

Frame No.	NT to TE Fa Bit Position	NT to TE M Bit	NT to TE S Bit	TE to NT Fa Bit Position
1	1	1	SC1.1	Q1
2	0	0	SC2.1	0
3	0	0	SC3.1	0
4	0	0	SC4.1	0
5	0	0	SC5.1	0
6	1	0	SC1.2	Q2
7	0	0	SC2.2	0
8	0	0	SC3.2	0
9	0	0	SC4.2	0
10	0	0	SC5.2	0
11	1	0	SC1.3	Q3
12	0	0	SC2.3	0
13	0	0	SC3.3	0
14	0	0	SC4.3	0
15	0	0	SC5.3	0
16	1	0	SC1.4	Q4
17	0	0	SC2.4	0
18	0	0	SC3.4	0
19	0	0	SC4.4	0
20	0	0	SC5.4	0
1	1	1	SC1.1	Q1
2	0	0	SC2.1	0

Table 10-2. NT Multiframe Interrupts

BR3(2) Interrupt Every Multiframe	NR4(2) Enable Multiframing Interrupt	$\overline{\text{IRQ}}$ MC145474 (Pin 16) MC145475 (Pin 20)
X	0	Multiframing never causes an interrupt
0	1	An interrupt is generated on the reception of a new Q channel nibble
1	1	An interrupt is generated every multiframe

10.5 READING Q CHANNEL DATA FROM AN NT CONFIGURED MC145474/75

The Q data nibble received from the TE/TEs is obtained by reading BR3(7:4). The demodulated Q channel data is written to this register every 5 ms. BR3(7:4) are read only bits.

10.6 WRITING Q CHANNEL DATA TO A TE CONFIGURED MC145474/75

Data written to BR2(7:4) is transmitted in the Q channel. The TE configured MC145474/75 polls this internal register once every 5 ms (a multiframe is 5 ms in duration). If no new data has been written to this register, the old data is re-transmitted. When multiframing is disabled, the data in this register is ignored and the Fa bit obeys the multiframing wrapping criteria as outlined in CCITT I.430 and ANSI T1.605.

BR2(7:4) comes out of reset in the all ones state in the TE mode of operation. To accommodate other TEs on the loop, BR2(7:4) should be left in the all ones state when the TE does not have access to the Q channel.

10.7 MULTIFRAME INTERRUPTS IN A TE CONFIGURED MC145474/75

The TE will generate an interrupt either once every multiframe or only in the event of a new SC1 subchannel nibble having been received. A new SC1 subchannel nibble is defined as one which differs from the previous SC1 nibble. Table 10-3 illustrates how to configure a TE for either of these options.

Table 10-3. TE Multiframe Interrupts

BR3(2) Interrupt Every Multiframe	NR4(2) Enable Multiframing Interrupt	$\overline{\text{IRQ}}$ MC145474 (Pin 16) MC145475 (Pin 20)
X	0	Multiframing never causes an interrupt
0	1	An interrupt is generated on the reception of a new SC1 subchannel nibble
1	1	An interrupt is generated every multiframe

10.8 READING S SUBCHANNEL DATA FROM A TE CONFIGURED MC145474/75

The S subchannel nibbles SC1, SC2, SC3, SC4, and SC5 received from the NT, are obtained by reading BR3(7:4), BR9(7:4), BR9(3:0), BR10(7:4), and BR10(3:0), respectively. The demodulated S subchannel data is written to these registers every 5 ms. These registers are read only registers in the TE mode of operation.

10.9 FAR END CODE VIOLATION (FECV) DETECTION

A Far-End Code Violation (FECV) occurs when a multiframe incoming to the NT from the TE(s) contains one or more illegal S/T line code violations. An FECV maintenance message, as defined in ANSI T1.605, indicates to the TEs that an FECV has occurred. This message is transmitted from the NT to the TEs through the SC1 subchannel. In an NT configured MC145474/75 the ‘‘FECV Detection’’ interrupt (IRQ #6) will indicate that an FECV has occurred. The FECV interrupt status bit is located in NR3(1) and its corresponding enable bit is located in NR4(1).

SECTION 11
NT1 STAR MODE OPERATION

Appendix B of ANSI T1.605 describes an example of an NT that will support multiple T interfaces. This is to accommodate multipoint operation with more than eight TEs. The MC145475 can be configured for NT1 Star mode of operation. This mode is for use in wire ORing multiple NT configured S/T chips on the IDL side. Each NT has a common IDL SYNC, IDL CLK, IDL Tx, and IDL Rx, as shown in Figure 11-1. Each NT is then connected to its own individual S/T loop containing either a single TE or a group of TEs. As such, the contention for either of the B channels or for the D channel is now extended from a single passive bus to a grouping of passive busses.

ISDN employs the use of HDLC data on the D channel. Access to either of the B channels is requested and either granted or denied by the user sending layer 2 frames on the D channel. In normal operation where there is only one NT, the TEs are granted access to the D channel in accordance with their priority and class. By counting the required number of E channel echo bits being '1', the TEs know when the D channel is clear. Thus in the NT1 Star mode of operation, where there are multiple passive busses competing for the same B1, B2, and D channels, the same E echo channel must be transmitted from each NT to its passive bus. This is accomplished in the MC145475 by means of the ANDIN, ANDOUT, and ECHO IN pins.

Figure 11-1 shows how to connect the multiple number of NTs in the NT1 Star mode. Successive connection of the ANDOUT (this is the output of an internal AND gate whose inputs are the demodulated D bits and the data on the ANDIN pin) and ANDIN pins, and the common connections of the ECHO IN pins, succeeds in sending the same E echo channel to each group of TE/TEs. To configure a series of NTs for NT1 Star mode, BR13(7) must be set to '1' in each NT. Data transmitted on IDL Tx in NT1 Star mode, will have the following format: a logic '0' is V_{SS}, a logic '1' causes IDL Tx to go to a high-impedance state. This then permits the series wire ORing of the IDL bus. Note that one of the NTs must have its ANDIN pin pulled high.

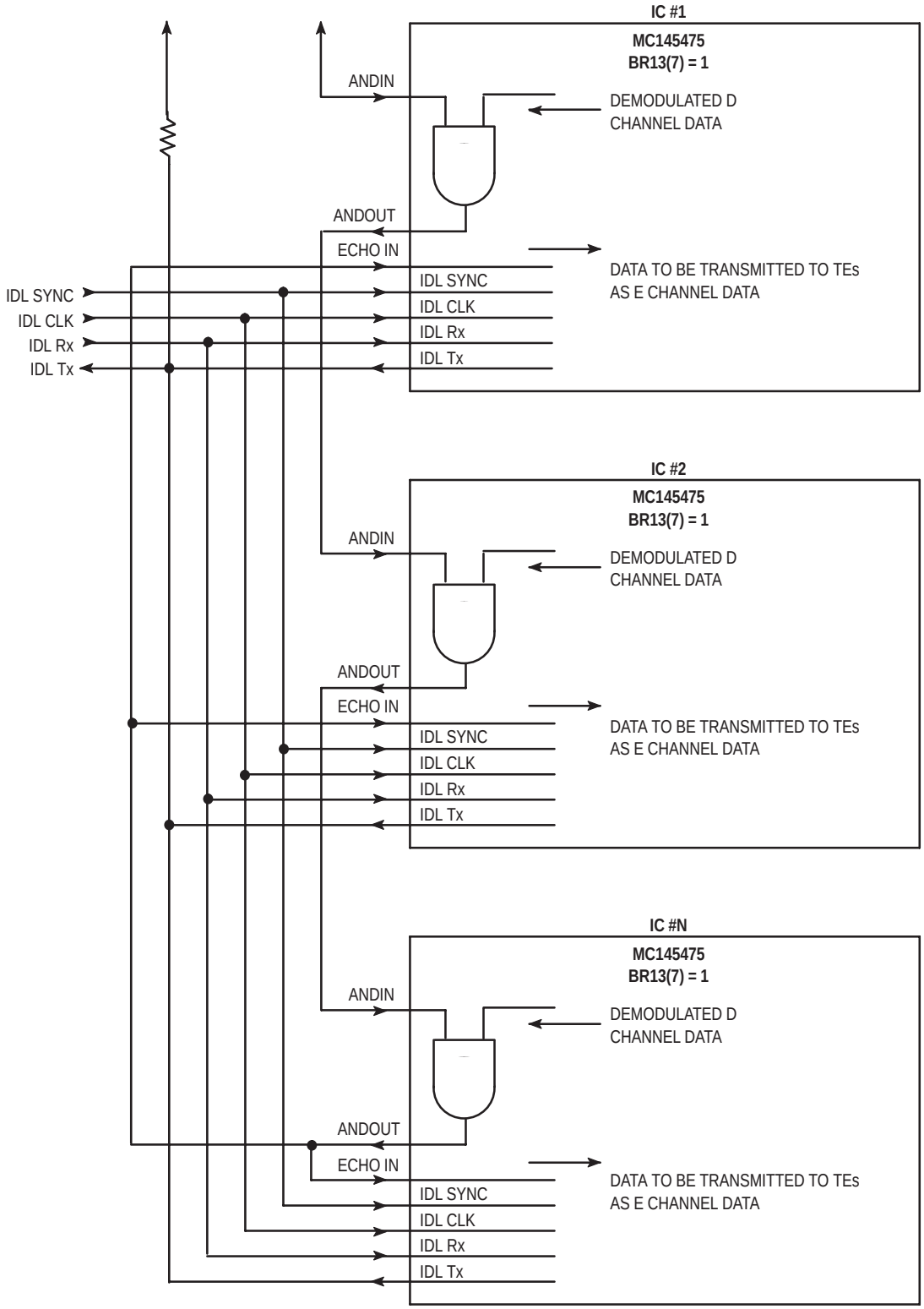


Figure 11-1. NT1 Star Mode of Operation

SECTION 12
IDL FIFOS

12.1 INTRODUCTION

The MC145474 and MC145475 are equipped with two sets of FIFOs: the IDL A and the IDL M. Associated with each of these FIFOs is a transmit and receive section. The IDL A and IDL M FIFOs are independent of each other. Similarly, the transmit and receive FIFOs associated with either the IDL A or IDL M FIFOs are independent of each other. These FIFOs are each four bytes deep. Communication with the FIFOs is made via the SCP and the IDL. These FIFOs are designed to provide two extra communication channels between IDL devices resident on the same printed circuit board (PCB). It is important to note that they have no effect on the operation of the S/T transceiver, their sole function is for interchip communication. Data loaded into the FIFOs never gets transmitted to another S/T device via the S/T interface. Note also that the IDL A and IDL M bits are totally independent of the S/T A and M Bits. As mentioned previously, both the IDL A and IDL M FIFOs have an associated transmit and receive section. The function of the transmit and receive FIFOs is as follows.

12.2 TRANSMIT FIFOs

The transmit FIFOs are shown in Figure 12-1.

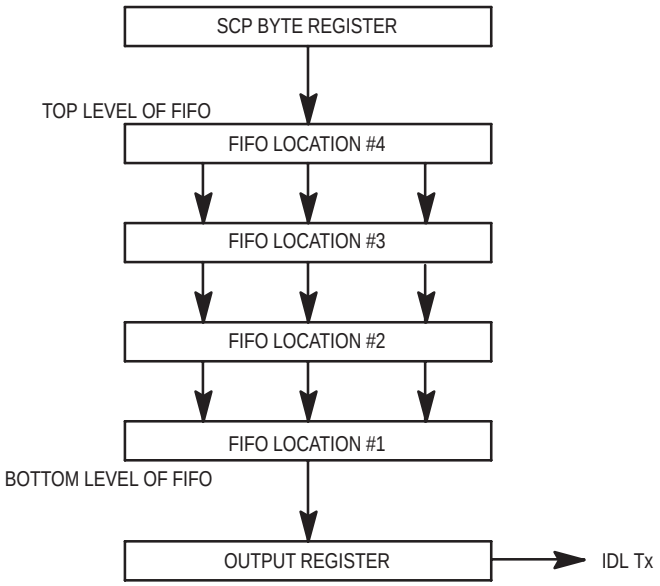


Figure 12-1. Transmit FIFOs

These FIFOs are four bytes deep. Data is loaded into the transmit or output FIFOs via the SCP. In the case of the IDL A transmit FIFOs, data is loaded into the FIFO by writing to BR1. Note that BR1(7) is the MSB and BR1(0) is the LSB of the transmit FIFOs. In the case of the IDL M transmit

FIFOs, data is loaded into the FIFO by writing to BR0. BR0(7) is the MSB and BR0(0) is the LSB. If the FIFO is empty this byte will fall through to FIFO location #1. This corresponds to the bottom level of the FIFO. Subsequent writing to the relevant byte register location will fill the FIFO. If the FIFO continues to be written to while full, the last location will be overwritten, i.e., data resident in FIFO location #4 (the top level of the FIFO) will be overwritten. As soon as FIFO location #1 is filled, it is loaded into the output register. This data is then transmitted out to IDL Tx, MSB first. Data is transmitted out on IDL Tx one bit every IDL frame, i.e., once every 125 μs. In the case of the IDL A transmit FIFOs, data is transmitted in the IDL A timeslot. This is the 10th timeslot of the IDL frame, as indicated in Figure 4-1 in Section 4. Data loaded into the IDL M transmit FIFOs is transmitted out on IDL Tx in the IDL M bit timeslot. The IDL M timeslot is the 20th bit position of the IDL frame, as indicated in Figure 4-1.

When the output register has been completely emptied, i.e., all eight bits have been transmitted out on IDL Tx, the next byte is downloaded. Thus, if a byte had been residing in FIFO location #2 it will be downloaded into FIFO location #1 (FIFO location #1 is duplicated in the output register for transmission out on IDL Tx). Similarly any data residing in FIFO location #3 gets downloaded into FIFO #2, etc. When the FIFOs have been fully flushed out, the last byte will be recirculated, i.e., the last byte will be continuously transmitted until either a new byte is loaded into the FIFOs or the FIFOs are cleared. The transmit FIFOs are reset to the all ones state by application of either a hardware or software reset. Note that the transmit FIFOs are operational regardless of the status of the S/T interface or whether the MC145474/75 is configured as an NT or as a TE.

12.3 RECEIVE FIFOs

The schematic equivalent of the IDL receive FIFOs is shown in Figure 12-2. Data is loaded into the IDL receive FIFOs via the IDL Rx pin. Data is loaded into the receive FIFOs one bit every IDL frame, i.e., once every 125 μs. In the case of the IDL A receive FIFOs, data is received in the IDL A timeslot. This is the 10th timeslot of the IDL frame, as indicated in Figure 4-1. Data loaded into the IDL M receive FIFOs enters the device via IDL Rx in the IDL M bit timeslot. The IDL M timeslot is the 20th bit position of the IDL frame, as indicated in Figure 4-1. The flow control for the IDL receive FIFOs is discussed in Section 12.3.3.

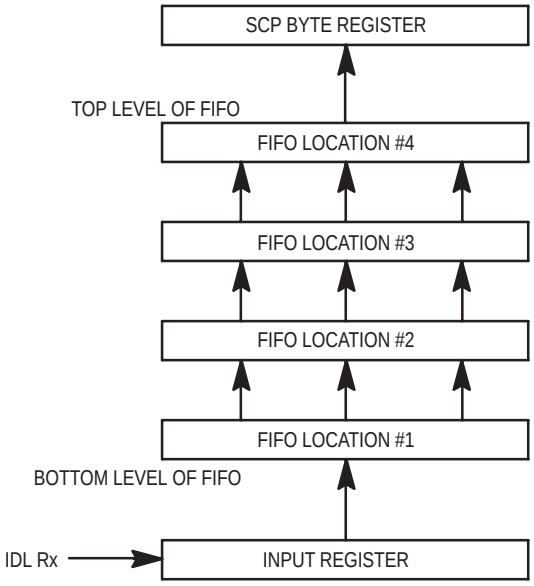


Figure 12-2. Receive FIFOs

After the first eight bits have been clocked into the input register, they are uploaded to the topmost empty position of the receive FIFOs. If the FIFOs had been empty this corresponds to FIFO location #4, the top level of the FIFO. Every time a byte is loaded into the receive FIFOs an interrupt is generated. Generation and subsequent clearing of the interrupts caused by the IDL A and IDL M FIFOs are discussed in Sections 12.3.1 and 12.3.2. Note that data is clocked into the receive FIFOs MSB first. Data can be read out from the receive FIFOs by an SCP read. Reading BR1 corresponds to reading the IDL A receive FIFOs. Similarly reading BR0 corresponds to reading the IDL M receive FIFOs. Reading the IDL receive FIFOs by doing an SCP read, corresponds to reading the top level of the receive FIFO. This corresponds to reading FIFO location #4. As soon as an SCP read has been performed, all bytes are shifted upwards, i.e., if a byte had been residing in FIFO location #3 it gets upshifted to FIFO location #4, etc. Note that application of either a hardware or software reset will clear the receive FIFOs, resetting them to the all zeros state.

An indication of how full the IDL receive FIFOs are can be obtained by reading the IDL receive FIFO ≤ 1/2 full bit. For the IDL A FIFOs this bit is BR8(6), for the IDL M FIFOs this bit is BR8(7). When the IDL receive FIFOs are less than or equal to half full, this bit is internally set to '1'. Since the FIFOs are four bytes deep this bit will be internally set to '1' whenever there are 0, 1, or 2 bytes resident in the IDL receive FIFOs. BR8(7) and BR8(6) are reset to '0' by application of either a hardware or software reset since this resets the receive FIFOs to the all zeros state. Note that the receive FIFOs are operational regardless of the status of the S/T interface or whether the MC145474/75 is configured as an NT or as a TE.

12.3.1 Generation and Clearing of IRQ #4

When a byte has been loaded into the IDL A receive FIFOs an interrupt is generated provided the corresponding interrupt enable has been set to '1'. The interrupt enable corresponding to IRQ #4 is BR8(3). When the interrupt is generated IRQ #4 (BR8(1)) is set to '1'. The interrupt is cleared by reading the IDL A receive FIFOs, i.e., reading BR1. Note that application of either a hardware or software reset will reset the IDL A receive FIFOs to the all zeros state. Application of either a hardware or software reset will also clear IRQ #4.

12.3.2 Generation and Clearing of IRQ #5

When a byte has been loaded into the IDL M receive FIFOs an interrupt is generated provided the corresponding interrupt enable has been set to '1'. The interrupt enable corresponding to IRQ #5 is BR8(2). When the interrupt is generated IRQ #5 (BR8(0)) is set to '1'. The interrupt is cleared by reading the IDL M receive FIFOs, i.e., reading BR0. Note that application of either a hardware or software reset will reset the IDL M receive FIFOs to the all zeros state. Application of either a hardware or software reset will also clear IRQ #5.

12.3.3 Flow Control of IDL Receive FIFOs

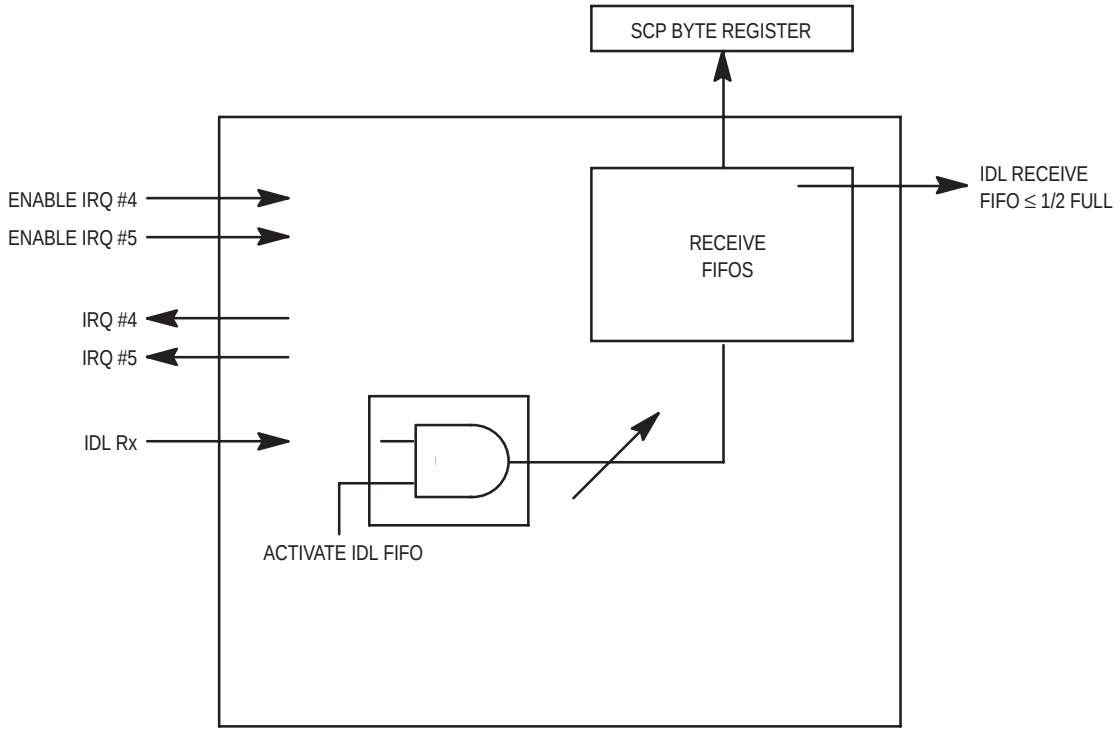
Flow control is provided for the IDL A and IDL M receive FIFOs. The flow control is as schematically depicted in Figure 12-3. In order for data to enter the IDL receive FIFOs the activate IDL FIFO bit must be set to '1'. The activate IDL A FIFO bit for the IDL A receive FIFOs is NR6(1). Correspondingly, the activate IDL M FIFO bit for the IDL M receive FIFOs is NR6(2).

After the activate IDL FIFO bit has been set to '1', data can enter the IDL receive FIFOs via the IDL Rx pin (data enters the IDL A receive FIFOs from the IDL A timeslot position, data enters the IDL

M receive FIFOs from the IDL M timeslot position). A further condition can be placed on the data prior to its being loaded into the IDL receive FIFOs. This condition is called the HOZ condition. The HOZ condition is enabled for the IDL A receive FIFOs by setting BR8(4) to a ‘1’. Correspondingly, the HOZ condition is enabled for the IDL M receive FIFOs by setting BR8(5).

When the HOZ condition is disabled data will be loaded into the IDL receive FIFOs on eight bit boundaries after the setting of the activate IDL FIFO bit to ‘1’. When the HOZ condition is enabled (the HOZ condition is enabled by setting the HOZ bit to ‘1’) data received via the IDL A and IDL M timeslots will be internally monitored by the device. (Note that the activate IDL FIFO bit must be set to ‘1’ after the HOZ bit has been set to ‘1’). Data received in the IDL A and IDL M timeslots will be ignored until the first ‘0’ is received. Upon reception of the first ‘0’, data will subsequently be loaded into the receive FIFOs (data received in the IDL A timeslot gets loaded into the IDL A receive FIFOs, data received in the IDL M timeslot gets loaded into the IDL M receive FIFOs) on eight bit boundaries, until the FIFOs are filled. Note that the first ‘0’ received will be the MSB of the first byte loaded into the receive FIFOs. Note also that after the first ‘0’ has been received the HOZ bit will be internally reset to ‘0’. For correct use of the HOZ flow control one should first set the HOZ bit to ‘1’ and then set the activate IDL FIFO bit to ‘1’.

After reading a byte from the FIFOs, the data is upshifted. If the IDL receive FIFO is not read after being filled up, then the last byte will be overwritten. This corresponds to FIFO location #1 as shown in Figure 12-2. When the FIFOs have been completely emptied then the whole process can be repeated i.e., set the activate and/or set the HOZ. Note that the HOZ flow control is optional, but if this control is being used it should be set to ‘1’ prior to the activate IDL FIFO bit being set to ‘1’.



NOTES:
1. HOZ set. Data gets loaded into FIFOs after first ‘0’ received.
2. HOZ not set. Data gets loaded into FIFO immediately.

Figure 12-3. Flow Control for Receive FIFOs

SECTION 13
INTERRUPTS

13.1 INTRODUCTION

The MC145474/75 when configured as a TE is equipped with five interrupt modes (IRQ #1 through IRQ #5). When the MC145474/75 is configured as an NT, it is also equipped with five interrupt modes (IRQ #2 through IRQ #6). Each of these interrupts is maskable. When an interrupt occurs (and if the interrupt condition is enabled), the MC145474/75 asserts the $\overline{\text{IRQ}}$ pin. A detailed description of these interrupts and how they are cleared is as follows.

13.2 IRQ #1 NR3(1) — TE: D CHANNEL COLLISION
NT: NOT APPLICABLE
NR4(1) — ENABLE

IRQ #1 is used in the TE mode of operation of the MC145474/75 to indicate to external devices that a collision has occurred on the D channel. A D-channel collision is considered to have occurred when the TE is transmitting on the D channel (both DREQUEST and DGRANT being high) and the received E echo bit from the NT does not match the previously modulated D bit. When IRQ #1 occurs the MC145474/75 internally sets NR3(1) to a '1'. If the IRQ #1 ENABLE is set to '1' an interrupt to an external device will be generated. The interrupt condition is cleared by writing a '0' to NR3(1). Note that this bit is maskable by means of NR4(1). This interrupt is only applicable in the TE mode of operation and hence is not available in the NT mode.

13.3 IRQ #2 NR3(2) — MULTIFRAME RECEPTION
NR4(2) — ENABLE

IRQ #2 is provided for multiframing reception indication. This interrupt is applicable and available in both NT and TE modes of operation of the MC145474/75. Note that this interrupt is maskable by means of NR4(2). Multiframing is initiated by the NT by setting BR7(5). A multiframe is 20 basic frames or 5 ms in duration. If this interrupt is enabled (it is enabled by setting NR4(2)) and if multiframing is in progress, then an interrupt will be generated on multiframe boundaries, i.e., every 5 ms. Alternatively an NT configured MC145474/75 can be programmed to generate an interrupt only in the event of a new Q channel nibble having been received. Similarly a TE configured MC145474/75 can be programmed to generate an interrupt only in the event or a new SC1 subchannel having been received. Refer to Section 10 for a detailed description of these features.

If an interrupt is to occur it will do so in the 47th baud of the transmitted frame of the 20th frame in a multiframe. Data to be transmitted in the SC1 through SC5 subchannels in the NT is internally latched from BR2(7:4), BR9(7:0), and BR10(7:0) during the 47th baud of the transmitted frame of the 20th frame in a multiframe. At this time the received Q channel nibble is made available by internally latching the data to BR3(7:4). Similarly, data to be transmitted in the Q channel of the TE is internally latched from BR2(7:4) during the 47th baud of the transmitted INFO 3 in the 20th frame of a multiframe. At this time the received SC1 through SC5 subchannel nibbles are also made available. A mutiframing interrupt is cleared by reading BR3. Reading BR3 will clear the interrupt

in both the NT and TE modes of operation, regardless of whether the MC145474/75 is configured to generate an interrupt in the event of a new nibble or every multiframe. Note that NR3(2) is a read only bit.

13.4 IRQ #3 NR3(3) — CHANGE IN Rx INFO STATE
NR4(3) — ENABLE

IRQ #3 is provided to indicate a change in the received INFO state of the transceiver. In the NT mode, this corresponds to a change in the receiving INFO 0, INFO 1, INFO 3, or INFO X state. Alternatively, in the TE mode this corresponds to a change in the receiving INFO 0, INFO 2, INFO 4, or INFO X state. Thus, when a change occurs in one of these states the MC145474/75 internally sets NR3(3) to a '1'. If the IRQ #3 ENABLE is set to '1' an interrupt to an external device will be generated. IRQ #3 can be cleared by writing a '0' to NR3(3). This bit is reset by a software reset or a hardware reset. Note that the transmission states for the NT (INFO 0, INFO 2, and INFO 4) and for the TE (INFO 0, INFO 1, and INFO 3) are as defined in Section 3. INFO X is defined as any transmission state other than those states. An example of such a state would be when the MC145474/75 is programmed to transmit a 96 kHz test tone (BR11(0) = '1'). The MC145474/75 comes out of reset in the receiving ''INFO X'' state. Hence IRQ #3 will be generated when it recognizes either INFO 0, INFO 1, INFO 2, INFO 3, or INFO 4. Note that NR3(3) is a read/write bit.

13.5 IRQ #4 BR8(1) — IDL A CHANNEL FIFO INTERRUPT
BR8(3) — ENABLE

The interrupt request condition IRQ #4 is generated whenever an IDL A channel byte is present at the top of the A channel input FIFOs. This byte will have been loaded into the IDL A channel input FIFOs from IDL Rx in the IDL A channel timeslot. IRQ #4 is cleared by reading BR1. This bit is cleared by application of either a hardware or software reset.

13.6 IRQ #5 BR8(0) — IDL M CHANNEL FIFO INTERRUPT
BR8(2) — ENABLE

The interrupt request condition IRQ #5 is generated whenever an IDL M channel byte is present at the top of the M channel input FIFOs. This byte will have been loaded into the IDL M channel input FIFOs from IDL Rx in the IDL M channel timeslot. IRQ #5 is cleared by reading BR0. This bit is cleared by application of either a hardware or software reset.

13.7 IRQ #6 NR3(1) — NT: FAR-END CODE VIOLATION (FECV) DETECTION
TE: NOT APPLICABLE
NR4(1) — ENABLE

The interrupt request condition IRQ #6 is generated when the NT has detected a Far-End Code Violation (FECV). An FECV occurs when a multiframe incoming to the NT from the TE(s) contains one or more illegal S/T line code violations. This interrupt is used to indicate to an NT when to send an FECV layer 1 maintenance message to the TEs as defined in ANSI T1.605. When IRQ #6 occurs the MC145474/75 internally sets NR3(1) to a '1'. If the IRQ #6 ENABLE is set to '1' an interrupt to an external device will be generated. The interrupt condition is cleared by writing a '0' to NR3(1). Note that this bit is maskable by means of NR4(1). This interrupt is applicable in the NT mode of operation and only when multiframing has been enabled.

SECTION 14
TRANSMISSION LINE INTERFACE CIRCUITRY

14.1 INTRODUCTION

The MC145474/75 is an ISDN S/T transceiver fully compliant with CCITT I.430 and ANSI T1.605. As such it is designed to interface with a four wire transmission medium, one pair being the transmit path, the other pair the receive path. TxP and TxN, a fully differential output transmit pair from the MC145474/75, are designed to interface to the transmit pair of the transmission medium via auxiliary discrete components and a 1:1 turns ratio transformer. RxP and RxN are a high-impedance differential input pair used for coupling the receive line signal through a 1:1 turns ratio transformer.

14.2 TRANSMIT LINE INTERFACE CIRCUITRY

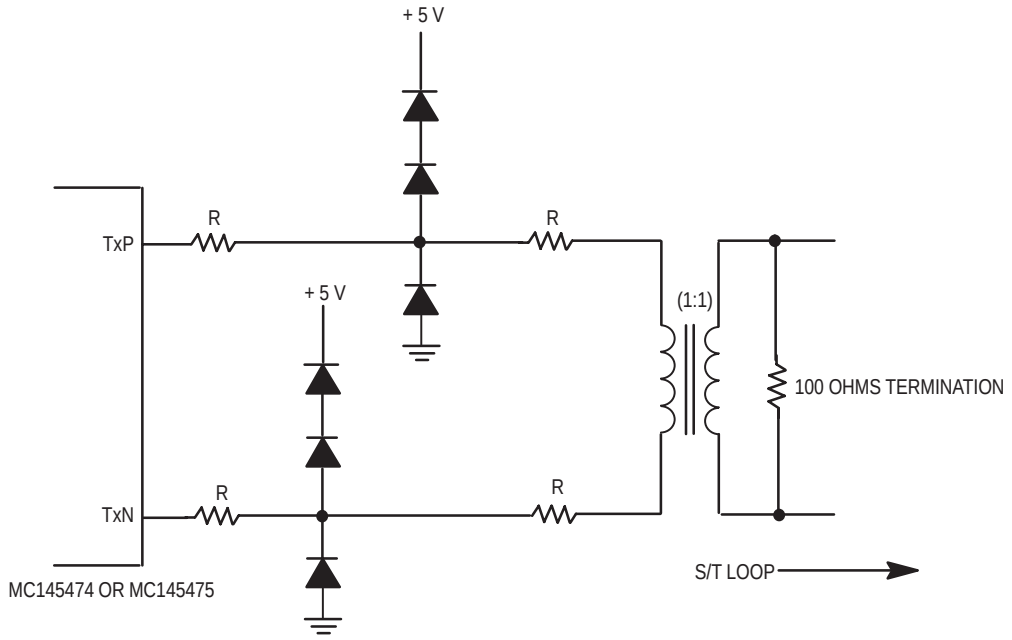
The TxP and TxN pins on the MC145474/75 act as a current limited differential voltage source pair. The TxP and TxN pair behave as active drivers when creating logical zero line signals (CCITT I.430 and ANSI T1.605 define the nominal pulse amplitude to be 750 mV, zero to peak, for a 50-ohm load) and are high-impedance outputs when generating logical one signals. The transmit circuitry within the S/T transceiver is designed to operate with a 1:1 turns ratio line interface transformer. The transmit transformer is similar in design to the receive transformer.

The TxP and TxN pair operate as a 1.17-volt current limited differential voltage source. As such two 1% series resistors should be inserted in the line interface circuit such that the combined resistance of these two resistors and the winding resistance of the transformer is 26.4 ohms. The current limit value is set by circuitry within the S/T transceiver and is approximately 18 milliamperes.

The TxP and TxN transmit pair will supply a current such that a positive potential is created between the TxP and TxN pins, respectively, when transmitting the F frame bit of each frame. The TxP and TxN line drive circuit of the MC145474/75 S/T transceiver is designed such that the device will continue to provide a high-impedance circuit to the transmit pair of the S/T loop when power is removed (i.e., when the circuit between V_{DD} and V_{SS} becomes a short circuit). Figure 14-1 illustrates the recommended line interface and protection circuitry for interfacing the MC145474/75 to the S/T loop.

14.3 RECEIVE LINE INTERFACE CIRCUITRY

The RxP and RxN pins serve as a fully differential input pair for the line signal from the S/T loop. The input impedance seen looking into the combination of the MC145474/75 and the associated receive line interface circuitry (as shown in Figure 14-2) exceeds the CCITT I.430 and ANSI T1.605 requirements under all conditions. The receive line circuitry within the MC145474/75 S/T transceiver is designed to operate with a 1:1 turns ratio transformer. The receive transformer is similar in design to the transmit transformer and recommended suppliers of these transformers are included.



NOTE: 4R + winding resistance = 26.4 ohms.

Figure 14-1. Transmit Line Interface Circuit

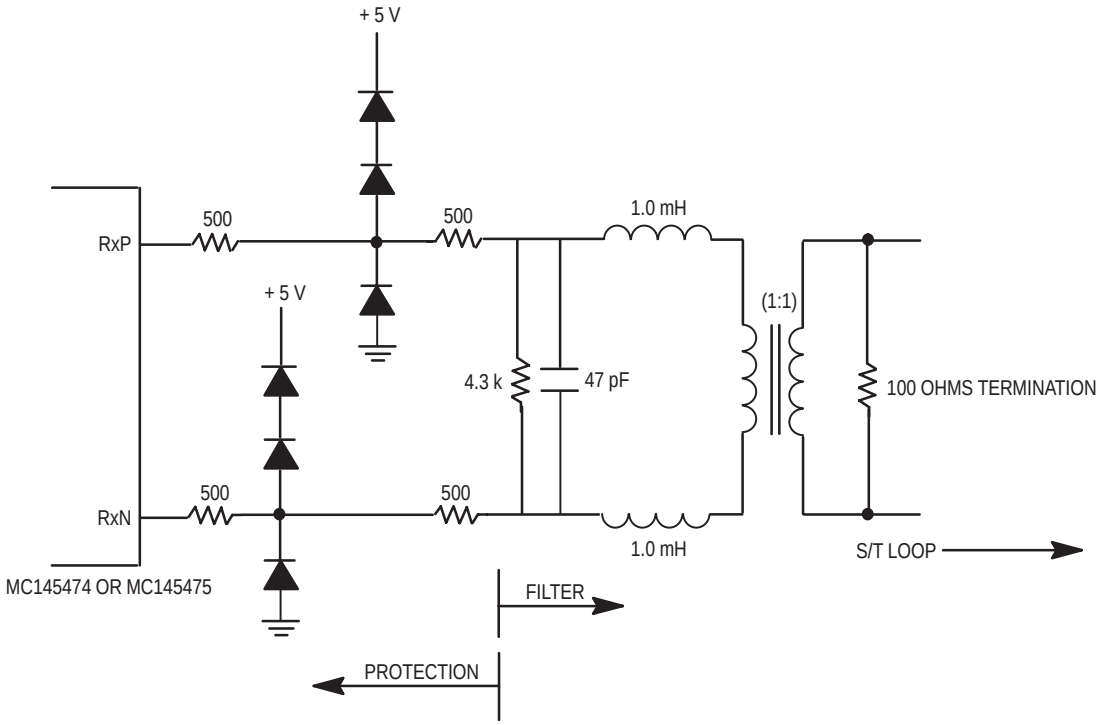


Figure 14-2. Receive Line Interface Circuit

The receive circuitry within the MC145474/75 automatically adapts to the optimum ternary detection thresholds for receiving the incoming line signal, regardless of the S/T loop bus configuration. The minimum ternary detection threshold is 90 mV, referenced to signal ground. This

value then sets the absolute maximum attenuation that can exist, before detection of the incoming signal becomes impossible. The RxP and RxN pair are not sensitive to the polarity of their connection to the line interface circuitry. An optional low pass filter may be included in the receive line interface circuitry of the MC145474/75. The filters break frequency should be greater than or equal to 500 kHz. The filter may be first or second order. The MC145474/75 configured as a TE compensates for the delay through the filter by 250 ns, i.e. the actual turnaround time from receive to transmit in the TE mode is 10.17 μs (10.42 μs (2 baud delay) minus 250 ns) . Figure 14-2 illustrates the recommended line interface and protection circuitry for interfacing the MC145474/75 S/T transceiver to the loop. An optional low pass filter with a break frequency at 500 kHz is included in this figure.

14.4 ADDITIONAL NOTES

14.4.1 Sources of Line Interface Transformers

Line interface transformers for use with the MC145474/75 S/T may be obtained from the following manufacturers:

Coilcraft
1102 Silver Lake Road
Cary, Illinois 60013
(708) 639-6400
Part #K0065-A

Pulse Engineering
12220 World Trade Drive
San Diego, California 92112
(619) 674-8100
Part #PE 64993 (single)
Part #PE 65493 (dual)

Shott Corporation
1000 Parkers Lake Road
Wazata, Minnesota 55391
(612) 475-1173
Part #67128920

Motorola cannot recommend one manufacturer over another and in no way implies that this is a complete listing.

14.4.2 Termination Resistors

Note that the 100-ohm termination resistors in the transmit and receive Line circuitry as shown in Figures 14-1 and 14-2 are mandatory when operating as an NT in accordance with CCITT I.430 and ANSI T1.605. When operating as a TE in point-to-point mode these are also required. However, when configured as a TE in the passive bus arrangement, only one TE has these termination resistors.

14.4.3 Protection Diodes

CCITT I.430 and ANSI T1.605 specify that the S/T interface voltage cannot exceed 1.6 times the nominal voltage of 750 mV (= 1.2 V). Since the MC145474/75 is designed to operate with 1:1 turns

ratio transformers, then the diode structure as illustrated in Figures 14-1 and 14-2 is required to provide protection, while not adversely affecting the S/T interface when power is removed from the device.

14.4.4 Printed Circuit Board (PCB) Layout Recommendations

- Because of the differential nature of the transmit and receive circuitry maximum performance will be achieved when traces and component placement are kept as symmetrical as possible in between the connector (usually an ISDN modular telephone jack) and the TxP/TxN and RxP/RxN pins. This will minimize unbalances that could occur within each of these two circuits.

- Use short low inductance traces for the transmit circuitry, receive circuitry and ISET resistor to reduce inductive, capacitive, and radio frequency noise sensitivities.

- Keep digital signals as far away from the analog signals as possible. The analog signals are the TxP/TxN and RxP/RxN pairs as well as the ISET pin.

SECTION 15
ELECTRICAL SPECIFICATIONS

15.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage (any pin to V_{SS})	V_{in}	– 0.3 to V_{DD} to + 0.3	V
DC Current, any pin (excluding V_{DD}, V_{SS}, TxP, and TxN)	I	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \geq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

15.2 DIGITAL DC ELECTRICAL CHARACTERICS (CMOS MODE, BR13(6) = 0)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	3.5	—	V
Input Low Voltage	V_{IL}	– 0.3	1.5	V
Input Leakage Current @ 5.5 V	I_{in}	—	5	µA
High-Impedance Input Current @ 4.5/0.5 V	$I_{lkg(Z)}$	—	10	µA
Input Capacitance	C_{in}	—	10	pF
Output High Voltage (I_{OH} = – 400 µA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 5.0 mA)	V_{OL}	—	0.5	V
XTAL Input High Level	$V_{IH(X)}$	3.5	—	V
XTAL Input Low Level	$V_{IL(X)}$	—	0.5	V
EXTAL Output Current (V_{OH} = 4.6 V)	$I_{OH(X)}$	—	– 400	µA
EXTAL Output Current (V_{OL} = 0.4 V)	$I_{OL(X)}$	—	400	µA
$\overline{IRQ}$ Output Low Current (V_{OL} = 0.4 V)		—	1.7	mA
$\overline{IRQ}$ Output Off State Impedance		100	—	kΩ

15.3 DC ELECTRICAL CHARACTERISTICS (TTL MODE, BR13(6) = 1)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V
Input Low Voltage	V_{IL}	– 0.3	0.8	V

The MC145474/75 can be programmed to accept TTL levels on all digital input pins (this does not include XTAL and EXTAL). The MC145474/75 is configured for TTL mode by writing a '1' to BR13(6). Programming the MC145474/75 for TTL mode has no effect on either the digital output pins, the crystal circuit, TxP/TxN, or RxP/RxN. Thus, the only dc electrical characteristics that differ, when operating in the CMOS mode, are the input voltages accepted on the digital inputs.

15.4 ANALOG CHARACTERISTICS

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristic	Min	Typ	Max	Unit
TxP/TxN Drive Current: R_L = 50 Ω	13.5	15	16.5	mA
(TxP – TxN) Voltage Limit	—	—	1.17	Vpeak
Input Amplitude (RxP – RxN)	35	—	—	mVpeak

15.5 POWER DISSIPATION

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristic	Min	Typ	Max	Unit	Notes
DC Supply Voltage (V_{DD})	4.5	5.0	5.5	V	
Worst Case Power Consumption	—	—	175	mW	1
Transmit Power Down (NR1(2) = 1)	—	—	75	mW	2
Absolute Minimum Power (NR1(1) = 1)	—	—	40	mW	2

NOTES:
1. The worst case power consumption occurs when the MC145474/75 is transmitting a 96 kHz test tone (BR11(0) = 1) into a 50 ohm load resistor. The 15.36 MHz clock is being provided by the crystal as depicted in Figure 6-3.
2. The power consumption figures for transmit power down and absolute minimum power are both determined with the crystal circuit as depicted in Figure 6-3 still connected and operational.

15.6 IDL TIMING CHARACTERISTICS (NT MODE, IDL SLAVE)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive IDL SYNCs	NOTE 1		
2	IDL SYNC Active After IDL CLK Falling Edge (Hold Time)	30	—	ns
3	IDL SYNC Active Before IDL CLK Falling Edge (Setup Time)	30	—	ns
4	IDL CLK Period	NOTE 2		
5	IDL CLK Width High	70	—	ns
6	IDL CLK Width Low	70	—	ns
7	IDL Rx Valid Before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid After IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High-Impedance	—	30	ns
10	IDL Tx High-Impedance to Active State	—	70	ns
11	IDL CLK to IDL Tx Active	—	70	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described in Section 4.
2. IDL CLK input frequency can be run at 1.536 MHz, 1.544 MHz, 2.048 MHz, 2.56 MHz, or 4.098 MHz.

15.7 IDL TIMING CHARACTERISTICS

(NT mode IDL master or TE mode with the IDL CLK rate set to 2.56 MHz)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive IDL SYNCs	NOTE 1		
2	IDL SYNC Active After IDL CLK Falling Edge (Hold iIme)	160	230	ns
3	IDL SYNC Active Before IDL CLK Falling Edge (Setup Time)	160	230	ns
4	IDL CLK Period	NOTE 2		
5	IDL CLK Width High	NOTE 2		
6	IDL CLK Width Low	NOTE 2		
7	IDL Rx Valid Before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid After IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High-Impedance	0	30	ns
10	IDL Tx High-Impedance to Active State	—	45	ns
11	IDL CLK to IDL Tx Active	—	45	ns

NOTES:

1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described in Section 4.
2. In NT mode IDL master or TE mode, the IDL CLK is generated internally in the MC145474/75. When configured for 2.56 MHz operation IDL CLK is the crystal frequency divided by six, and has a 50% duty cycle.

15.8 IDL TIMING CHARACTERISTICS

(NT mode IDL master or TE mode with the IDL CLK rate set to 2.048 MHz)

(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Reference Number	Characteristic	Min	Max	Unit
1	Time Between Successive IDL SYNCs	NOTE 1		
2	IDL SYNC Active After IDL CLK Falling Edge (Hold Time)	210	280	ns
3	IDL SYNC Active Before IDL CLK Falling Edge (Setup Time)	210	280	ns
4	IDL CLK Period	NOTE 2		
5	IDL CLK Width High	NOTE 2		
6	IDL CLK Width Low	NOTE 2		
7	IDL Rx Valid Before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid After IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High-Impedance	0	30	ns
10	IDL Tx High-Impedance to Active State	—	45	ns
11	IDL CLK to IDL Tx Active	—	45	ns

NOTES:

1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described in Section 4.
2. In NT mode IDL master or TE mode, the IDL CLK is generated internally in the MC145474/75. When configured for 2.048 MHz operation IDL CLK is the crystal frequency divided by 7.5, and has a 53.3% duty cycle.

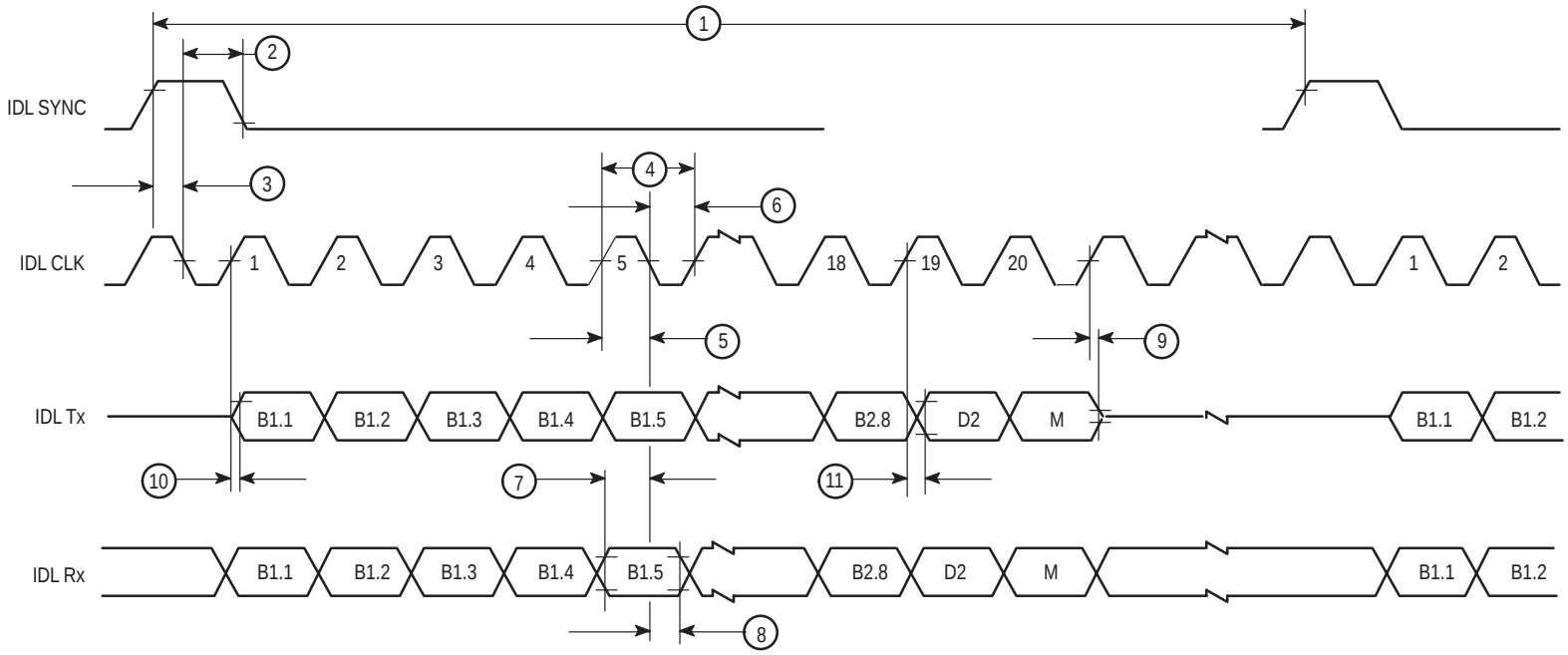
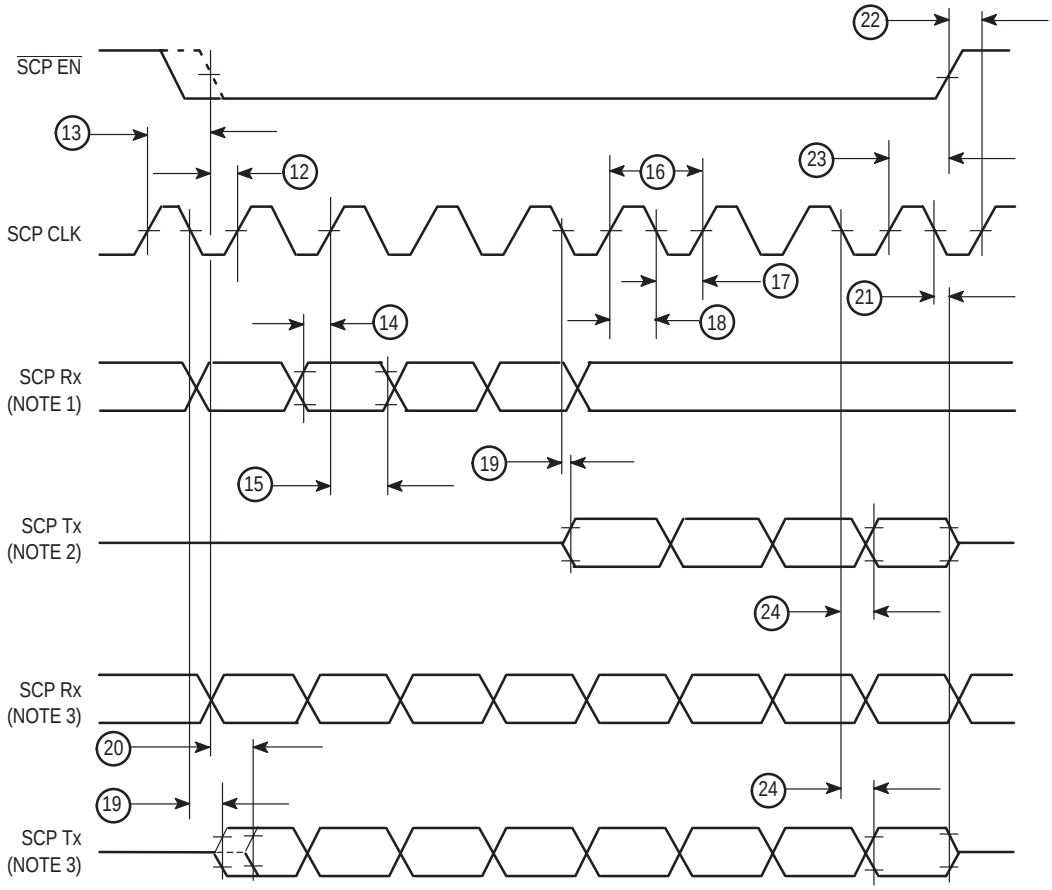


Figure 15-1. IDL Timing Characteristics

15.9 SCP TIMING CHARACTERISTICS

Reference Number	Characteristic	Min	Max	Unit	Notes
12	$\overline{\text{SCP EN}}$ Active Before Rising Edge of SCP CLK	50	—	ns	
13	SCP CLK Rising Edge Before $\overline{\text{SCP EN}}$ Active	50	—	ns	
14	SCP Rx Valid Before SCP CLK Rising Edge (Setup Time)	35	—	ns	
15	SCP Rx Valid After SCP CLK Rising Edge (Hold Time)	20	—	ns	
16	SCP CLK Period	244	—	ns	1
17	SCP CLK Width (Low)	30	—	ns	
18	SCP CLK Width (High)	30	—	ns	
19	SCP Tx Active Delay	0	50	ns	
20	$\overline{\text{SCP EN}}$ Active to SCP Tx Active	0	50	ns	
21	SCP CLK Falling Edge to SCP Tx High-Impedance	—	30	ns	
22	$\overline{\text{SCP EN}}$ Inactive Before SCP CLK Rising Edge	50	—	ns	
23	SCP CLK Rising Edge Before $\overline{\text{SCP EN}}$ Inactive	50	—	ns	
24	SCP CLK Falling Edge to SCP Tx Valid Data	0	50	ns	

NOTES:
1. Maximum SCP Clock frequency is 4.096 MHz.



NOTES:

1. During a nibble read, four bits are presented on SCP Rx.
2. During a nibble read, SCP Tx will be active for the duration of the 4-bit transmission as shown.
3. A byte transaction consists of two eight bit exchanges. During the first exchange, whether a read or a write, 8 bits (the byte register address) are presented on SCP Rx. In the second exchange, 8 bits are presented on SCP Tx during a byte read. During a byte write, the second exchange consists of 8 bits presented to SCP Rx. Refer to Section 5, "The Serial Control Port", for a detailed description.

Figure 15-2. SCP Timing Characteristics

15.10 NT1 STAR MODE TIMING CHARACTERISTICS

Reference Number	Characteristic	Min	Max	Unit
25	Propagation Delay from ANDIN to ANDOUT, While Receiving INFO 0	—	30	ns

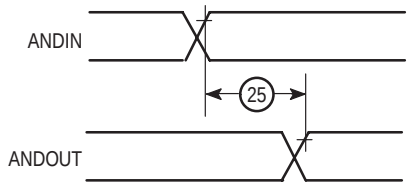


Figure 15-3. NT1 Star Mode

15.11 D CHANNEL TIMING CHARACTERISTICS (TE Mode)

Reference Number	Characteristic	Min	Max	Unit
26	DREQUEST Valid Before Falling Edge of IDL SYNC	30	—	ns
27	DREQUEST Valid After Falling Edge of IDL SYNC	30	—	ns
28	DGRANT Valid Before Falling Edge of IDL SYNC	390	—	ns

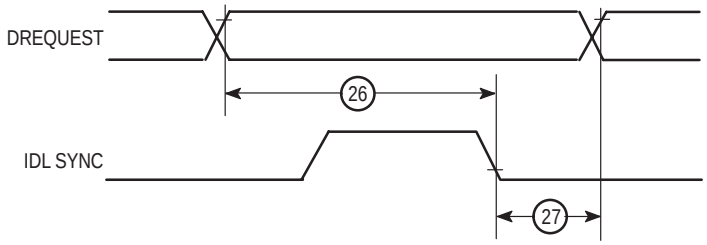


Figure 15-4. D Channel Timing

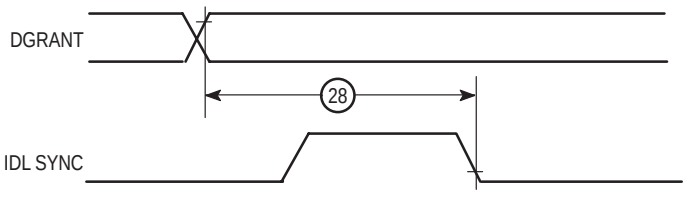


Figure 15-5. D Channel Timing

SECTION 16
MECHANICAL DATA

16.1 PIN ASSIGNMENT

The Motorola MC145474/75 ISDN S/T transceiver is available in both 22- and 28-pin versions, MC145474 being the 22-pin version (see Figure 16-1) and the MC145475 the 28-pin version (see Figure 16-2).

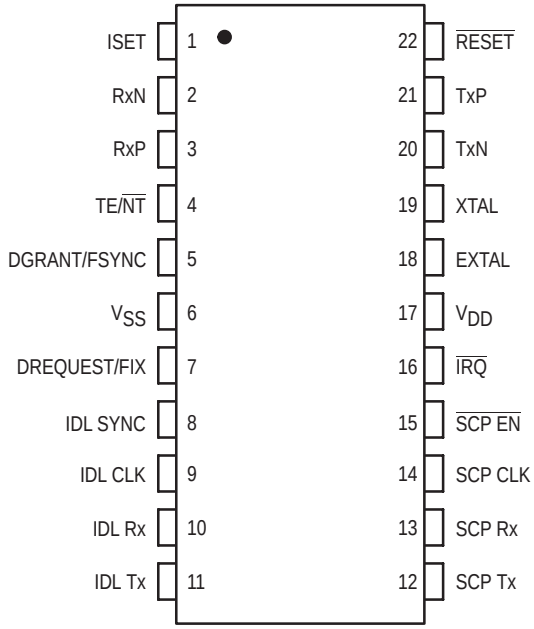


Figure 16-1. MC145474 Pin Assignment

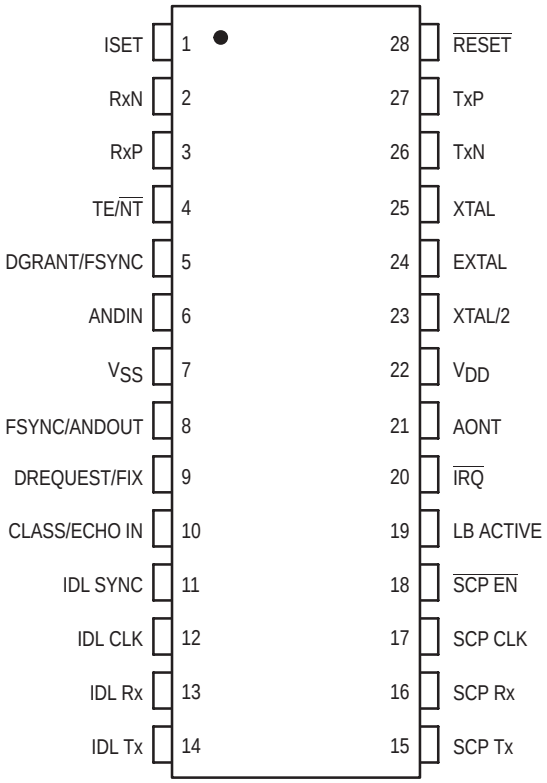
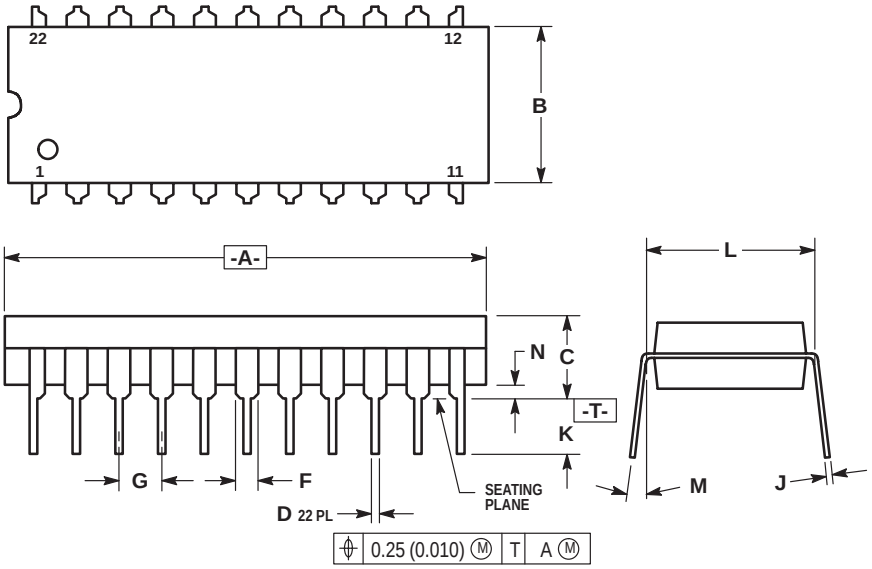


Figure 16-2. MC145475 Pin Assignment

16.2 PACKAGE DIMENSIONS

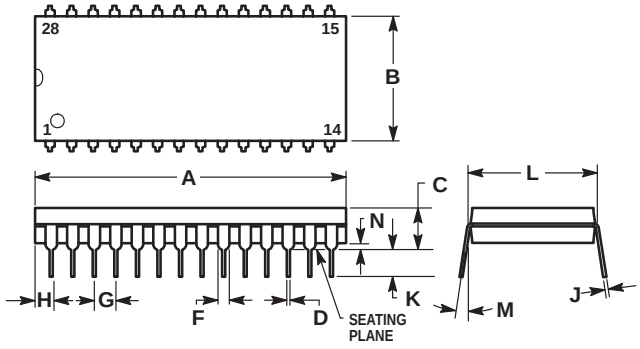
MC145474P
CASE 736A-01



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.65	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.74	4.57	0.155	0.180
D	0.38	0.55	0.015	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

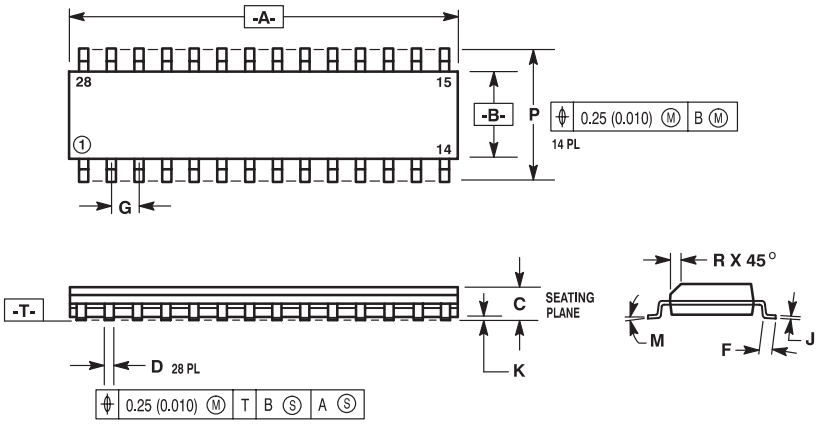
MC145475P
CASE 710-02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STANDARD 710-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

MC145475DW
CASE 751F-03



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Literature Distribution Centers:

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