

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K04FE

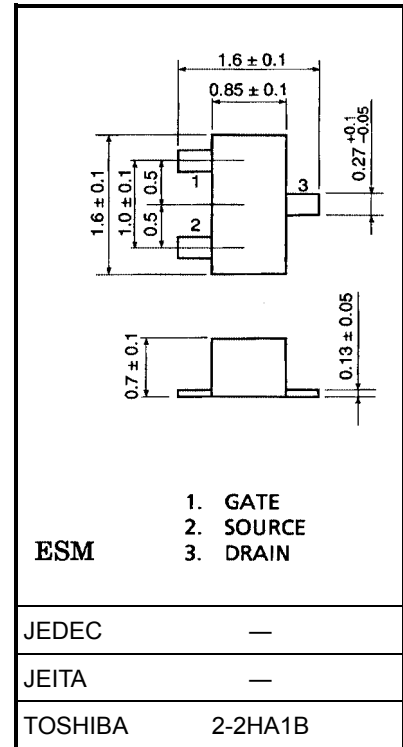
High Speed Switching Applications

- With built-in gate-source resistor: $R_{GS} = 1\text{ M}\Omega$ (typ.)
- 2.5 V gate drive
- Low gate threshold voltage: $V_{th} = 0.7\sim 1.3\text{ V}$
- Small package

Maximum Ratings ($T_a = 25^\circ\text{C}$)

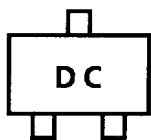
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GSS}	10	V
DC drain current	I_D	100	mA
Drain power dissipation	P_D	100	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55~150	$^\circ\text{C}$

Unit: mm

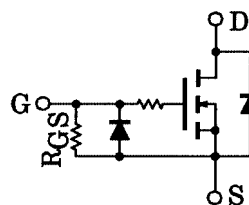


Weight: 2.3 mg (typ.)

Marking



Equivalent Circuit

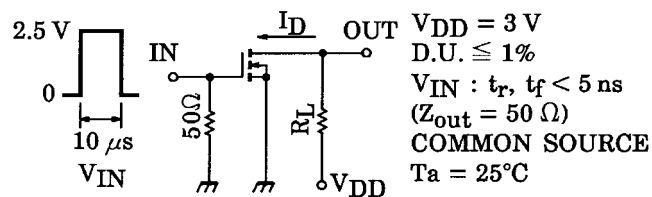


Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	I_{GSS}	$V_{GS} = 10\text{ V}, V_{DS} = 0$	—	—	15	μA	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 100\ \mu\text{A}, V_{GS} = 0$	20	—	—	V	
Drain cut-off current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0$	—	—	1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.7	—	1.3	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	25	50	—	mS	
Drain-source ON resistance	$R_{DS(ON)}$	$I_D = 10\text{ mA}, V_{GS} = 2.5\text{ V}$	—	4	12	Ω	
Input capacitance	C_{iss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	11.0	—	pF	
Reverse transfer capacitance	C_{rss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	3.3	—	pF	
Output capacitance	C_{oss}	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	9.3	—	pF	
Switching time	Turn-on time	t_{on}	$V_{DD} = 3\text{ V}, I_D = 10\text{ mA}, V_{GS} = 0\sim 2.5\text{ V}$	—	0.16	—	μs
	Turn-off time	t_{off}	$V_{DD} = 3\text{ V}, I_D = 10\text{ mA}, V_{GS} = 0\sim 2.5\text{ V}$	—	0.19	—	
Gate-source resistor	R_{GS}	$V_{GS} = 0\sim 10\text{ V}$	0.7	1.0	1.3	M Ω	

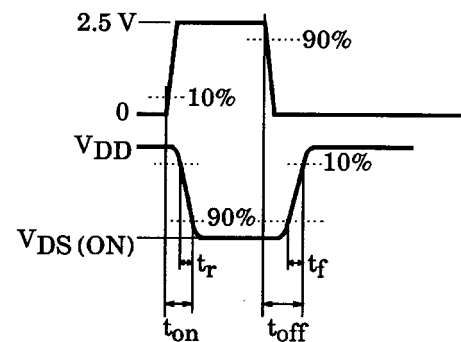
Switching Time Test Circuit

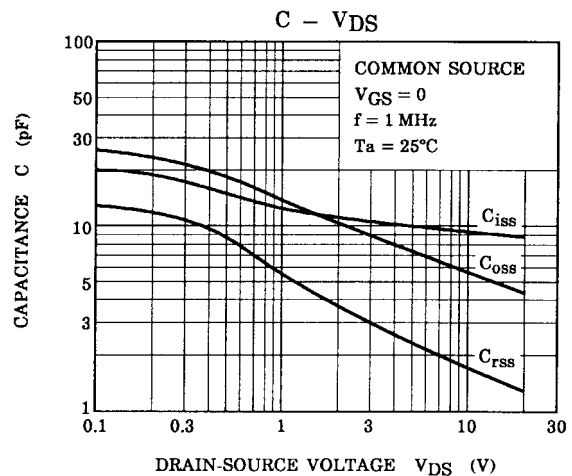
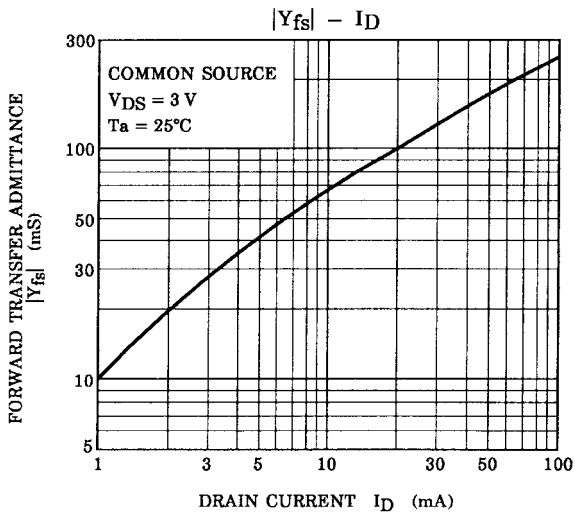
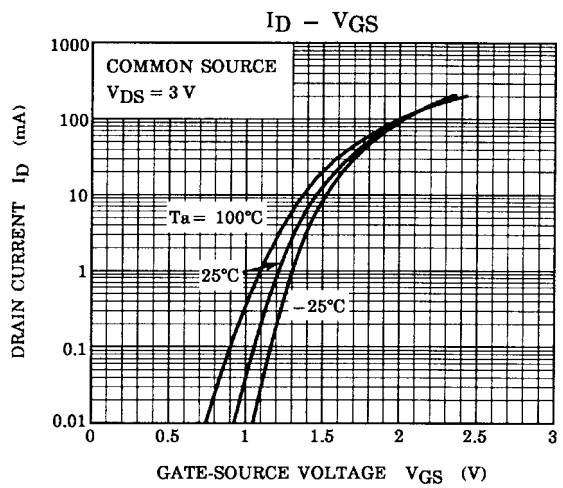
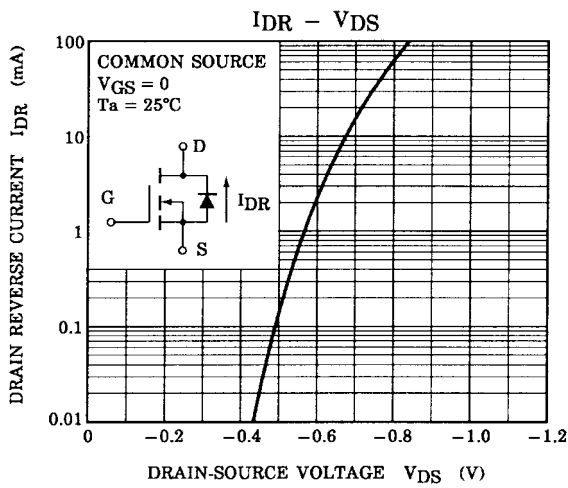
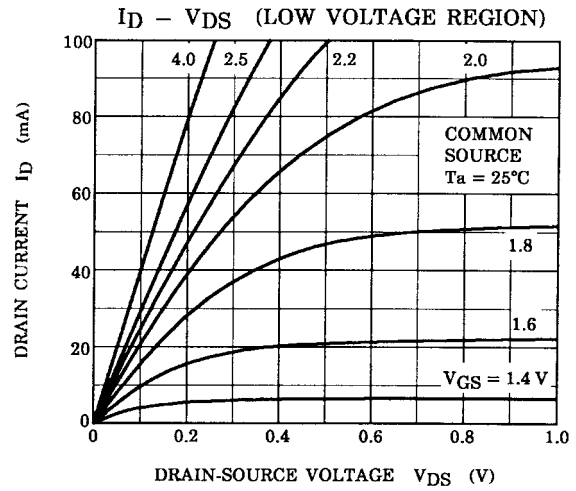
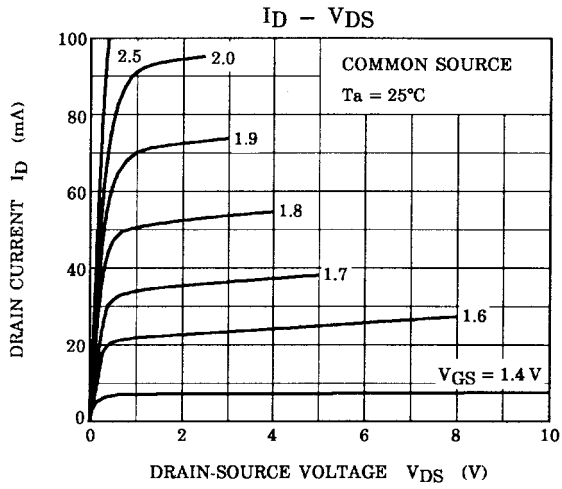
(a) Test circuit

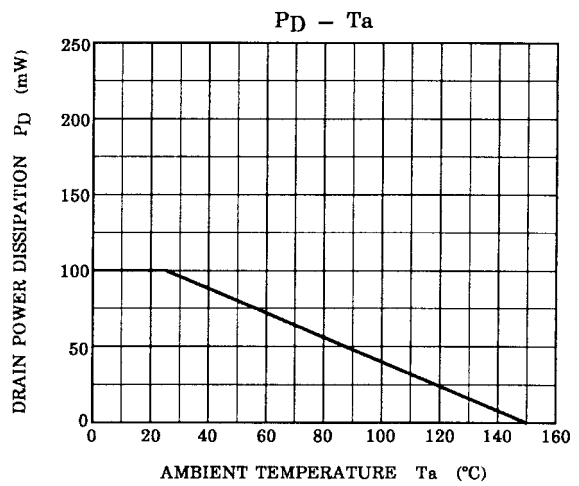
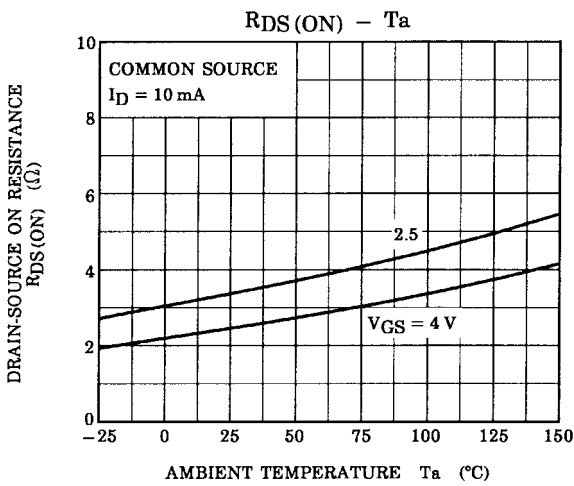
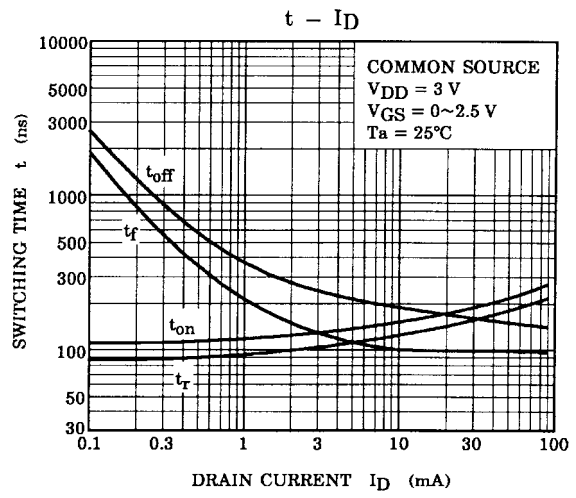
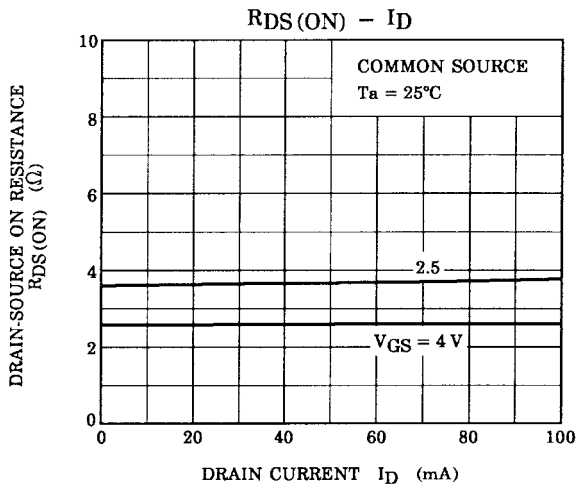


(b) V_{IN}
 V_{GS}

(c) V_{OUT}
 V_{DS}







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