Ordering number : ENN6928

CMOS IC

LC75411ES, 75411WS

Electronic Volume Controller for Car Audio Systems

Overview

The LC75411ES and 75411WS are electronic volume controllers that enable control of volume, balance, fader, bass/treble, loudness, input switching, and input gain using only a small number of external components.

Functions

- Volume: 0 dB to –79.5 dB in 0.5-dB steps, and –∞ (161 positions) Balance function with separate L/R control
- Fader: rear output or front output can be attenuated across 16 positions (in 1-dB steps from 0 dB to –2 dB, 2-dB steps from –2 dB to 20 dB, 10-dB steps from –20 dB to –30 dB, and –45 dB, –60 dB, –∞)
- Bass/treble: Both bass and treble can be controlled in 1-dB steps from 0 dB to ±6 dB, and in 2-dB steps from ±8 dB to ±12 dB.
- Input gain: 0 dB to +18.75 dB (1.25-dB steps) amplification is possible for the input signal.
- Input switching: four input signals can be selected for Left and for Right
- Loudness: A tap is output from the –32 dB position of a 2 dB step volume control resistor ladder. A loudness function can be implemented by connecting an external RC circuit.

Features

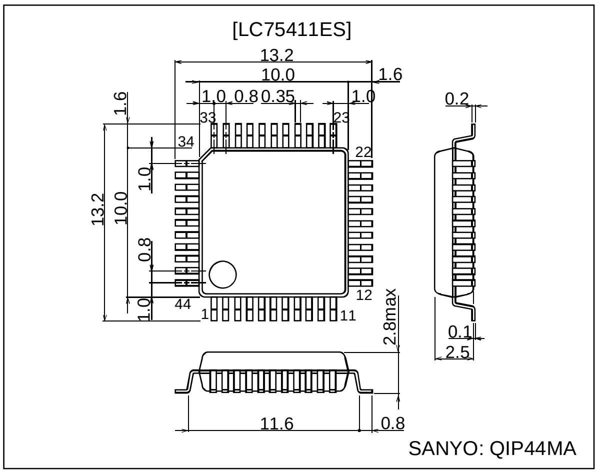
- On-chip buffer amplifier cuts down number of external components
- Low switching noise generated by on-chip switch through use of silicon gate CMOS process, for low switching noise when there is no signal
- Low switching noise when there is a signal due to use of on-chip zero-cross switching circuit
- On-chip 1/2 VDD reference voltage circuit
- Controls performed with serial input (CCB)

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

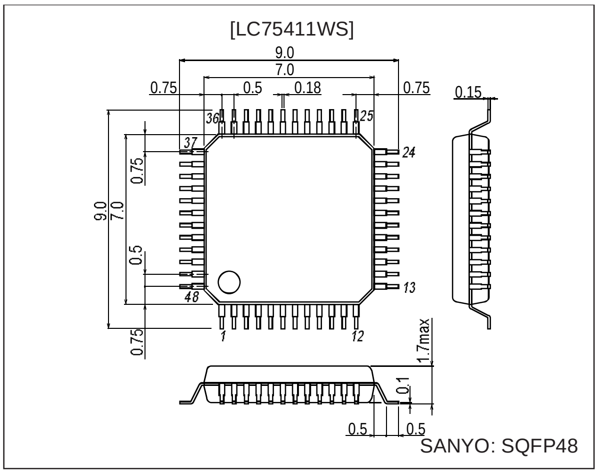
unit: mm

3148-QIP44MA



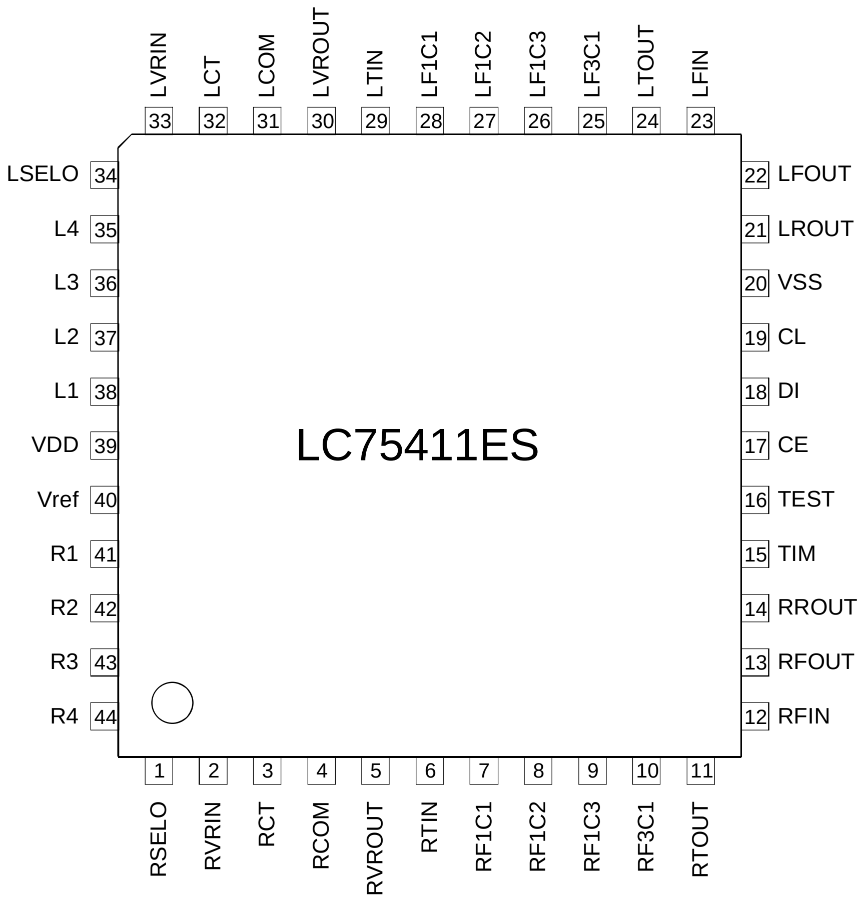
unit: mm

3163A-SQFP48



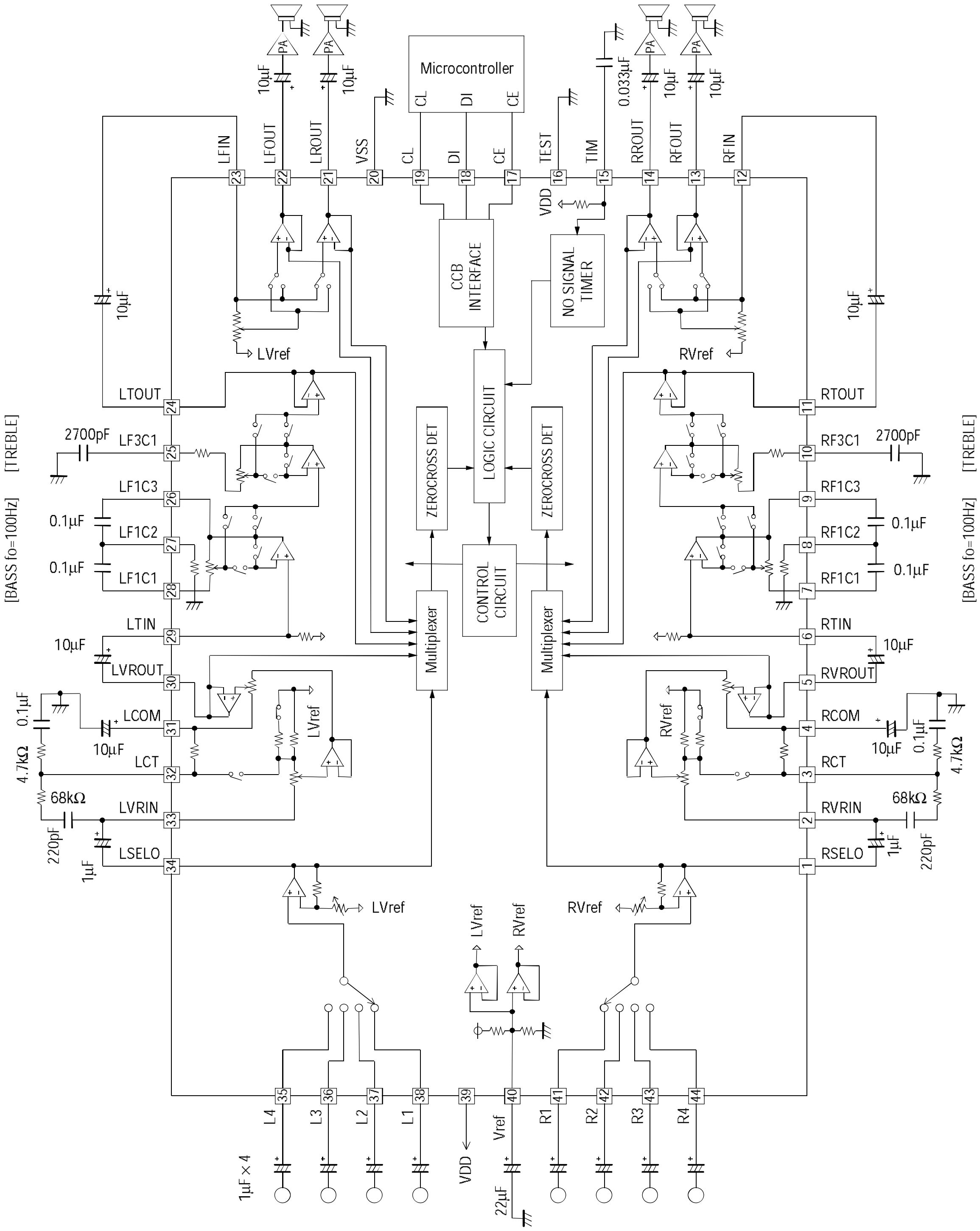
Pin Assignment

[LC75411ES]



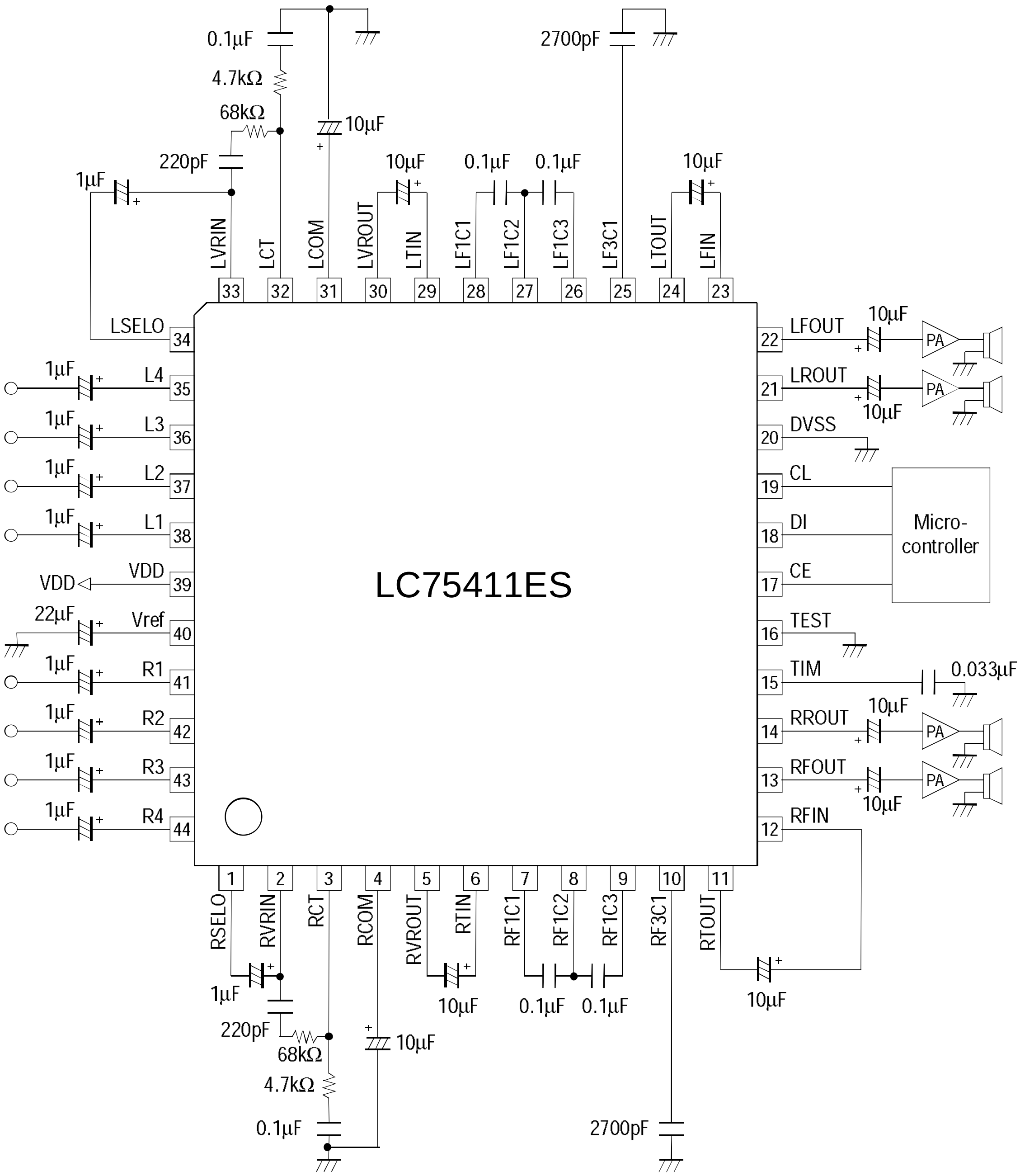
Equivalent Circuit Block Diagram

[LC75411ES]



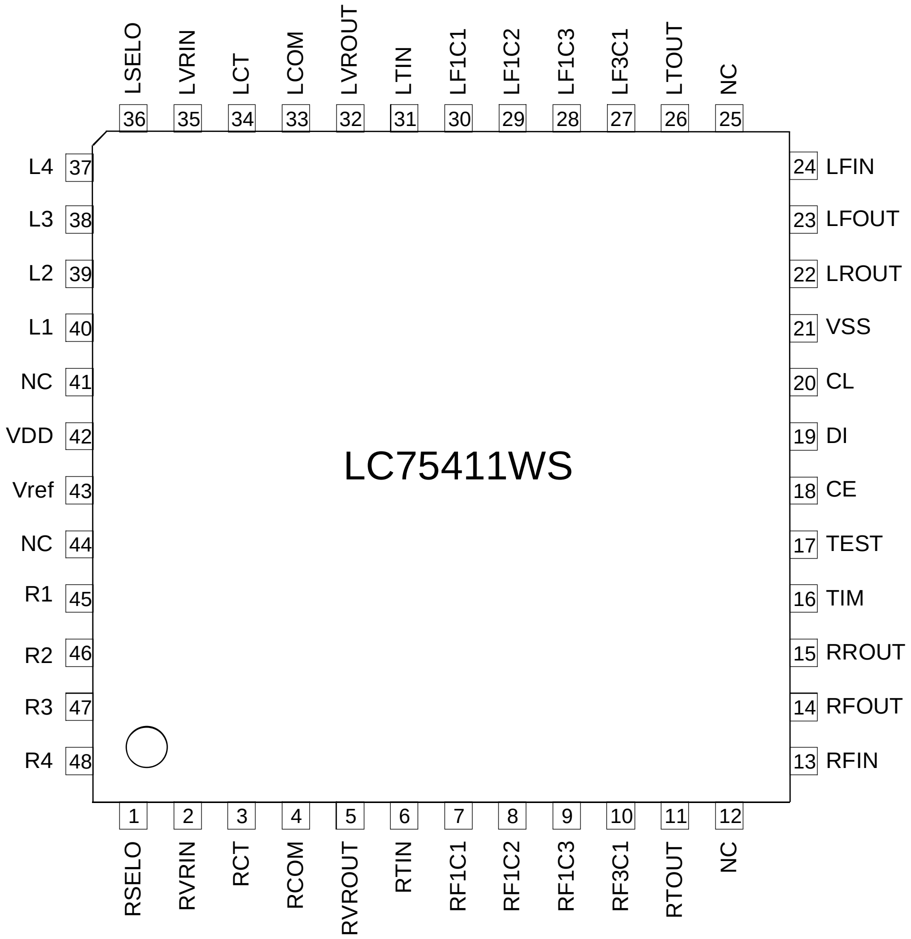
Sample Application Circuit

[LC75411ES]



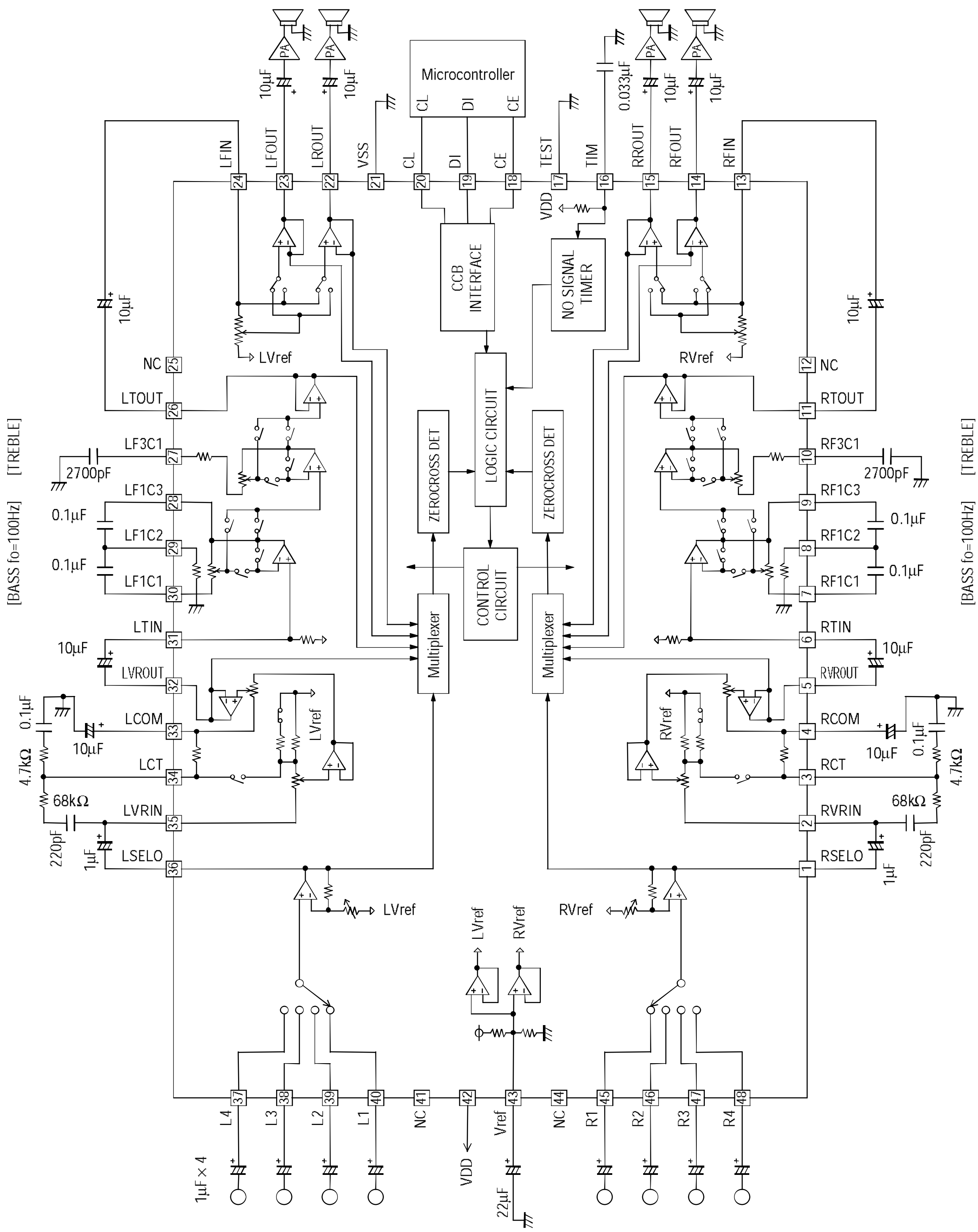
Pin Assignment

[LC75411WS]



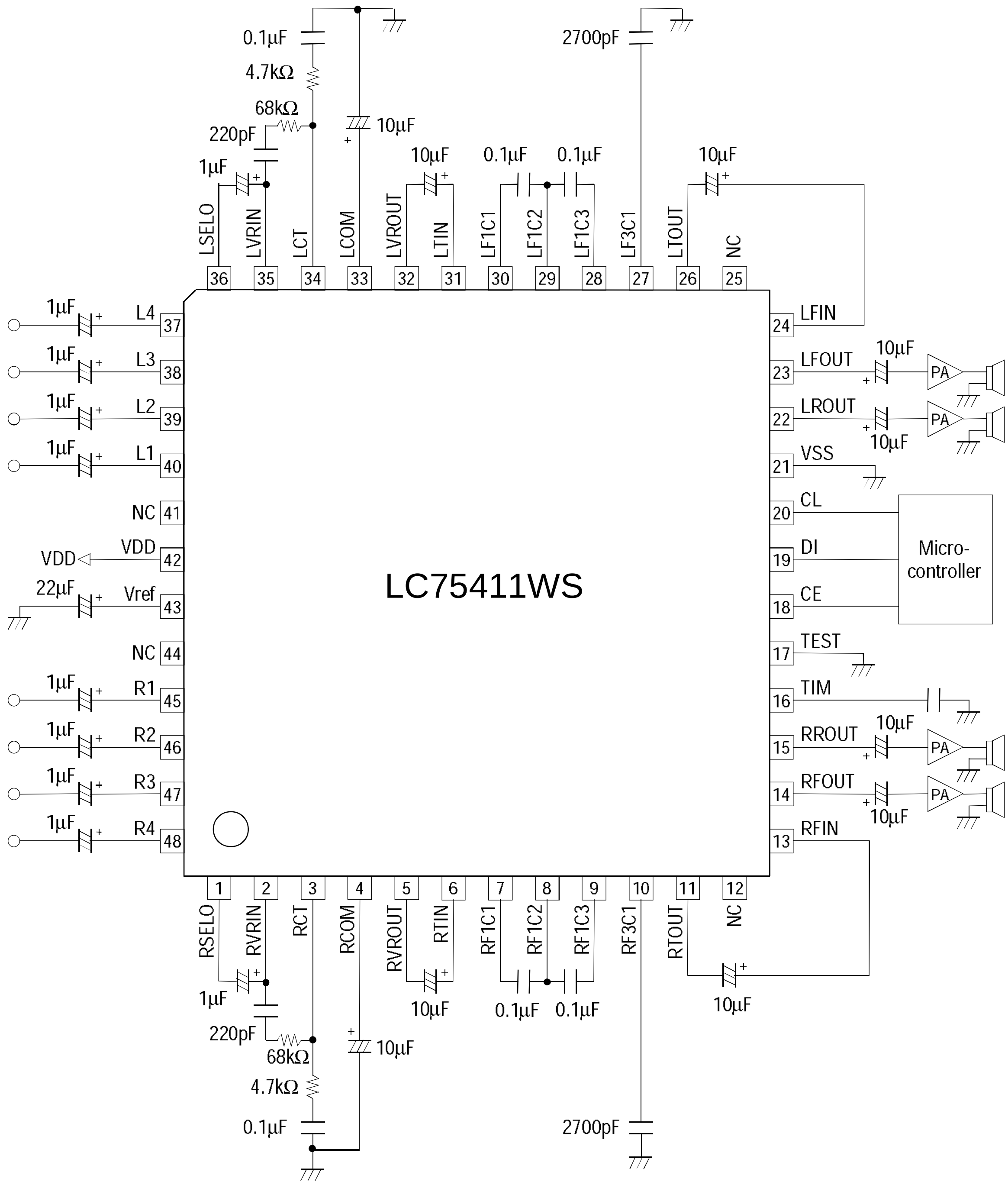
Equivalent Circuit Block Diagram

[LC75411WS]



Sample Application Circuit

[LC75411WS]



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions		Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		11	V
Maximum input voltage	V_{IN} max	All input pins		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C, when mounted on board	LC75411ES	600	mW
			LC75411WS	550	
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–50 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
Input high-level voltage	V_{IH}	CL, DI, CE, TEST	4.0		10.5	V
Input low-level voltage	V_{IL}	CL, DI, CE, TEST	V_{SS}		1.0	V
Input amplitude voltage	V_{IN}		V_{SS}		V_{DD}	Vp-p
Input pulse width	TøW	CL	1			µs
Setup time	Tsetup	CL, DI, CE	1			µs
Hold time	Thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
[Input block]							
Input resistance	Rin	L1 to L4, R1 to R4		25	50	100	kΩ
Minimum input gain	Ginmin	L1 to L4, R1 to R4		–1	0	+1	dB
Maximum input gain	Ginmax			+16.5	+18.75	+21	dB
Step setting error	ATerr					±0.5	dB
L/R balance	BAL					±0.5	dB
[Volume Block]							
Input resistance	Rvr	LVRIN, RVRIN, loudness off		113	226	452	kΩ
Step setting error	ATerr					±0.5	dB
L/R balance	BAL					±0.5	dB
[Tone block]							
Step setting error	ATerr					±1.0	dB
Bass control range	Gbass		max. boost/cut	±9	±12	±15	dB
Treble control range	Gtre		max. boost/cut	±9	±12	±15	dB
L/R balance	BAL					±0.5	dB

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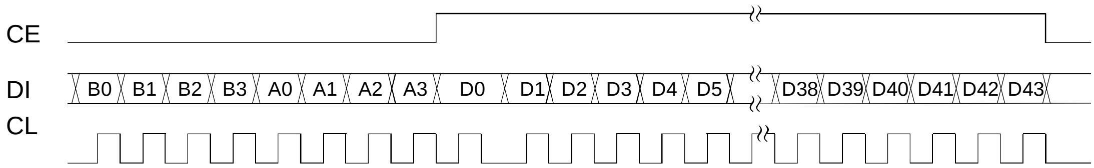
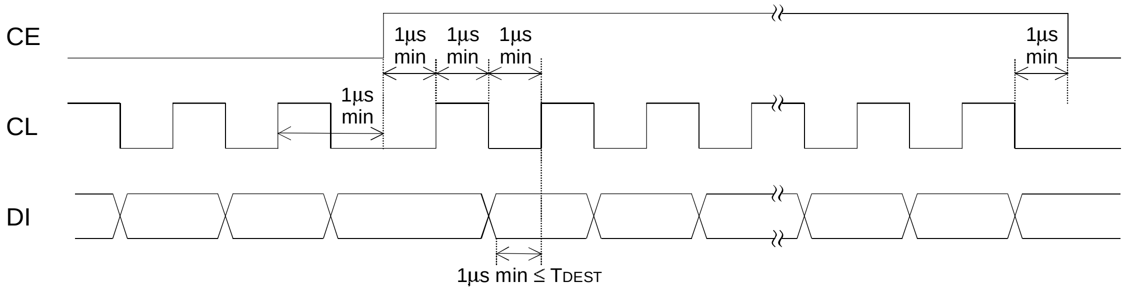
Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
[Fader Block]							
Input resistance	Rfed	LFIN, RFIN		25	50	100	kΩ
Step setting error	ATerr		0dB to –2dB			±0.5	dB
			–2dB to –20dB			±1	dB
			–20dB to –30dB			±2	dB
			–30dB to –60dB			±3	dB
L/R balance	BAL					±0.5	dB
[General]							
Total harmonic distortion	THD (1)	V_{IN} = –10dBV, f = 1 kHz			0.004	0.01	%
	THD (2)	V_{IN} = –10dBV, f = 10 kHz			0.006	0.01	%
Input crosstalk	CT	V_{IN} = 1Vrms, f = 1 kHz		80	88		dB
L/R crosstalk	CT	V_{IN} = 1Vrms, f = 1 kHz		80	88		dB
Maximum attenuated output	Vomin (1)	V_{IN} = 1Vrms, f = 1 kHz		80	88		dB
	Vomin (2)	V_{IN} = 1Vrms, f = 1 kHz INMUTE, fader –∞		90	95		dB
Output noise voltage	V_N (1)	Flat overall, IHF-A filter			5	10	μV
	V_N (2)	Flat overall, 20 to 20 kHzBPF			7	15	μV
Current drain	I_{DD}				33	40	mA
Input high-level current	I_{IH}	CL, DI, CE, V_{IN} = 9 V				10	μA
Input low-level current	I_{IL}	CL, DI, CE, V_{IN} = 0 V		–10			μA
Maximum input voltage	V_{CL}	THD = 1%, R_L = 10 kΩ flat overall, f_{IN} = 1 kHz		2.5	2.9		Vrms

Control Timing and Data Format

To control the LC75411ES and LC75411WS input specified serial data to the CE, CL, and DI pins.
The data configuration consists of a total of 52 bits broken down into 8 address bits and 44 data bits.





Address code (B0 to A3)

The LC75411ES and 75411WS use 8-bit address code and can be used in common with ICs that support SANYO's CCB serial bus.

Address Code

(LSB)

B0	B1	B2	B3	A0	A1	A2	A3
1	0	0	0	0	0	0	1

(81HEX)

Control code allocation

Input Switching Control

D0	D1	D2	Setting	Setting
0	0	0	L1 (R1)	
1	0	0	L2 (R2)	
0	1	0	L3 (R3)	
1	1	0	L4 (R4)	
0	1	1		For IC testing: Normally not used
1	1	1		

D3	Bit for IC testing: Normally set to 0

Input Gain Control

D4	D5	D6	D7	Operation
0	0	0	0	0dB
1	0	0	0	+1.25dB
0	1	0	0	+2.50dB
1	1	0	0	+3.75dB
0	0	1	0	+5.00dB
1	0	1	0	+6.25dB
0	1	1	0	+7.50dB
1	1	1	0	+8.75dB
0	0	0	1	+10.0dB
1	0	0	1	+11.25dB
0	1	0	1	+12.5dB
1	1	0	1	+13.75dB
0	0	1	1	+15.0dB
1	0	1	1	+16.25dB
0	1	1	1	+17.5dB
1	1	1	1	+18.75dB

Volume Control (0 to –20.5dB)

D8	D9	D10	D11	D12	D13	D14	D15	Operation
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	–0.5dB
1	0	0	0	0	0	0	0	–1dB
1	0	0	0	0	0	0	1	–1.5dB
0	1	0	0	0	0	0	0	–2dB
0	1	0	0	0	0	0	1	–2.5dB
1	1	0	0	0	0	0	0	–3dB
1	1	0	0	0	0	0	1	–3.5dB
0	0	1	0	0	0	0	0	–4dB
0	0	1	0	0	0	0	1	–4.5dB
1	0	1	0	0	0	0	0	–5dB
1	0	1	0	0	0	0	1	–5.5dB
0	1	1	0	0	0	0	0	–6dB
0	1	1	0	0	0	0	1	–6.5dB
1	1	1	0	0	0	0	0	–7dB
1	1	1	0	0	0	0	1	–7.5dB
0	0	0	1	0	0	0	0	–8dB
0	0	0	1	0	0	0	1	–8.5dB
1	0	0	1	0	0	0	0	–9dB
1	0	0	1	0	0	0	1	–9.5dB
0	1	0	1	0	0	0	0	–10dB
0	1	0	1	0	0	0	1	–10.5dB
1	1	0	1	0	0	0	0	–11dB
1	1	0	1	0	0	0	1	–11.5dB
0	0	1	1	0	0	0	0	–12dB
0	0	1	1	0	0	0	1	–12.5dB
1	0	1	1	0	0	0	0	–13dB
1	0	1	1	0	0	0	1	–13.5dB
0	1	1	1	0	0	0	0	–14dB
0	1	1	1	0	0	0	1	–14.5dB
1	1	1	1	0	0	0	0	–15dB
1	1	1	1	0	0	0	1	–15.5dB
0	0	0	0	1	0	0	0	–16dB
0	0	0	0	1	0	0	1	–16.5dB
1	0	0	0	1	0	0	0	–17dB
1	0	0	0	1	0	0	1	–17.5dB
0	1	0	0	1	0	0	0	–18dB
0	1	0	0	1	0	0	1	–18.5dB
1	1	0	0	1	0	0	0	–19dB
1	1	0	0	1	0	0	1	–19.5dB
0	0	1	0	1	0	0	0	–20dB
0	0	1	0	1	0	0	1	–20.5dB

Volume Control (–21 to –40.5dB)

D8	D9	D10	D11	D12	D13	D14	D15	Operation
1	0	1	0	1	0	0	0	–21dB
1	0	1	0	1	0	0	1	–21.5dB
0	1	1	0	1	0	0	0	–22dB
0	1	1	0	1	0	0	1	–22.5dB
1	1	1	0	1	0	0	0	–23dB
1	1	1	0	1	0	0	1	–23.5dB
0	0	0	1	1	0	0	0	–24dB
0	0	0	1	1	0	0	1	–24.5dB
1	0	0	1	1	0	0	0	–25dB
1	0	0	1	1	0	0	1	–25.5dB
0	1	0	1	1	0	0	0	–26dB
0	1	0	1	1	0	0	1	–26.5dB
1	1	0	1	1	0	0	0	–27dB
1	1	0	1	1	0	0	1	–27.5dB
0	0	1	1	1	0	0	0	–28dB
0	0	1	1	1	0	0	1	–28.5dB
1	0	1	1	1	0	0	0	–29dB
1	0	1	1	1	0	0	1	–29.5dB
0	1	1	1	1	0	0	0	–30dB
0	1	1	1	1	0	0	1	–30.5dB
1	1	1	1	1	0	0	0	–31dB
1	1	1	1	1	0	0	1	–31.5dB
0	0	0	0	0	1	0	0	–32dB
0	0	0	0	0	1	0	1	–32.5dB
1	0	0	0	0	1	0	0	–33dB
1	0	0	0	0	1	0	1	–33.5dB
0	1	0	0	0	1	0	0	–34dB
0	1	0	0	0	1	0	1	–34.5dB
1	1	0	0	0	1	0	0	–35dB
1	1	0	0	0	1	0	1	–35.5dB
0	0	1	0	0	1	0	0	–36dB
0	0	1	0	0	1	0	1	–36.5dB
1	0	1	0	0	1	0	0	–37dB
1	0	1	0	0	1	0	1	–37.5dB
0	1	1	0	0	1	0	0	–38dB
0	1	1	0	0	1	0	1	–38.5dB
1	1	1	0	0	1	0	0	–39dB
1	1	1	0	0	1	0	1	–39.5dB
0	0	0	1	0	1	0	0	–40dB
0	0	0	1	0	1	0	1	–40.5dB

Volume Control (–41 to –59.5dB)

D8	D9	D10	D11	D12	D13	D14	D15	Operation
1	0	0	1	0	1	0	0	–41dB
1	0	0	1	0	1	0	1	–41.5dB
0	1	0	1	0	1	0	0	–42dB
0	1	0	1	0	1	0	1	–42.5dB
1	1	0	1	0	1	0	0	–43dB
1	1	0	1	0	1	0	1	–43.5dB
0	0	1	1	0	1	0	0	–44dB
0	0	1	1	0	1	0	1	–44.5dB
1	0	1	1	0	1	0	0	–45dB
1	0	1	1	0	1	0	1	–45.5dB
0	1	1	1	0	1	0	0	–46dB
0	1	1	1	0	1	0	1	–46.5dB
1	1	1	1	0	1	0	0	–47dB
1	1	1	1	0	1	0	1	–47.5dB
0	0	0	0	1	1	0	0	–48dB
0	0	0	0	1	1	0	1	–48.5dB
1	0	0	0	1	1	0	0	–49dB
1	0	0	0	1	1	0	1	–49.5dB
0	1	0	0	1	1	0	0	–50dB
0	1	0	0	1	1	0	1	–50.5dB
1	1	0	0	1	1	0	0	–51dB
1	1	0	0	1	1	0	1	–51.5dB
0	0	1	0	1	1	0	0	–52dB
0	0	1	0	1	1	0	1	–52.5dB
1	0	1	0	1	1	0	0	–53dB
1	0	1	0	1	1	0	1	–53.5dB
0	1	1	0	1	1	0	0	–54dB
0	1	1	0	1	1	0	1	–54.5dB
1	1	1	0	1	1	0	0	–55dB
1	1	1	0	1	1	0	1	–55.5dB
0	0	0	1	1	1	0	0	–56dB
0	0	0	1	1	1	0	1	–56.5dB
1	0	0	1	1	1	0	0	–57dB
1	0	0	1	1	1	0	1	–57.5dB
0	1	0	1	1	1	0	0	–58dB
0	1	0	1	1	1	0	1	–58.5dB
1	1	0	1	1	1	0	0	–59dB
1	1	0	1	1	1	0	1	–59.5dB

Volume Control (–60 to –∞)

D8	D9	D10	D11	D12	D13	D14	D15	Operation
0	0	1	1	1	1	0	0	–60dB
0	0	1	1	1	1	0	1	–60.5dB
1	0	1	1	1	1	0	0	–61dB
1	0	1	1	1	1	0	1	–61.5dB
0	1	1	1	1	1	0	0	–62dB
0	1	1	1	1	1	0	1	–62.5dB
1	1	1	1	1	1	0	0	–63dB
1	1	1	1	1	1	0	1	–63.5dB
0	0	0	0	0	0	1	0	–64dB
0	0	0	0	0	0	1	1	–64.5dB
1	0	0	0	0	0	1	0	–65dB
1	0	0	0	0	0	1	1	–65.5dB
0	1	0	0	0	0	1	0	–66dB
0	1	0	0	0	0	1	1	–66.5dB
1	1	0	0	0	0	1	0	–67dB
1	1	0	0	0	0	1	1	–67.5dB
0	0	1	0	0	0	1	0	–68dB
0	0	1	0	0	0	1	1	–68.5dB
1	0	1	0	0	0	1	0	–69dB
1	0	1	0	0	0	1	1	–69.5dB
0	1	1	0	0	0	1	0	–70dB
0	1	1	0	0	0	1	1	–70.5dB
1	1	1	0	0	0	1	0	–71dB
1	1	1	0	0	0	1	1	–71.5dB
0	0	0	1	0	0	1	0	–72dB
0	0	0	1	0	0	1	1	–72.5dB
1	0	0	1	0	0	1	0	–73dB
1	0	0	1	0	0	1	1	–73.5dB
0	1	0	1	0	0	1	0	–74dB
0	1	0	1	0	0	1	1	–74.5dB
1	1	0	1	0	0	1	0	–75dB
1	1	0	1	0	0	1	1	–75.5dB
0	0	1	1	0	0	1	0	–76dB
0	0	1	1	0	0	1	1	–76.5dB
1	0	1	1	0	0	1	0	–77dB
1	0	1	1	0	0	1	1	–77.5dB
0	1	1	1	0	0	1	0	–78dB
0	1	1	1	0	0	1	1	–78.5dB
1	1	1	1	0	0	1	0	–79dB
1	1	1	1	0	0	1	1	–79.5dB
0	1	1	1	1	1	1	0	–∞

Tone Control

D16	D17	D18	D19	D40	Bass
D24	D25	D26	D27	D42	Treble
0	1	1	0	0	+12dB
1	0	1	0	0	+10dB
0	0	1	0	0	+8dB
1	1	0	0	0	+6dB
1	1	0	0	1	+5dB
0	1	0	0	0	+4dB
0	1	0	0	1	+3dB
1	0	0	0	0	+2dB
1	0	0	0	1	+1dB
0	0	0	0	0	0dB
1	0	0	1	1	–1dB
1	0	0	1	0	–2dB
0	1	0	1	1	–3dB
0	1	0	1	0	–4dB
1	1	0	1	1	–5dB
1	1	0	1	0	–6dB
0	0	1	1	0	–8dB
1	0	1	1	0	–10dB
0	1	1	1	0	–12dB

D20	D21	D22	D23	D41	Setting
0	0	0	0	0	Set to 0

Fader Volume Control

D28	D29	D30	D31	Operation
0	0	0	0	0dB
1	0	0	0	–1dB
0	1	0	0	–2dB
1	1	0	0	–4dB
0	0	1	0	–6dB
1	0	1	0	–8dB
0	1	1	0	–10dB
1	1	1	0	–12dB
0	0	0	1	–14dB
1	0	0	1	–16dB
0	1	0	1	–18dB
1	1	0	1	–20dB
0	0	1	1	–30dB
1	0	1	1	–45dB
0	1	1	1	–60dB
1	1	1	1	–∞

Channel Selection Control

D32	D33	Operation
0	0	Initial setting mode: Rapid charging
1	0	RCH
0	1	LCH
1	1	L/R simultaneously

Fader Rear/Front Control

D34	Setting
0	Rear
1	Front

Loudness Control

D35	Setting
0	OFF
1	ON

Zero-Cross Control

D36	D37	Setting
0	0	Data write through zero-cross detection
1	1	Zero-cross detection stopped (data write at falling edge of CE)

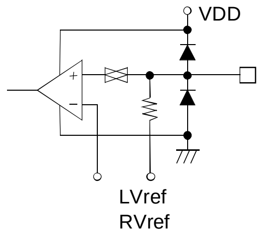
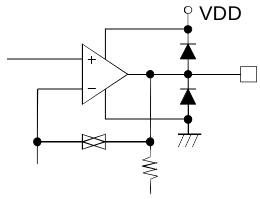
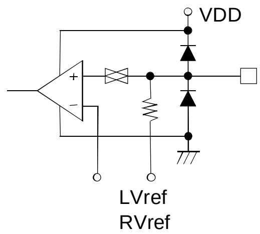
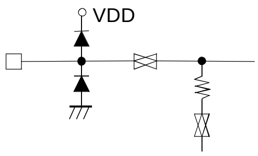
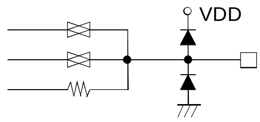
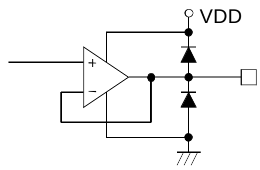
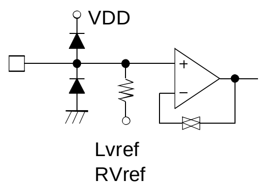
Zero-Cross Signal Detection Block Control

D38	D39	Setting
0	0	Selector
1	0	Volume
0	1	Tone
1	1	Fader

Test Mode Control

D43	Setting
0	For IC testing. Always set to 0.

Pin Functions

Pin Name	Pin No.		Function	Equivalent circuit
	LC75411ES	LC75411WS		
L1 L2 L3 L4 R1 R2 R3 R4	38 37 36 35 41 42 43 44	40 39 38 37 45 46 47 48	• Single-end input pin	
LSEL0 RSEL0	34 1	36 1	• Input selector output pins	
LVRIN RVRIN	33 2	35 2	• 2-dB step volume input pins • Perform input at low-impedance.	
LCT RCT	32 3	34 3	• Loudness pins. Connect high-pass compensation RC between LCT (RCT) and LVRIN (RVRIN), and connect low-pass compensation RC between LCT (RCT) and GND.	
LCOM RCOM	31 4	33 4	• 2-dB stop volume output pins. • Connect these pins to GND through coupling capacitors to reduce switching noise.	
LVROUT RVROUT	30 5	32 5	• 0.5-dB step volume output pin	
LTIN RTIN	29 6	31 6	• Equalizer input pin	

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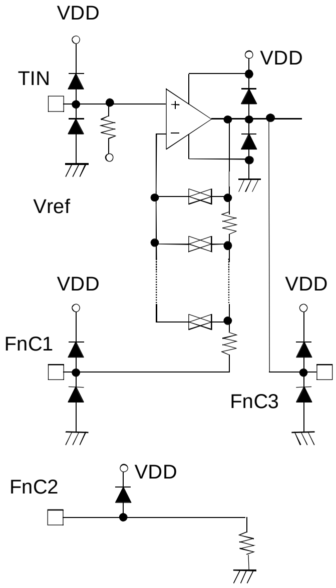
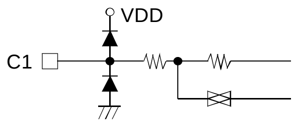
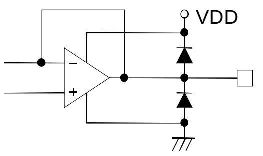
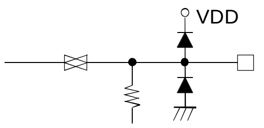
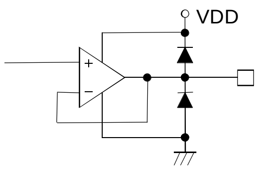
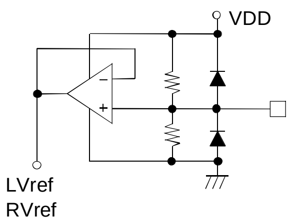
Pin Name	Pin No.		Function	Equivalent circuit
	LC75411ES	LC75411WS		
LF1C1 LF1C2 LF1C3 RF1C1 RF1C2 RF1C3	28 27 26 7 8 9	30 29 28 7 8 9	• Equalizer F1 band filter configuration capacitor connection pins. Connect capacitor between LF1C1 (RF1C1) and LF1C2 (RF1C2) LF1C2 (RF1C2) and LF1C3 (RF1C3)	
LF3C1 RF3C1	25 10	27 10	• Equalizer F3 band circuit filter configuration capacitor connection pins. Connect high-pass compensation capacitor between LF3C1 (RF3C1) and VSS.	
LTOUT RTOUT	24 11	26 11	• Equalizer output pins	
LFIN RFIN	23 12	24 13	• Fader block input pins • Drive at low impedance.	
LFOUT LROUT RFOUT RROUT	22 21 13 14	23 22 14 15	• Fader output pins. Attenuation is possible separately for the front end and rear end. The attenuation amount is the same for L and R.	
Vref	40	43	• Connect a capacitor of a few tens of μF between Vref and VSS as a 0.55 VDD voltage generator, current ripple countermeasure.	

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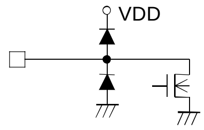
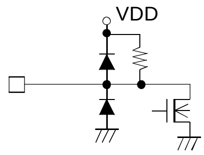
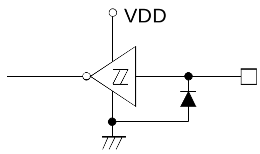
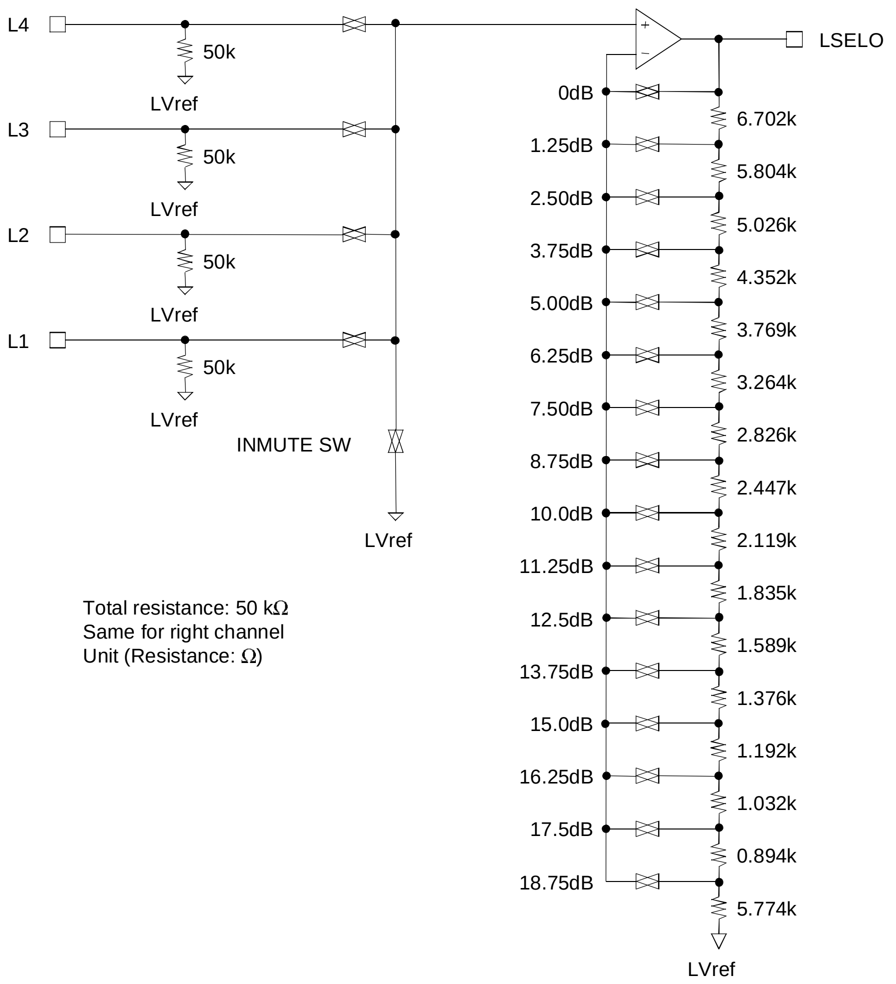
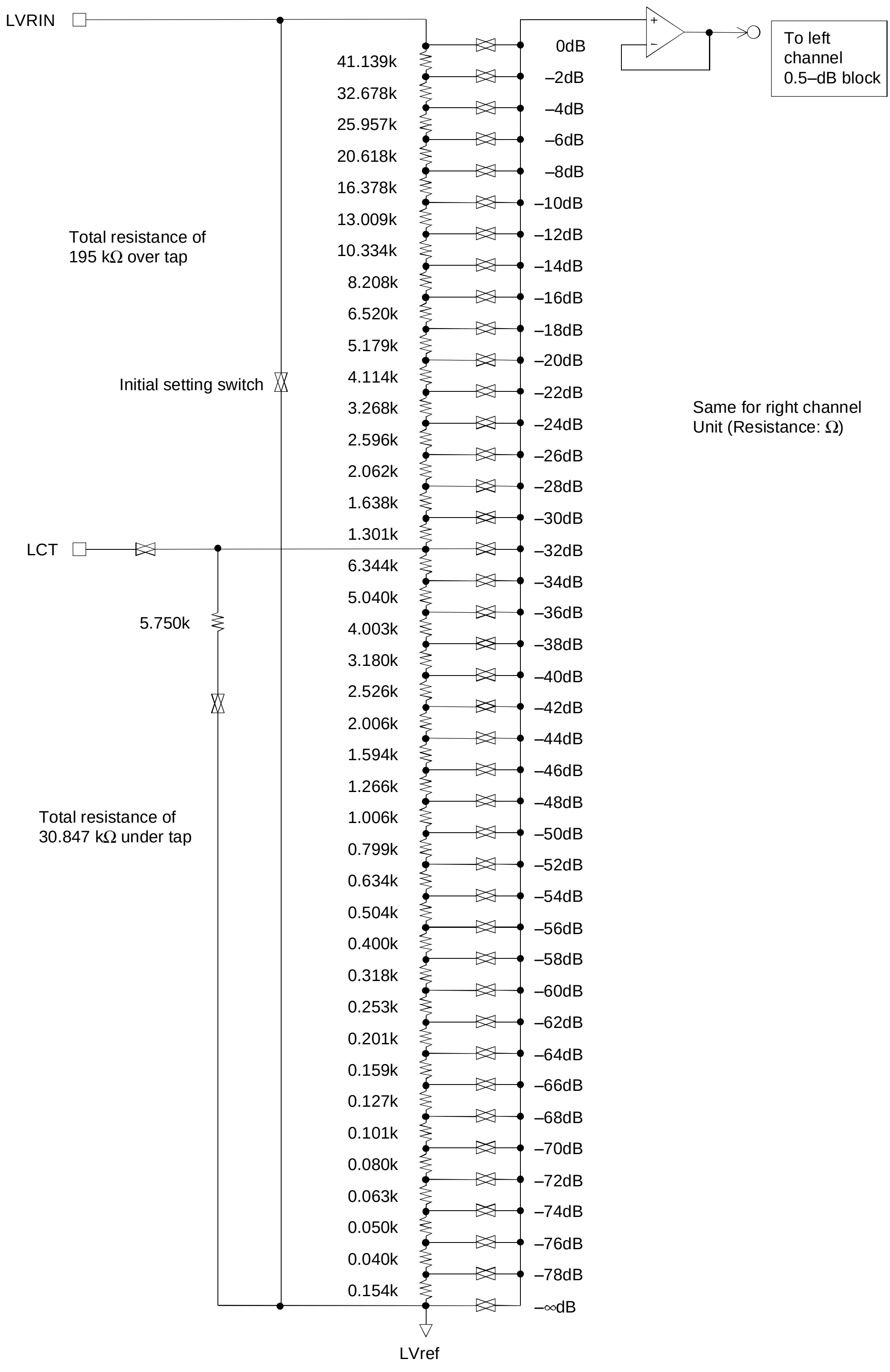
Pin Name	Pin No.		Function	Equivalent circuit
	LC75411ES	LC75411WS		
VDD	39	42	• Power supply pin	
VSS	20	21	• Ground pin	
TEST	16	17	• Dedicated IC test pin • Normally this pin is used connected to GND.	
TIM	15	16	• Timer pin when there is no signal in the zero-cross circuit. Forcibly set data when there is no zero-cross signal, from the time the data is set until the timer ends.	
CL DI	19 18	20 19	• Input pin for serial data and clock used for control	
CE	17	18	• Chip enable pin. Data is written to the internal latch and the analog switches are operated when the level changes from High to Low. Data transfer is enabled when the level is High.	
NC	—	12 25 41 44	• No Connect pin. Leave this pin open or connect it to V_{SS}.	

Internal Equivalent Circuit Block Diagram

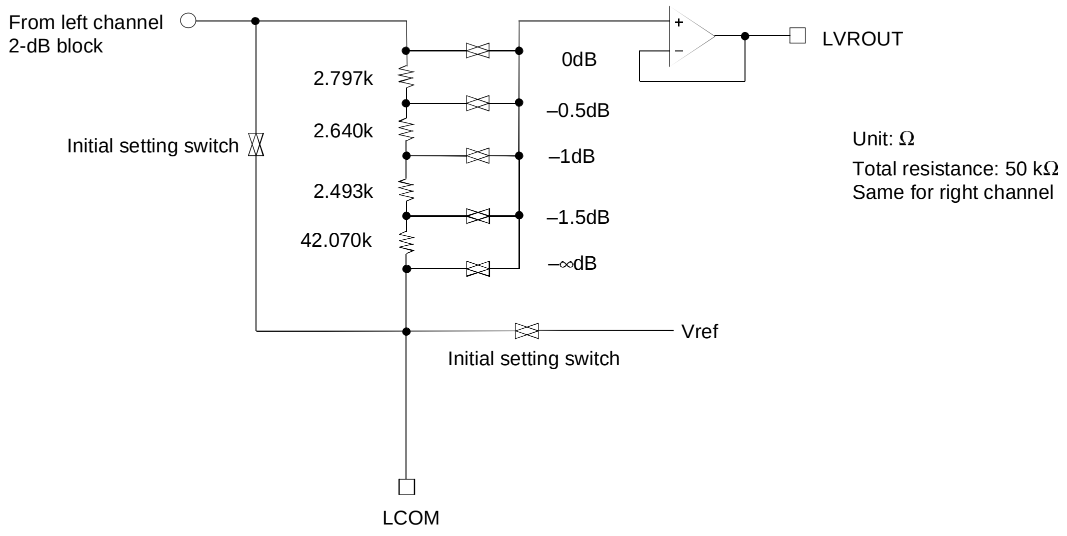
Selector Block Equivalent Circuit Block Diagram



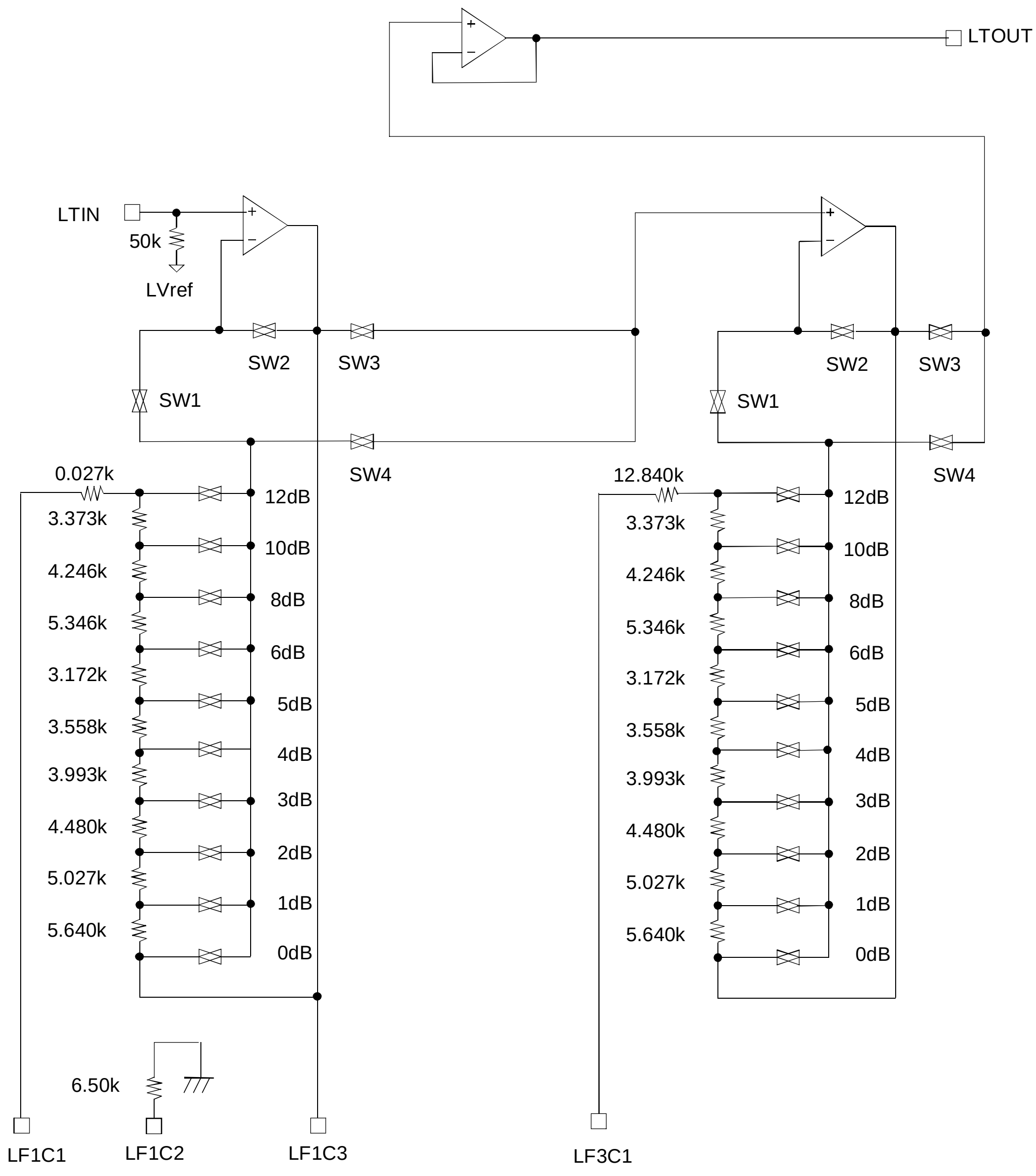
2-dB Volume Block Equivalent Circuit Block Diagram



0.5-dB Volume Block Equivalent Circuit Block Diagram



Tone Block Equivalent Circuit Diagram



Unit: Ω
Total resistance: 38.861 kΩ
Same for right channel

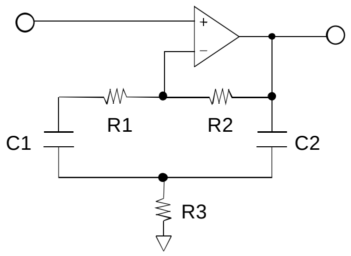
During boost, SW 1 and SW 3 are ON, during cut SW 2 and SW 4 are ON,
and when 0 dB, 0 dB SW and SW 2 and SW 3 are ON.

Tone Circuit Constant Calculation Example

Bass Band Circuit

The equivalent circuit and the formula for calculating the external RC with a mean frequency of 100 Hz are shown below.

• Bass band equivalent circuit block diagram



• Calculation example

Specification Mean frequency: f0 = 100 Hz

Gain during maximum boost: G = 12 dB

Let us use R1 = 0, R2 = 38.861 kΩ, R3 = 6.5 kΩ (assuming R1 = 0 during maximum boost) , and C1 = C2 = C.

1. We obtain C from mean frequency f0 = 100 Hz, as follows.

$$f0 = \frac{1}{2\pi\sqrt{R3R2C1C2}}$$

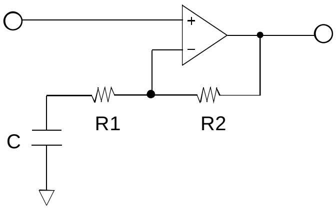
$$C = \frac{1}{2\pi \mathrm{f0}\sqrt{\mathrm{R3R2}}} = \frac{1}{2\pi \times 100\sqrt{38861 \times 6500}} \cong 0.1\mu\mathrm{F}$$

2. We obtain Q as follows.

$$\mathrm{Q} = \frac{\mathrm{R3R2}}{2\ \mathrm{R3}} \times \frac{1}{\sqrt{\mathrm{R3R2}}} \cong 1.223$$

Treble Band Circuit

The shelving characteristics for the treble band can be obtained.
The equivalent circuit and the calculation formula during boost are shown below.



• Calculation example

Specification Setting frequency: f = 26000 Hz

Gain during maximum boost: G = 12 dB

Let us use R1 = 12.840 kΩ and R2 = 38.861 kΩ

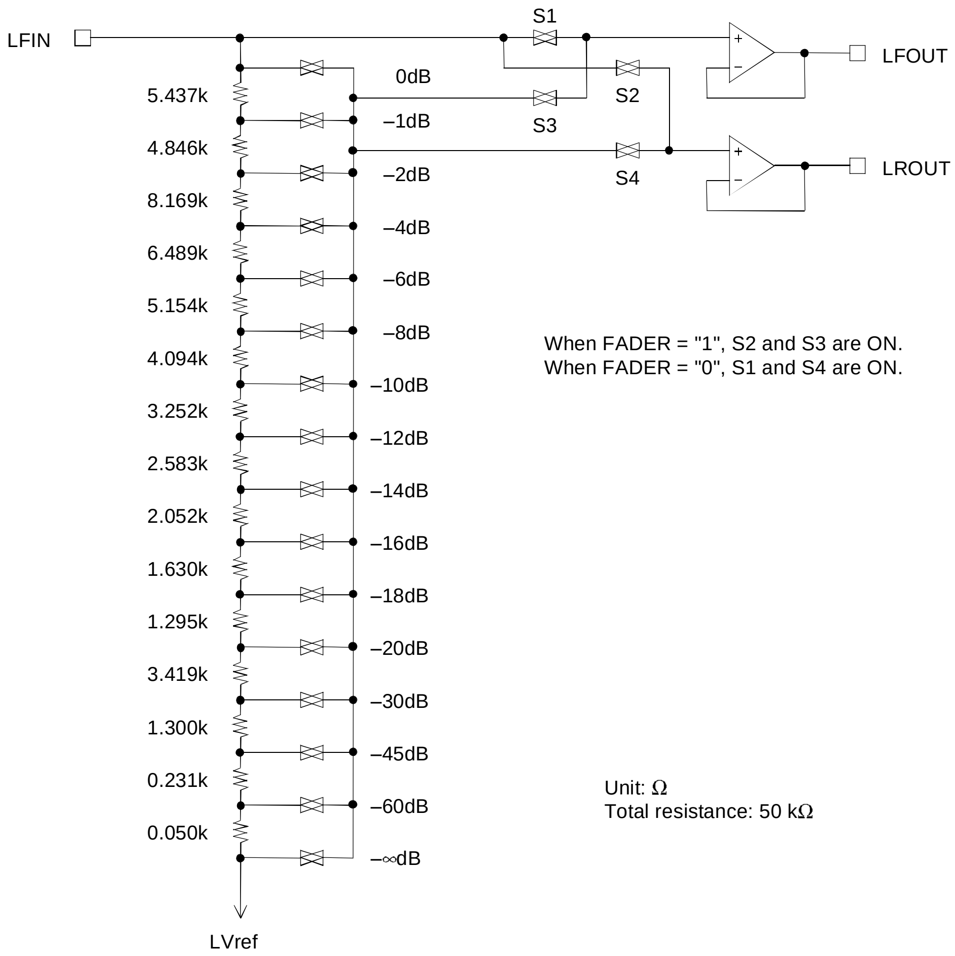
The above constants are inserted in the following formula.

$$G = 20 \times LOG_{10}\left(1 + \frac{R2}{\sqrt{R1^2 + (1/\omega C)^2}}\right)$$

$$C = \frac{1}{2\pi f\sqrt{(\frac{R2}{10^{G/20}-1})^2 - R1^2}}$$

$$= \frac{1}{2\pi \times 26000\sqrt{\left(\frac{38861}{3.981-1}\right)^2 - 12840^2}} \cong 2700(pF)$$

Fader Volume Block Equivalent Circuit Block Diagram



When FADER = "1", S2 and S3 are ON.
When FADER = "0", S1 and S4 are ON.

Unit: Ω
Total resistance: 50 kΩ

When –∞ data is sent to the main volume 0.5dBSTEP, S1 and S2 become open, and S3 and S4 simultaneously become ON.

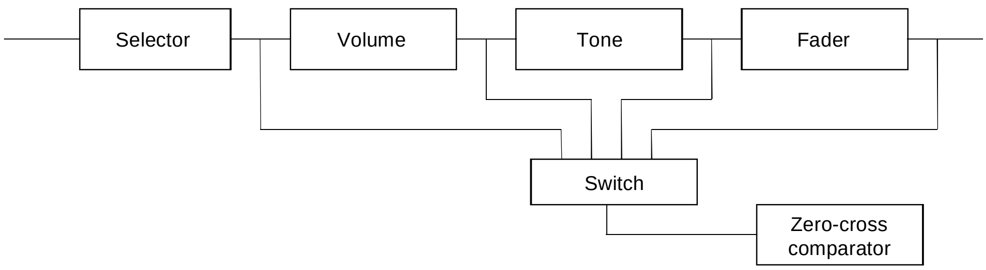
Usage Cautions

(1) Data transmission at power ON

- The status of internal analog switches is unstable at power ON. Therefore, perform muting or some other countermeasure until the data has been set.
- At power ON, initial setting data must be sent once in order to stabilize the bias of each block in a short time.

(2) Description of zero-cross switching circuit operation

The LC75411ES and 75411WS have a function to switch zero-cross comparator signal detection locations, enabling the selection of the optimum detection location for blocks whose data is to be updated. Basically, the switching noise can be minimized by inputting the signal immediately following the block whose data is to be updated to the zero-cross comparator, so it is necessary to switch the detection location every time.



LC75411ES, 75411WS Zero-Cross Detection Circuit

(3) Zero-cross switching control method

The zero-cross switching control method consists of setting the zero-cross control bits to the zero-cross detection mode (D36, D37 = 0), and specifying the detection blocks (D38, D39) before transmitting the data. These control bits are latched immediately following data transfer, that is to say beforehand in sync with the falling edge of CE, so when updating data of volumes, etc., it is possible to perform mode setting and zero-cross switching with one data transfer. An example of control when updating the data of the volume block is shown below.

D36	D37	D38	D39
0	0	1	0

$\underbrace{\text{D36, D37}}_{\text{Zero-cross detection mode setting}}$ $\underbrace{\text{D38, D39}}_{\text{Volume block setting}}$

(4) Zero-cross timer setting

If the input signal becomes lower than the zero-cross comparator detection sensitivity, or if only low-frequency signals are input, zero-cross detection continues to be impossible, and data is not latched during this time.

The zero-cross timer can set a time for forcible latch during such a status when zero-cross detection is not possible.

For example, to set 25 ms,
using T = 0.69CR and C = 0.033 μF,
we obtain

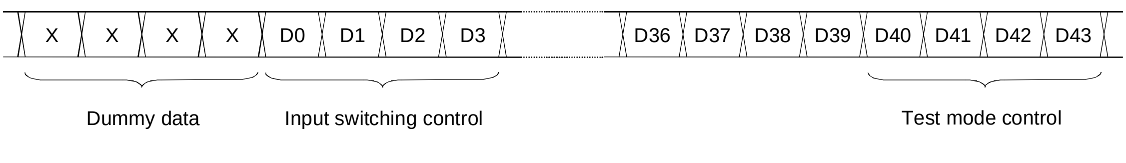
$$R = \frac{25 \times 10^{-3}}{0.69 \times 0.033 \times 10^{-6}} \fallingdotseq 1.1\ \mathrm{M\Omega}$$

Normally, a value between 10 ms and 50 ms is set.

(5) Cautions related to serial data transfer

1. To ensure that the high-frequency digital signals transferred to the CL, DI, and CE pins do not spill over to the analog signal block, either guard these signal lines with a ground pattern, or perform transmission using shielded wires.
2. The data format of the LC75411ES and 75411WS uses 8-bit addresses and 44-bit data. When sending data using multiples of 8 (when sending 48 bits), use the method described in Figure 1.

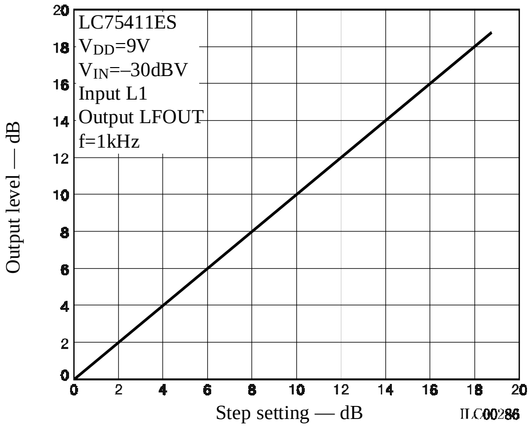
   Method for Receiving Data Using Multiple of 8 of LC75411ES and 75411WS

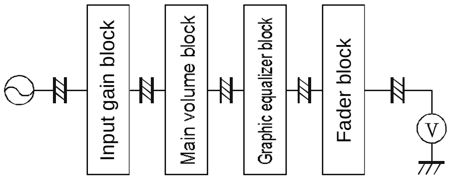


X : don't care

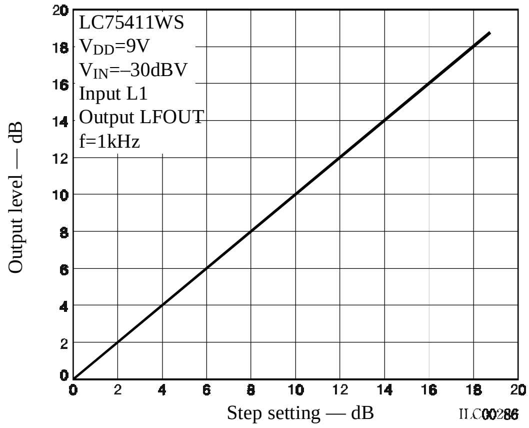
Figure 1

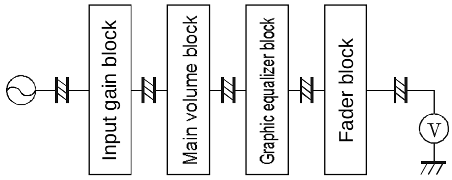
Gain Step Characteristics



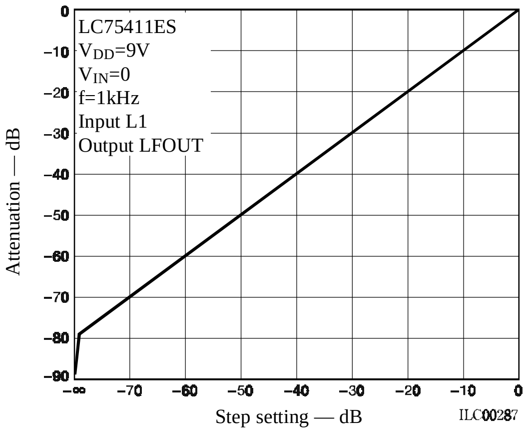


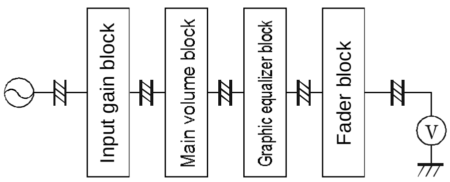
Gain Step Characteristics



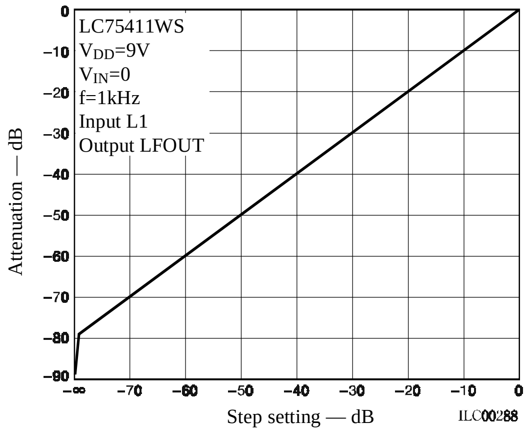


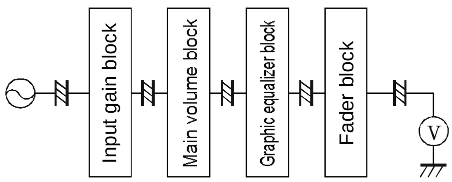
Main Volume Control Step Characteristics



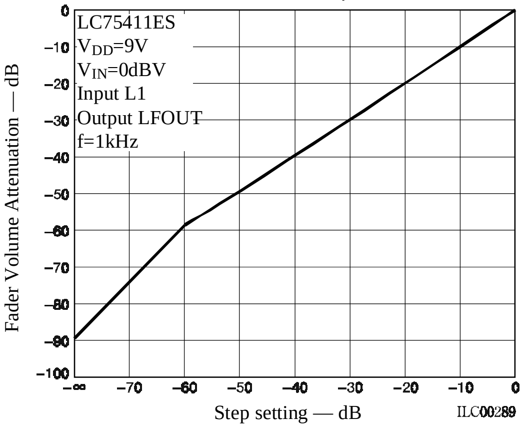


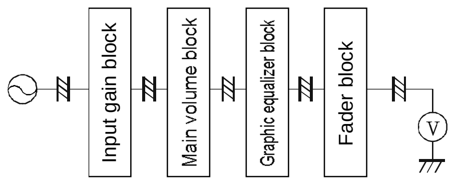
Main Volume Control Step Characteristics



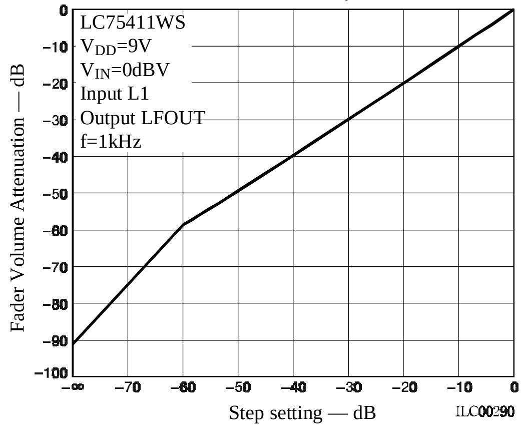


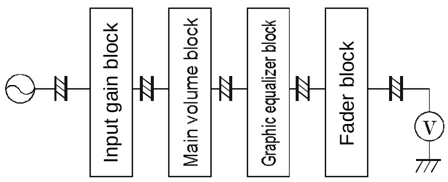
Fader Volume Control Step Characteristics



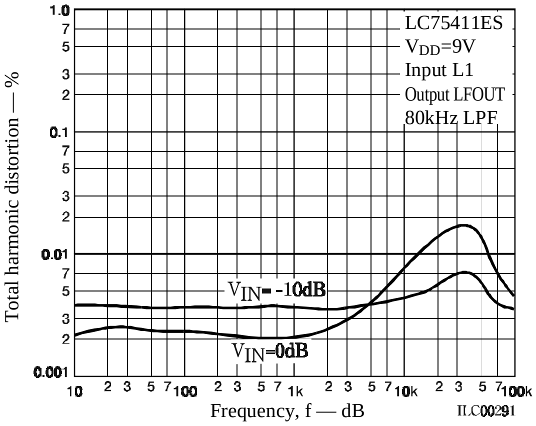


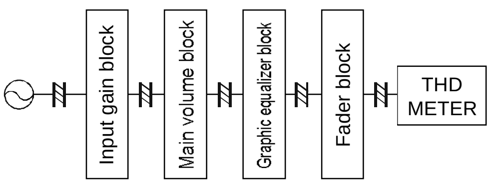
Fader Volume Control Step Characteristics



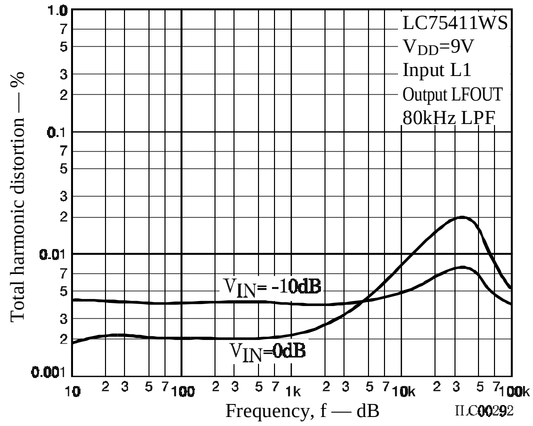


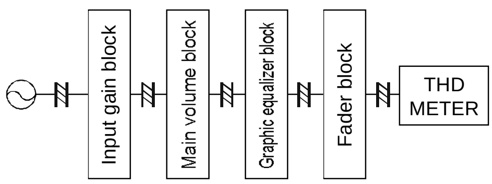
THD — Frequency Characteristics



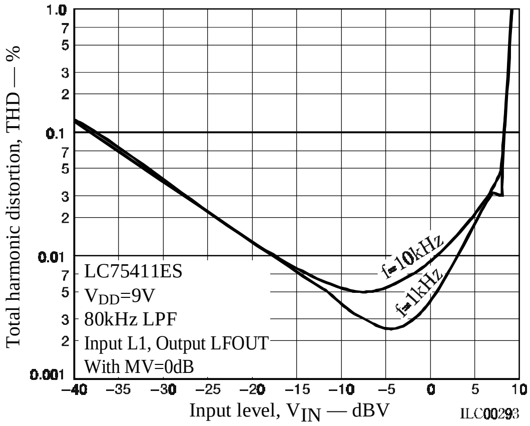


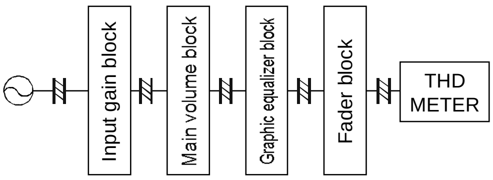
THD — Frequency Characteristics



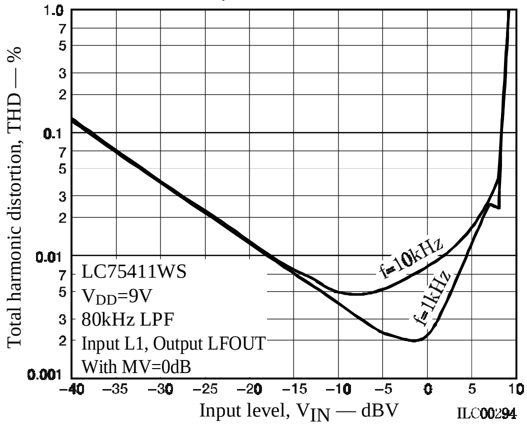


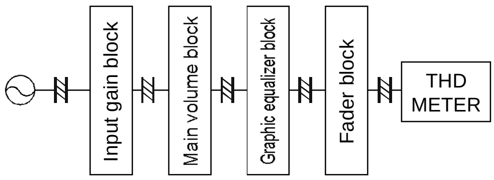
THD — Input Level Characteristics



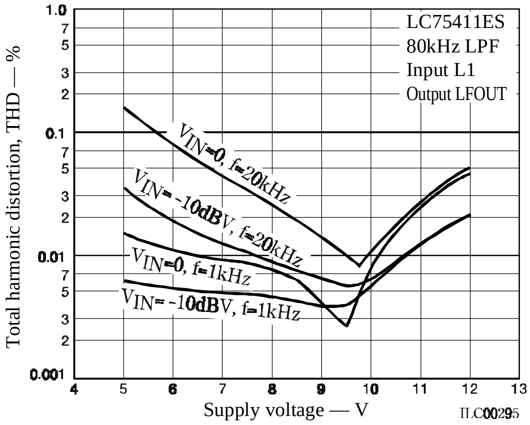


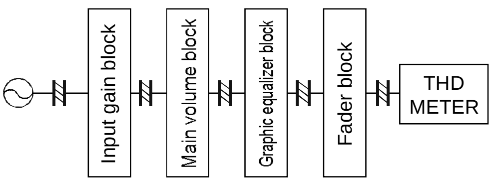
THD — Input Level Characteristics



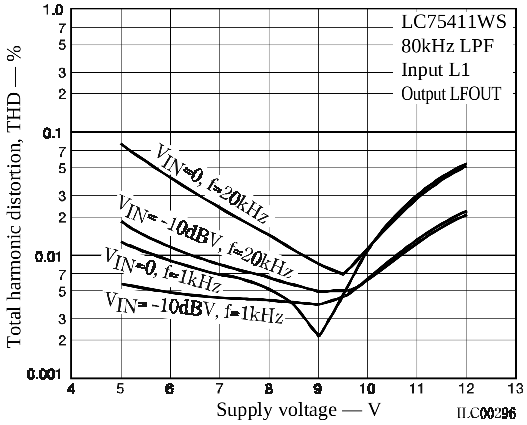


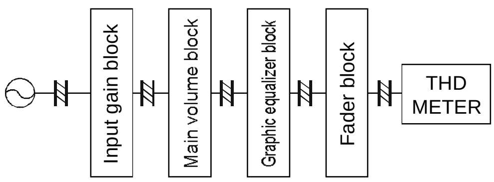
THD — Supply Voltage Characteristics



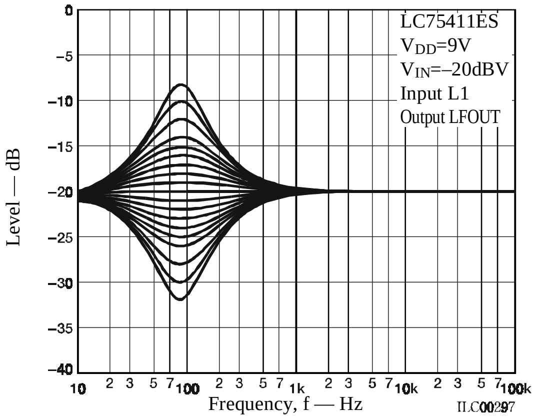


THD — Supply Voltage Characteristics

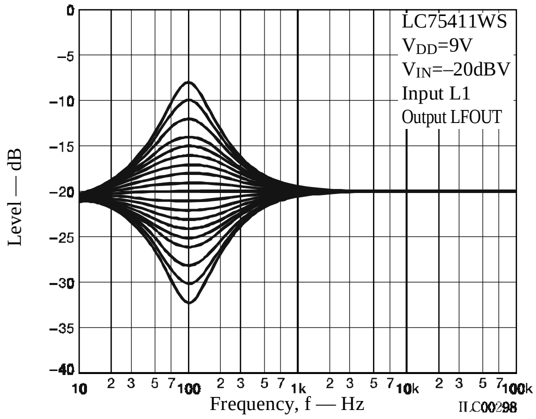




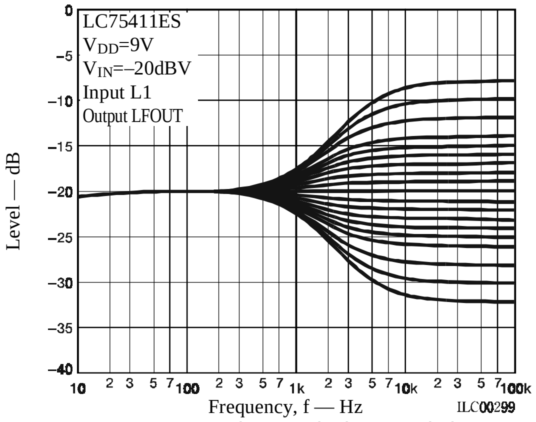
Bass Control Characteristics



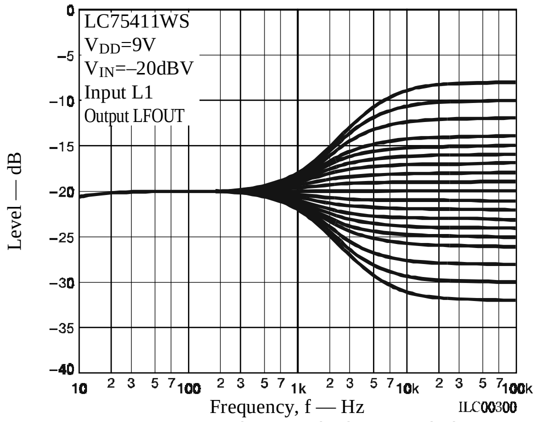
Bass Control Characteristics



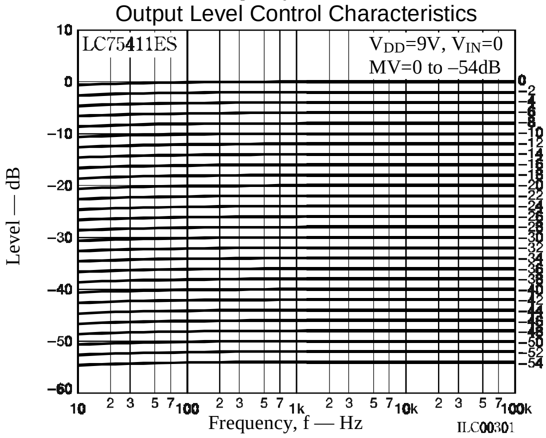
Treble Control Characteristics



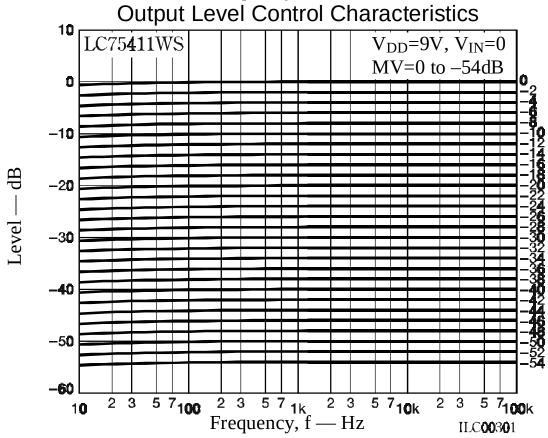
Treble Control Characteristics



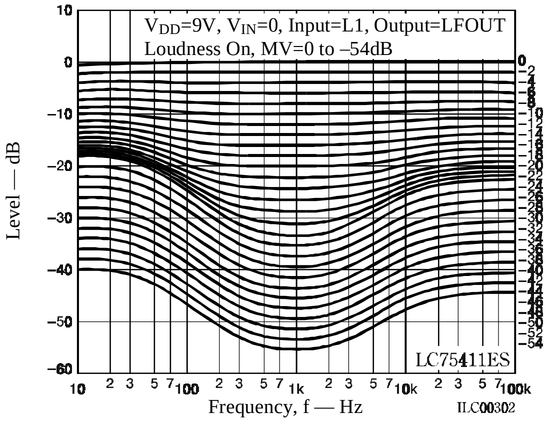
Output Level Control Characteristics



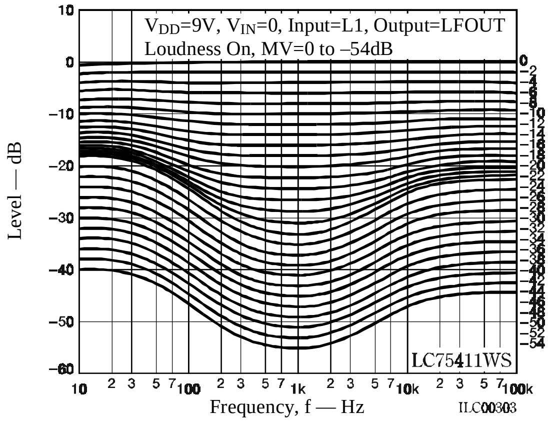
Output Level Control Characteristics



Loudness Control Characteristics



Loudness Control Characteristics



This catalog provides information as of June, 2001. Specifications and information herein are subject to change without notice.