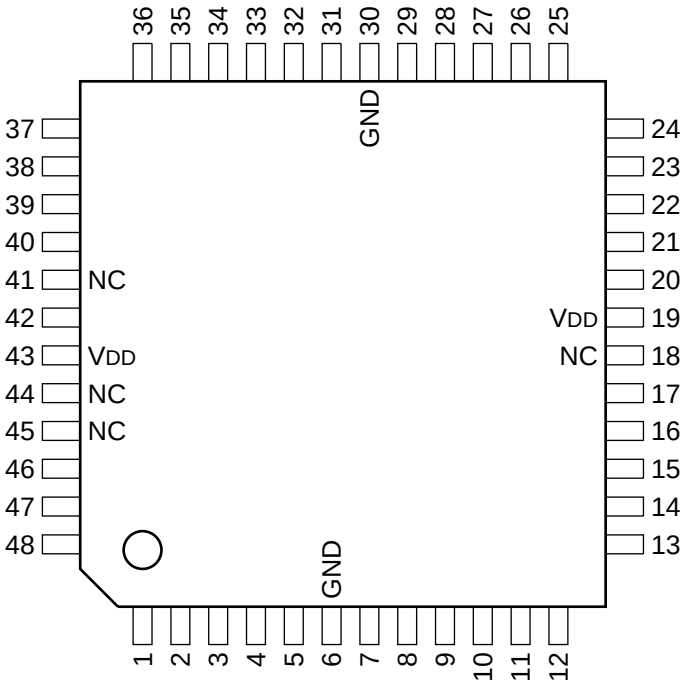
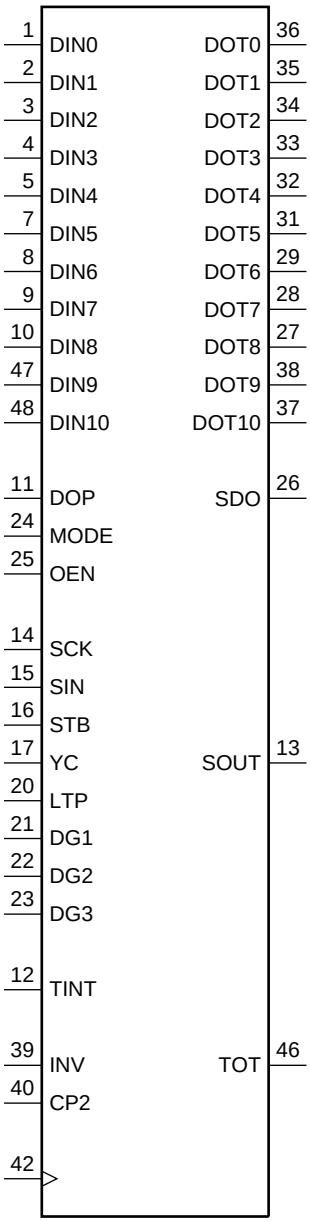
C-MOS DIGITAL DELAY LINE

—TOP VIEW—





INPUT

CLK	;	CLOCK
DIN0 - DIN10	;	DATA
DOP	;	DO PULSE
MODE	;	H : 14CK DELAY
		L : 5CK DELAY
OEN	;	OUTPUT ENABLE
		(L : DOT0-10 OUTPUT STATUS H : HIGH IMPEDANCE STATUS)
TINT	;	H : MPU COMMUNICATION MODE
SCK	;	MPU SERIAL I/F CLOCK
SIN	;	MPU SERIAL DATA IN
STB	;	MPU SERIAL I/F STROBE
YC	;	L : CHROMA, H : Y
DG1-DG3	;	FOR DIAG
LTP	;	FOR DIAG
CP2	;	TEST TERMINAL GENERALLY USE : L
INV	;	TEST TERMINAL GENERALLY USE : L

OUTPUT

DOT0 - DOT10	;	DATA
SDO	;	STRETCHED DO
SOUT	;	DATA OUT TO MPU
TOT	;	TEST

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	DIN0	13	O	SOUT	25	I	OEN	37	O	DOT10
2	I	DIN1	14	I	SCK	26	O	SDO	38	O	DOT9
3	I	DIN2	15	I	SIN	27	O	DOT8	39	I	INV
4	I	DIN3	16	I	STB	28	O	DOT7	40	I	CP2
5	I	DIN4	17	I	YC	29	O	DOT6	41	—	NC
6	—	GND	18	—	NC	30	—	GND	42	I	CLK
7	I	DIN5	19	—	V_{DD}	31	O	DOT5	43	—	V_{DD}
8	I	DIN6	20	I	LTP	32	O	DOT4	44	—	NC
9	I	DIN7	21	I	DG1	33	O	DOT3	45	—	NC
10	I	DIN8	22	I	DG2	34	O	DOT2	46	O	TOT
11	I	DOP	23	I	DG3	35	O	DOT1	47	I	DIN9
12	I	TINT	24	I	MODE	36	O	DOT0	48	I	DIN10