– OBSOLETE –

High Voltage 1 REN Ring Generator

Ordering Information

Device	Package Options
	8-Lead SO
HV421	HV421LG

Features

- Processed with HVCMOS® technology
- 4.75V to 9.5V operating supply voltage
- DC to AC conversion
- 1 REN load capacity
- Adjustable ring frequency from 15Hz to 60Hz
- Adjustable converter frequency
- Enable/Disable function

General Description

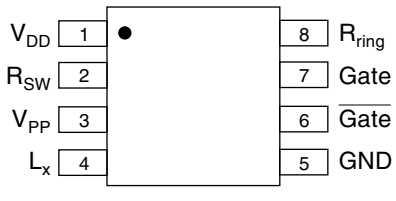
The Supertex HV421 is a high voltage ring generator designed to drive 1 North American REN (ringer equivalent number) from a 5V source. The HV421 has an internal DC-DC converter which converts the 5V DC supply to a nominal 68V DC connected to the V_{PP} pin. The DC-DC converter frequency of the HV421 is set by an external resistor connected between R_{SW} and V_{DD}. The ringing signal is generated by a high voltage H-bridge which produces two square waves which are 180 degrees from each other. The ringing frequency of the H-bridge is set by an external resistor connected between R_{RING} and V_{DD}.

Absolute Maximum Ratings*

Supply Voltage, V_{DD}	-0.5V to +10V
Output Voltage, V_{cs}	-0.5V to +120V
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	-65°C to +150°C
SO-8 Power Dissipation	400mW

Note:
*All voltages are referenced to GND.

Pin Configuration



Top View

SO-8

Electrical Characteristics

DC Characteristics (V_{DD}=5.0V, R_{RING}=30MΩ, R_{SW}=1.3MΩ, L_X=330μH, T_A=25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor		3.5	5	Ω	I=100mA
I_{DDQ}	Quiescent V_{DD} supply current			50	nA	R_{SW}=Low
I_{DD}	Input current going into the V_{DD} pin			300	μA	V_{IN}=5.0V. See Figure 1.
I_{IN}	Input current including inductor current		170	220	mA	V_{IN}=5.0V. See Figure 1.
V_{PP}	Output voltage on V_{PP}	65	68		V	V_{IN}=5.0V. See Figure 1.
F_{RING}	Ring frequency	20	25	30	Hz	V_{IN}=5.0V. See Figure 1.
D_{RING}	Ringing frequency duty cycle		50		%	
fsw	Switching transistor frequency		35		KHz	V_{IN}=5.0V. See Figure 1.
Dsw	Switching transistor duty cycle		88		%	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	4.75		9.5	V	
T_A	Operating temperature	0		85	°C	

Enable/Disable Table

Symbol	Parameter	Min	Typ	Max	Units	Conditions
EN-L	Logic input low voltage	0		0.5	V	
EN-H	Logic input high voltage	V_{DD}-0.5		V_{DD}	V	

Block Diagram

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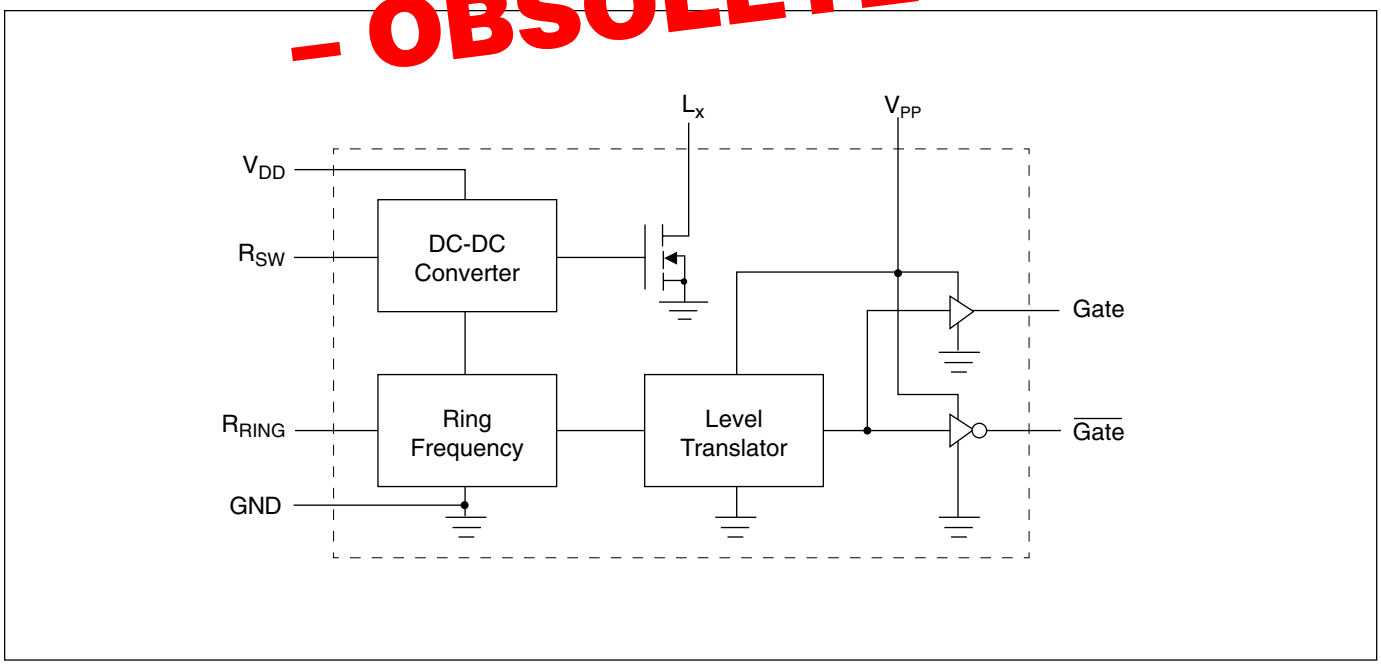
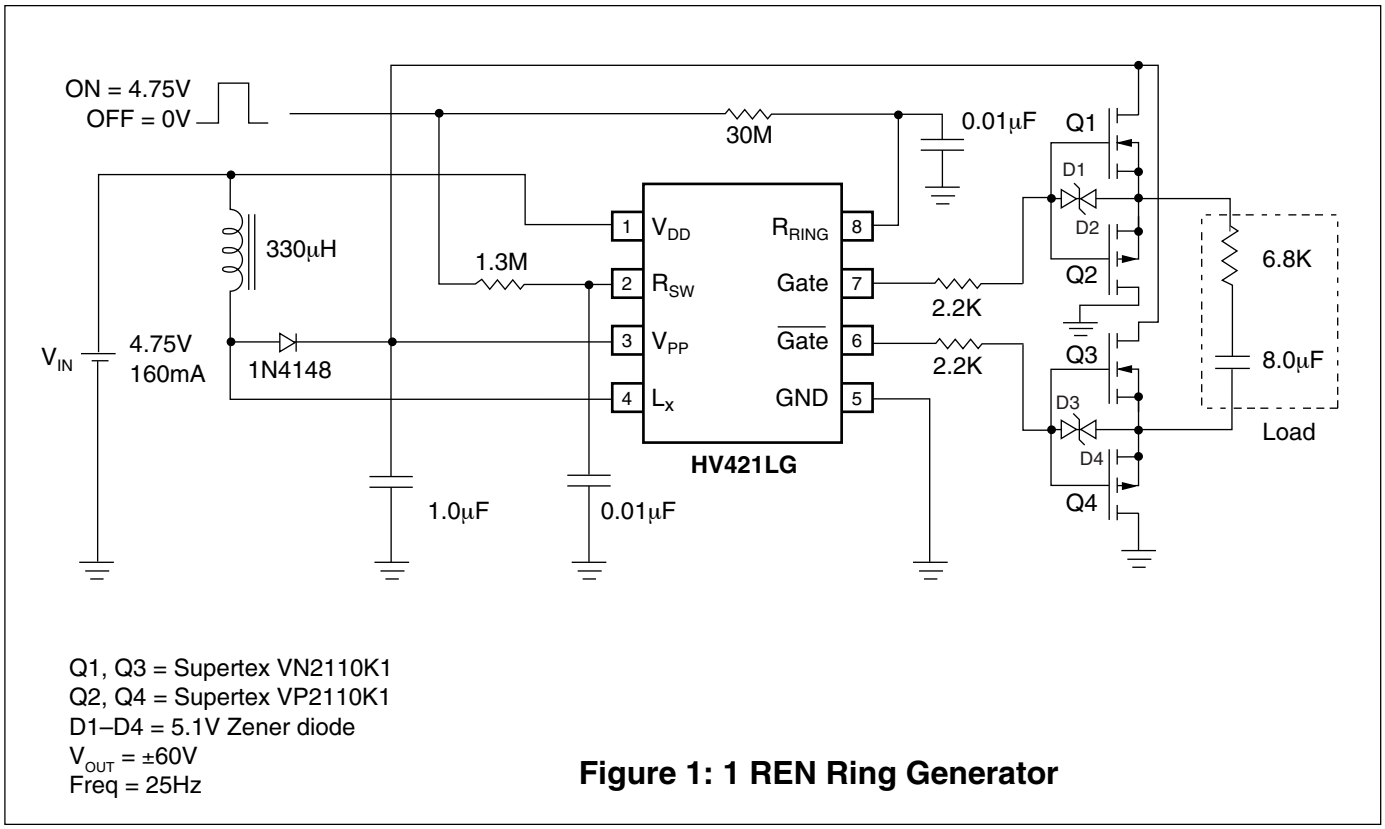


Typical Application



Q1, Q3 = Supertex VN2110K1
Q2, Q4 = Supertex VP2110K1
D1–D4 = 5.1V Zener diode
V_{OUT} = ±60V
Freq = 25Hz

Figure 1: 1 REN Ring Generator

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Application Description

The Supertex HV421LG is a high voltage 1 REN ring generator. A typical application circuit is shown in Figure 1. There are four basic parts to the circuit; the DC-DC converter, level translation of the ringing frequency, enable/disable function, and an external source follower buffer stage.

DC-DC converter

The DC-DC converter consists of a 330μH inductor, 1N4148 diode, 1.0μF capacitor and 1.3MΩ resistor. The 1.3MΩ resistor sets the DC-DC converter frequency. Energy is stored in the 330μH inductor when the switching transistor is turned on and is released into the 1.0μF capacitor when the switch is in the off state. A high voltage DC will develop at V_{PP} which is internally connected to the level translator.

Level translation of the ringing frequency

The ringing frequency is set by a 30MΩ resistor. A low voltage square wave is generated with a nominal frequency of 25Hz. Lower ringing frequencies can be obtained by using resistors greater than 30MΩ. The signal is then level translated to swing from 0V to the V_{PP} voltage. An inverted and a noninverted output are generated (gate and gate bar).

Enable/Disable function

The HV421 can be enabled by connecting the 1.3MΩ and 30MΩ resistors to the same potential as V_{DD} and disabled by connecting them to ground.

External source follower buffer stage

The gate and gate bar are connected to an external source follower stage. Supertex transistors VP2110K1 and VN2110K1 are used for the buffering. Zener diodes clamps across the gates are recommended as a precaution but not required.

The voltage seen by the load is ±60V. A 6.8KΩ resistor in series with an 8.0μF capacitor is used to simulate 1 North American REN (ringer equivalent number). The main specifications for the Supertex source follower transistors are listed below.

Device	Type	Breakdown Voltage, BV_{DSS}	Gate Threshold Voltage, $V_{GS(th)}$	On-Resistance, $R_{DS(ON)}$	Package Options
VN2110	N-Channel	100V	0.8V to 2.4V	6.0Ω at V_{GS}=5V	TO-92, SOT-23
VP2110	P-Channel	-100V	-1.5V to -3.5V	11Ω at V_{GS}=-5V	TO-92, SOT-23

Advanced Information

High-Voltage Ring Generator

Ordering Information

Operating Voltage	Package Options
V_{PP1} - V_{NN1}	SOW-20
325V	HV430WG

Features

- ☐ $100V_{RMS}$ ring signal
- ☐ Output over current protection
- ☐ 5.0V CMOS logic control
- ☐ Logic enable/disable to save power
- ☐ Fault output for over-current and low voltage lockout conditions
- ☐ Adjustable deadband in single-control mode
- ☐ Power-on reset for hot-swap protection
- ☐ Low voltage lockout

Applications

- ☐ High voltage ring generator
- ☐ Set-top/Street box ring generator

General Description

The Supertex HV430 is a high voltage PWM ring generator integrated circuit. The high voltage outputs, Pgate and Ngate, are used to drive the gates of external high voltage P-channel, TP2640, and N-channel, TN2640, MOSFETs in a push-pull configuration. Pulse by pulse over current protection are implemented on both the P-channel and N-channel MOSFETs. The RESET inputs functions as a power-on reset and as a low voltage lockout, allowing for hot-swapping capabilities. The FAULT output indicates over-current and low voltage lockout conditions. It is active-low and open-drain to allow wire OR'ing of multiple drivers.

P_{GATE} and N_{GATE} are controlled independently by logic inputs P_{in} and N_{in} when the mode pin is at logic high. A logic high on P_{in} will turn on the external P-channel MOSFET. Similarly, a logic high on N_{in} will turn on the external N-channel MOSFET. Lockout circuitry prevents the N and P switches from turning on simultaneously.

For applications where a single control input is desired, the mode pin should be connected to Gnd. The PWM control signal is then input to the N_{in} pin. A user-adjustable deadband in the control logic assures break-before-make on the outputs, thus avoiding cross conduction on the high voltage output during switching. A logic high on Nin will turn the external P-Channel MOSFET on and the N-Channel off, and vice versa. The IC can be powered down by applying a logic low on the Enable pin, placing both external MOSFETs in the off state.

Absolute Maximum Ratings

V_{PP1} - V_{NN1}, power supply voltage	+340V
V_{PP1}, positive high voltage supply	+220V
V_{PP2}, positive gate voltage supply	+220V
V_{NN1}, negative high voltage supply	-220V
V_{NN2}, negative gate voltage supply	-220V
V_{DD}, logic supply	+7.5V
Storage temperature	-65°C to +150°C
Power dissipation	800mW