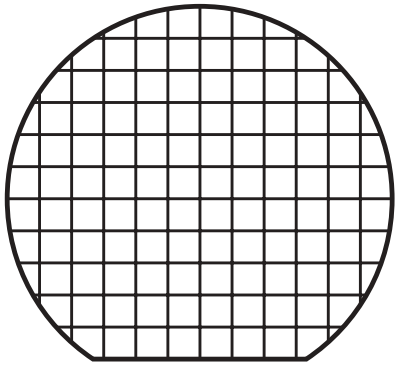
XRA00

UHF, EPCglobal Class 1b, Contactless Memory Chip 96 bit ePC with Inventory and Kill Function

FEATURES SUMMARY

- ePCglobal Class 1b Specification
- Passive Operation (No Battery Required)
- UHF Carrier Frequencies From 860MHz to 960MHz ISM Band Which Comply To:
  - North American Regulation
  - European Regulation
  - Similar Regulations in Other Countries
- To the XRA00:
  - Asynchronous 50% to 100% ASK Modulation Using PWM Pulse Coding (15K to 70Kbits/s)
- From the XRA00:
  - Backscattered rEflective Answers using FSK bit coding (30K to 140Kbits/s)
- 128 bit EEPROM with Lock Bit
- 96 Bit ePC
- Internal PLL for Data Transfer Synchronisation
- Inventory, Read, Prog and Erase features
- Persistance Mode For Inventory Sequence Optimisation
- Kill Command
- 30ms Programming Time (typical)
- More than 10,000 Write/Erase cycles
- More than 40 Years' Data Retention

Figure 1. Delivery Forms



Unsawn unbumped wafers or sawn and bumped wafers

TABLE OF CONTENTS

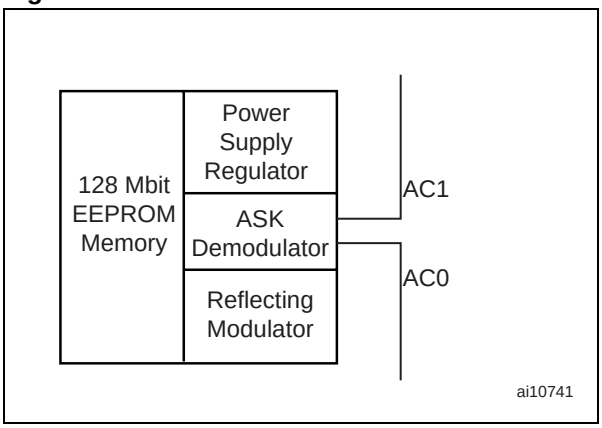
SUMMARY DESCRIPTION

The XRA00 is a low-cost integrated circuit for use in Radio Frequency Identification (RFID) transponders (tags) operating at UHF frequencies. It is a 128 bit memory organized as 8 blocks of 16 bits as shown in Table 5.

When connected to an antenna, the operating power is derived from the RF energy produced by the RFID Reader. Incoming data are demodulated and decoded from the received Amplitude Shift Keyed (ASK) signal and outgoing data are generated by the antenna reflectivity change using the Frequency Shift Keying (FSK) coding principle. The Data transfer rate is determined by the local UHF frequency regulation.

The XRA00 follows the ePCglobal Class 1b UHF recommendation for the radio-frequency power and signal interface.

Figure 2. Pad Connections



The dialogue between the Reader and the XRA00 is conducted through the following consecutive operations:

- activation of the XRA00 by the UHF operating field of the Reader
- transmission of a command by the Reader
- transmission of a response by the XRA00

This technique is called Reader Talk First (RTF).

Table 1. Signal Names

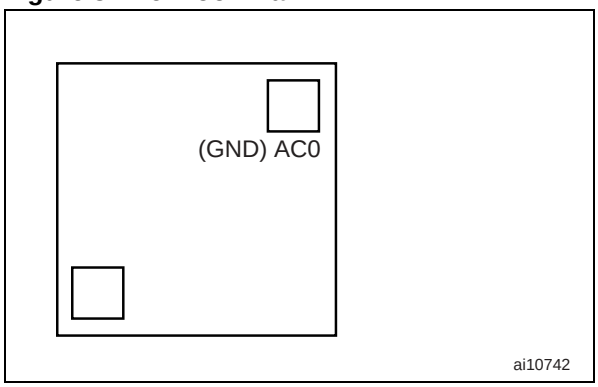
AC1	Antenna Pad
AC0 (GND)	Antenna Pad

The XRA00 is specifically designed for extented range applications that need automatic item identification. The XRA00 provides a fast and flexible anti-collision protocol that is robust under noisy and unpredictable RF conditions typical of RFID applications. It is based on a determinist binary tree scanning method accelerated by bin slot distribution. The XRA00 EEPROM memory can be read and written, so that the users can program the ePC code themselves, if desired.

The XRA00 has the following command set:

- ***SCROLLID:*** XRA00, matching data sent by the Reader, replies by sending back the entire ID Code. This command is used during the anti-collision sequence.
- ***SCROLLALLID:*** XRA00 replies in an indiscriminate way by sending back the entire ID Code.
- ***PINGID:*** This command is used as part of a multi-XRA00 anti-collision sequence. XRA00, matching data sent by the Reader, responds in one of the eight specific bin slots.
- ***QUIET:*** XRA00, matching data sent by the Reader, enters the Asleep state where it no longer responds to the Reader commands. The memory remains in the Asleep state until a valid Talk command is received or the persistence mode limit time has run out.
- ***TALK:*** XRA00, matching data sent by the Reader, returns to the Awake state where it responds to commands from the Reader.
- ***KILL:*** XRA00, matching the entire ID Code, 16 bit CRC and the 8 bit Kill Code sent by the Reader, no longer responds to Reader queries.
- ***ERASEID:*** The EraseID command is used to erase the entire memory array.
- ***PROGRAMID:*** XRA00 programming is accomplished 16 bits at a time. Programming is allowed only when the XRA00 is not locked.
- ***VERIFYID:*** The VerifyID command is used to verify that all memory data bits have been programmed correctly.

Figure 3. Die Floor Plan



DATA TRANSFER

Input Data Transfer from the Reader to the XRA00 (Request Frame)

The RF Interface and Voltage Multiplier convert the RF energy into the DC power required for the XRA00 to operate. It provides modulation information to the ASK demodulator which discriminates between High and Low digital levels and forwards this discriminated signal to the State Logic for Data Recovery (see Figure 4.).

Within the State Logic, the Data Recovery and Timing Block recovers the data from the de-modulated signals and generates commands and control functions that coordinate all of the XRA00 operations. The State Logic interprets the Request Frame, performs the required internal operations and determines if a response is required. The State Logic implements the State Diagram and Communications Protocols.

The Reader-to-XRA00 link makes use of Amplitude Shift Keying (ASK) with a maximum modulation depth of 100% (see Figure 5.). Because of the local UHF frequency regulation, the shape, depth and rate of the modulation are variable within the limits described in Table 2. The XRA00 adjusts its timing over a range of modulation rates to lock to Reader transmissions automatically.

Figure 4. ASK Modulation of the Received Wave

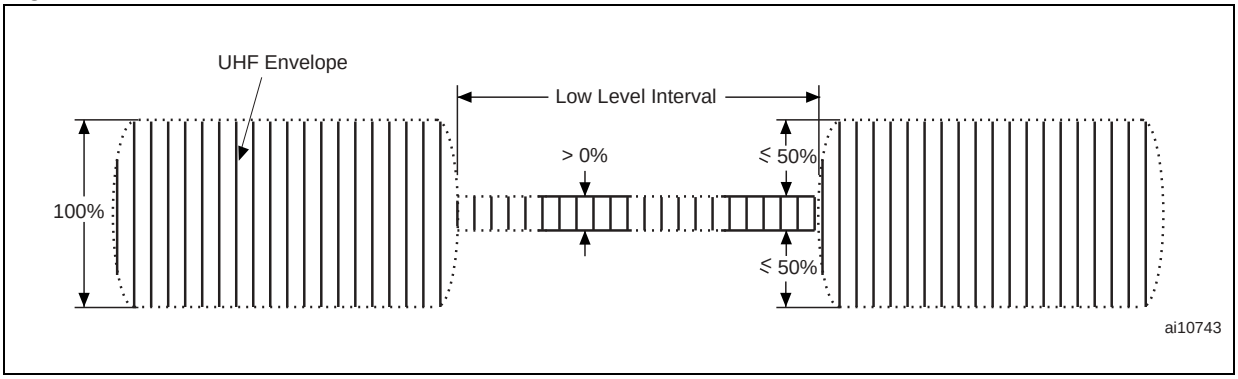
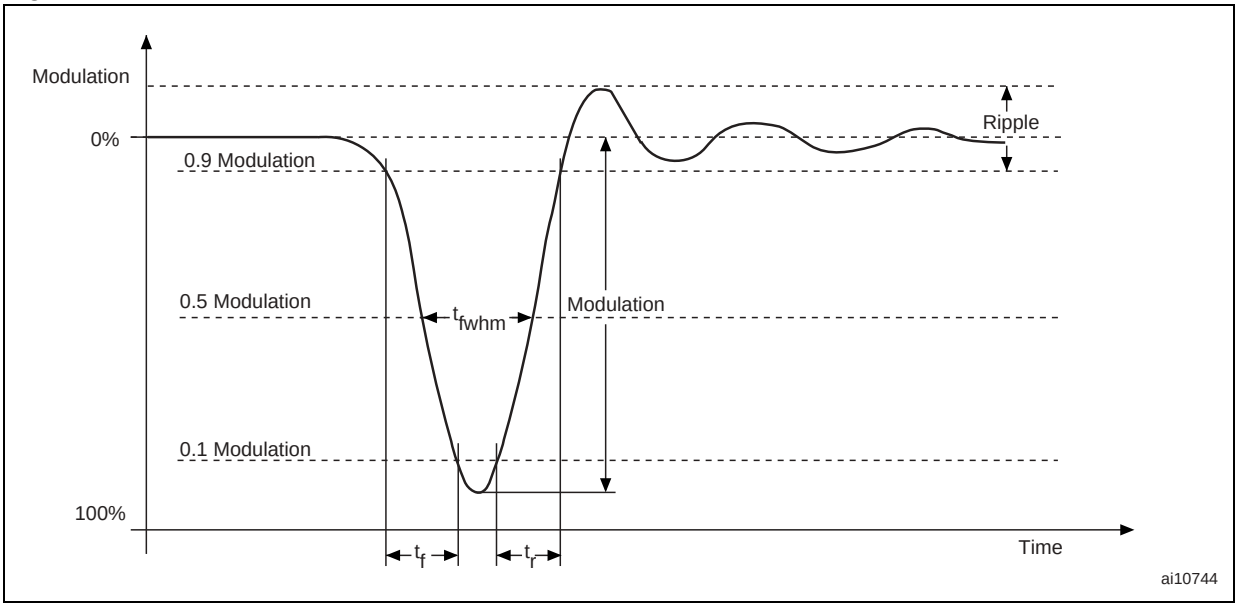


Figure 5. ASK Pulse Modulation Parameters



Symbol Transmission Format for Request Frame

Modulation of negative pulse width (RF interruption period) is used for data transmission and synchronization to XRA00s. Four timings are distinguished by their shortness. Their symbols are as follows:

- t_{fwhm0}: encode binary data "0"
- t_{fwhm1}: encode binary data “1”
- $t_{fwhmBin}$: encode Bin synchroniZation pulse
- $t_{trangap}$: encode Transaction Gap pulse

Each symbol is referenced to the Master Clock Time Period, t_0, which is defined by the Reader during the Request Frame header modulation. t_0 is the bit duration period generated by the Reader.

Request Binary Data "0"

Data Modulation Timing, t_{fwhm0}, for Reader-to-XRA00 clocking when data = "0", is encoded by a "narrow" $1/8t_0$ pulse width modulation. This timing is also used during data synchronization at the begining of each Request Frame. t_{fwhm0} is illustrated in Figure 6.

Request Binary Data "1"

Data Modulation Timing, t_{fwhm1}, for Reader-to-XRA00 clocking when data = "1", is encoded by a "wide" $3/8t_0$ pulse width modulation. This timing is also used for SOF (Start Of Frame) and EOF (End Of Frame) symbols within the Request Frame. t_{fwhm1} is illustrated in Figure 7.

Bin pulse and Bin Response Window

XRA00 Answer Frames are synchronized by the Reader using Bin pulse modulation. The Bin pulse is encoded by a $3/8t_0$ pulse width modulation.The Bin pulse is also used to define the Bin Response Window time slots during the inventory sequence after a PINGID command is issued. The Bin Response Window is shown in Figure 8.

Transaction Gap

During communication with XRA00, each Request Frame begins with a transaction gap, $t_{trangap}$, followed by a period of time, $t_{transetup}$, during which the carrier frequency is unmodulated (See Figure 9. for an illustration and Table 2. for the value of $t_{transetup}$). $t_{transetup}$ precedes the Data Modulation Window.

Power Up

If during communication with the Reader the carrier is turned off for a time exceeding t_{Reset} , XRA00 loses DC power. After XRA00 is powered up again, a minimum time of $t_{transetup}$, during which the carrier frequency is unmodulated, must precede the Data Modulation Window. (See Figure 10. for an illustration and Table 2. for the value of $t_{transetup}$.)

Figure 6. Data Modulation Timing - “0”

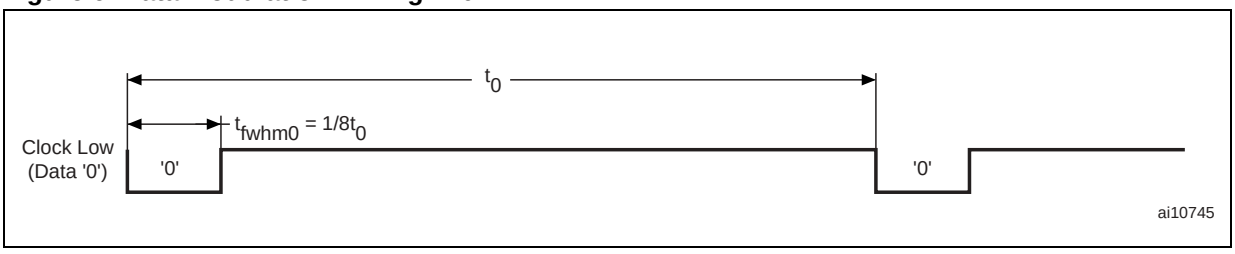


Figure 7. Data Modulation Timing - “1”

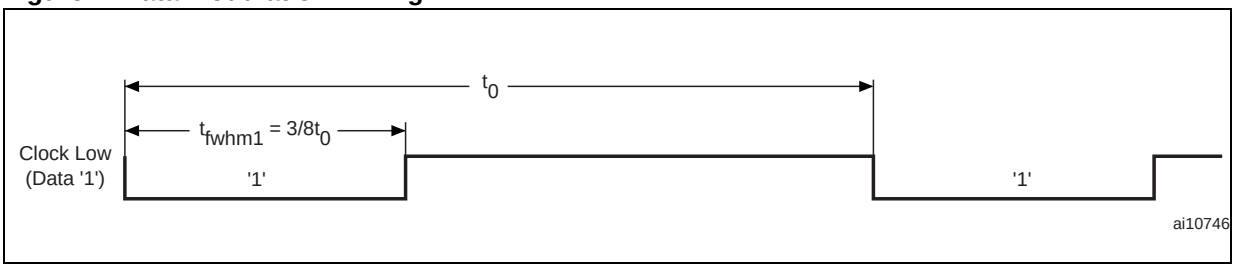


Figure 8. Bin Response Window Timing

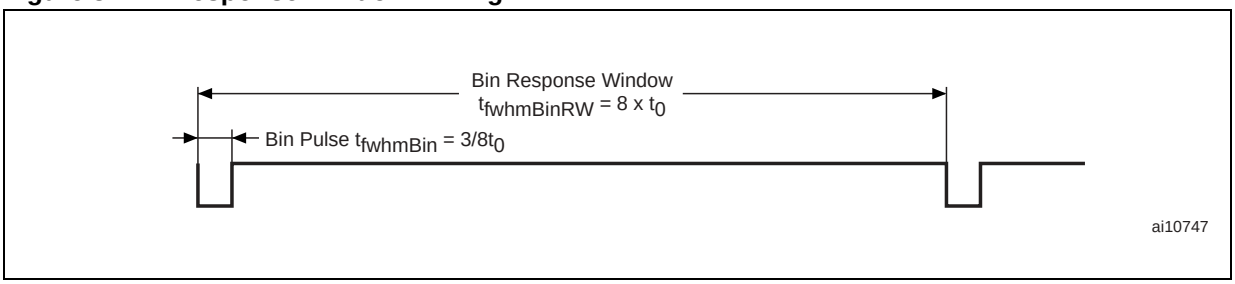


Figure 9. Transaction Gap Timing

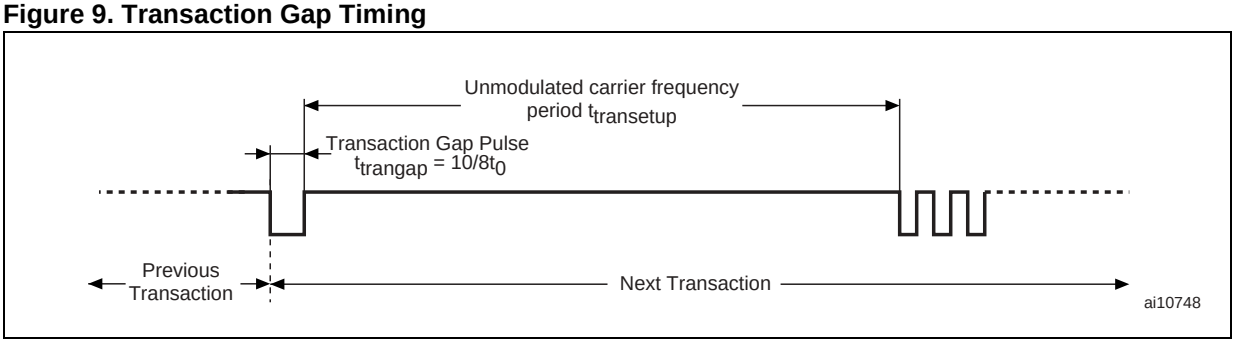


Figure 10. Transaction after Power Up

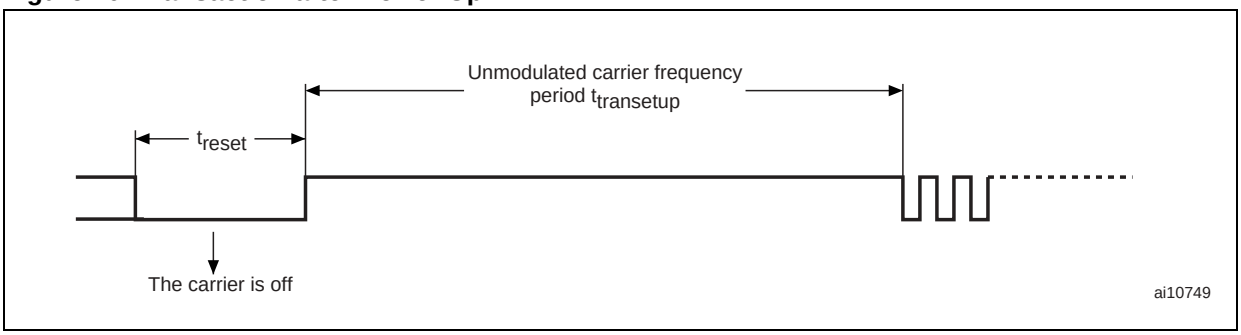


Table 2. Request Modulation Pulse Parameters for North American Operation (-20 to 55°C)

Symbol	Description	Min	Max	Units
F_C	UHF Carrier Frequency	900	930	MHz
t_0	Master Clock Time Period for a single bit sent to the XRA00	12.5	16.6	µs
T_{0Tol}	Master Clock Time Period Tolerance	-1	+1	%
$1/t_0$	Request Frame Data Rate ($1/t_0$)	60	80	Kbps
T_{fwhm0}	Pulse Modulation Width of Binary Data 0 at 50% Level	$1/8 * T_0$		µs
T_{fwhm1}	Pulse Modulation Width of Binary Data 1 at 50% Level	$3/8 * T_0$		µs
$T_{fwhmBin}$	Pulse Modulation Width of Bin Pulse at 50% Level	$3/8 * T_0$		µs
$T_{trangap}$	Pulse Modulation Width of Transaction Gap at 50% Level	$10/8 * T_0$		µs
$T_{fwhmBinRW}$	Bin Response Window at 50% Level	$4*T_0$	$8*T_0$	µs
$T_{transetup}$	Delay between Transaction Gap and Data Modulation Windows	64		µs
$T_{tranhold}$	Delay before the next Transaction Gap	$2.5*T_0$	2000	µs
t_f	Pulse Modulation Fall Time (90% to 10% level)		300	ns
t_r	Pulse Modulation Rise Time (10% to 90% level)		300	ns
Ripple	Ripple		10	%
MOD	Pulse Modulation Depth	80	100	%
t_{Coast}	Delay between Request EOF and the next Transaction Gap		20	ms
t_{Reset}	RF Off time to Power down a XRA00	200		µs

Table 3. Request Modulation Pulse Parameters for European Operation (-20 to 55°C)

Symbol	Description	Min	Max	Units
F_C	UHF Carrier Frequency	860	870	MHz
t_0	Master Clock Time Period for a single bit sent to the XRA00	40	66,67	µs
t_{0Tol}	Master Clock Time Period Tolerance	-1	+1	%
$1/t_0$	Request Frame Data Rate ($1/T_0$)	15	25	Kbps
t_{fwhm0}	Pulse Modulation Width of Binary Data 0 at 50% Level	$1/8 * T_0$		µs
t_{fwhm1}	Pulse Modulation Width of Binary Data 1 at 50% Level	$3/8 * T_0$		µs
$t_{fwhmBin}$	Pulse Modulation Width of Bin Pulse at 50% Level	$3/8 * T_0$		µs
$t_{trangap}$	Pulse Modulation Width of Transaction Gap at 50% Level	$10/8 * T_0$		µs
$t_{fwhmBinRW}$	Bin Response Window at 50% Level	$4*T_0$	$8*T_0$	µs
$t_{transetup}$	Delay between Transaction Gap and Data Modulation Windows	64		µs
$t_{tranhold}$	Delay before the next Transaction Gap	$2.5*T_0$	2000	µs
t_f	Pulse Modulation Fall Time (90% to 10% level)		300	ns
t_r	Pulse Modulation Rise Time (10% to 90% level)		300	ns
Ripple	Ripple		10	%
MOD	Pulse Modulation Depth	40	60	%
t_{Coast}	Delay between Request EOF and the next Transaction Gap		20	ms
T_{Reset}	RF Off time to Power down a XRA00	200		µs

Note: The data shown in Table 3. is Preliminary Data. It is subject to change without previous notice.

Request Frame Format

Readers communicate with the XRA00 using two types of modulation: Data modulation and Bin modulation.

Data modulation is used to transmit data from the Reader to the XRA00.

Bin modulation is used to synchronize XRA00 answers and define time slot intervals while running the XRA00 anti-collision algorithm after a PINGID command.

All transactions begin with a transaction gap pulse, $t_{trangap}$, followed by a period of time at least equal to $t_{transetup}$ that precedes the Data modulation window as described in Figure 11.

During the Data modulation, the Reader provides a master clock signal to XRA00 devices located in its neighborhood. The time between clock pulses, t_0, determines the Reader-to-XRA00 data rate.

The XRA00 devices are synchronized to the Reader on the negative-going edge of the low level interval of the RF envelope. There is a proportional relationship between this fundamental frequency and all subsequent signaling.

The encoding used for the binary data from the Reader to the XRA00 is the pulse width modulation of the low level pulse as shown in Figure 12. Logical 0 is defined as a modulation whose width is 1/8 of the master clock interval (Figure 6.), t_0. Logical 1 is encoded as a modulation whose width is 3/8 of the master clock interval (Figure 7.), t_0.

After the Data modulation windows in which the Reader generates the XRA00 command, the Reader generates Bin pulses to define the time slots used by the XRA00 to answer. During the first interval, after the Data modulation EOF, the XRA00 sets up for answers. The XRA00 uses one out of two Bin modulation schemes depending on the Reader command.

For SCROLL commands, the Reader generates 1 Bin pulse used for synchronization, followed by the XRA00 answer.

For PING commands, the Reader generates 8 BIN pulses to define 8 BIN response windows. These 8 BIN response windows are used to delineate XRA00 answers during a PINGID command.

A BIN interval is defined by a BIN pulse with a width of $t_{fwhmBin} = 3/8t_0$, followed by a BIN response window delay of $t_{fwhmBinRW} = 8T_0$.

At the end of a complete transaction, a minimun delay of $t_{tranhold}$ = 2.5t_0 (but that cannot exceed t_{coast}) is required before the XRA00 is ready to receive the next Transaction Gap.

Figure 11. Reader to XRA00 Modulation Overview (Request Frame)

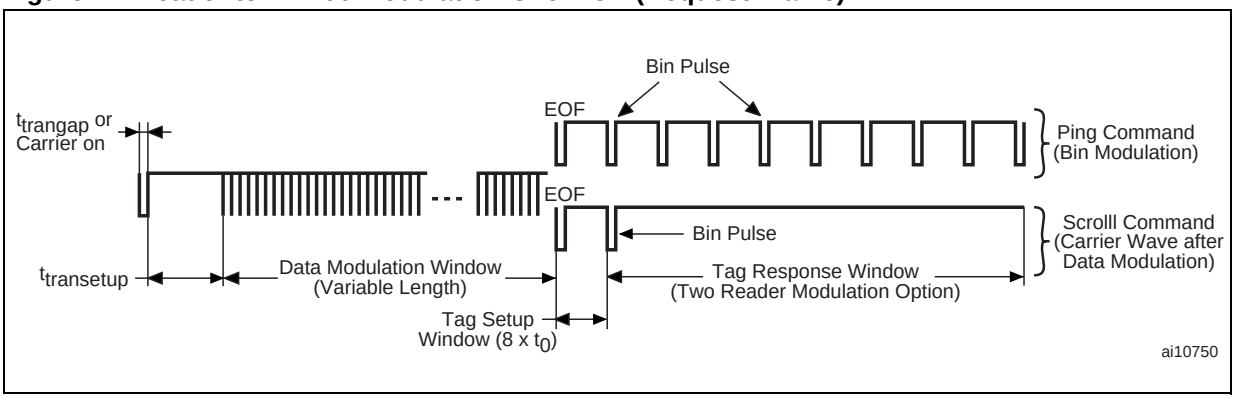


Figure 12. Data Modulation Window

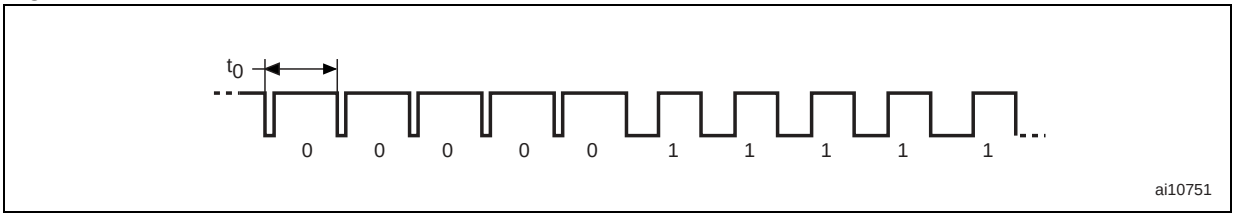


Figure 13. Bin Modulations

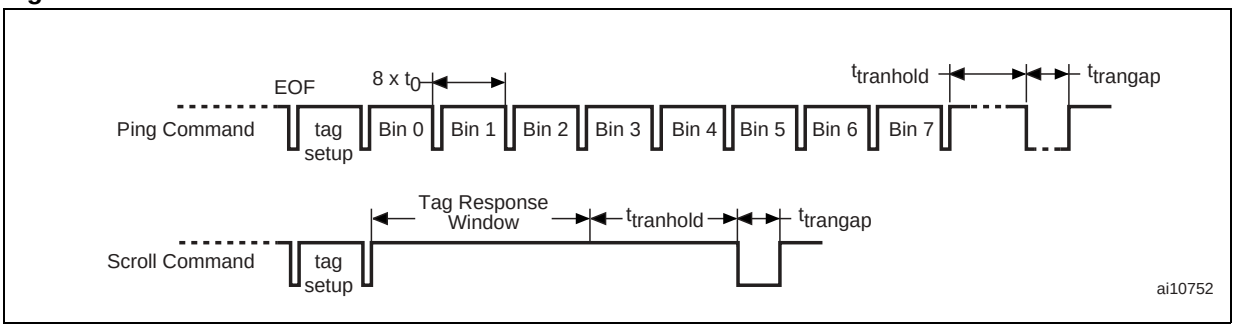
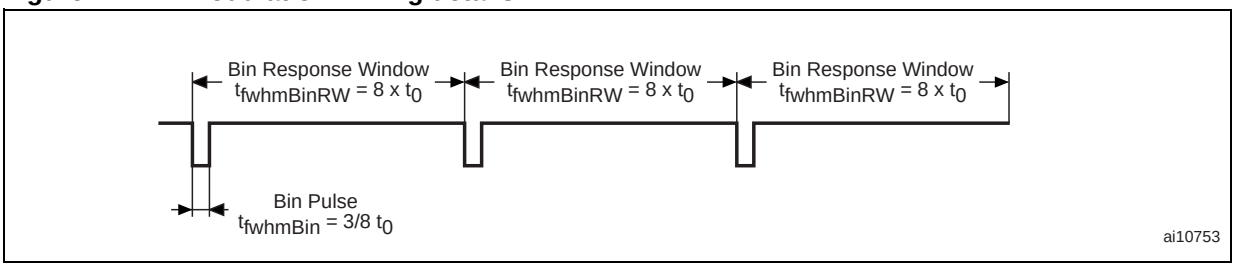


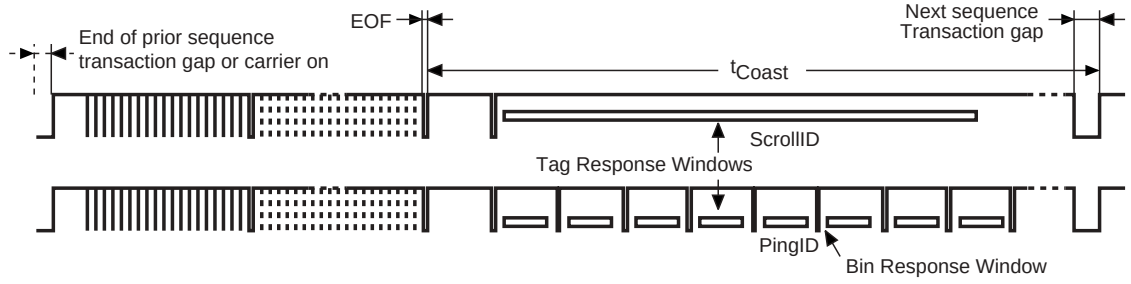
Figure 14. Bin Modulation Timing details



Coast Interval

In order for the XRA00 to be able to detect the next Transaction Gap, the Reader must start the next transaction within t_{coast} (see Figure 15.). This restriction does not apply when the carrier has been turned off long enough (at least for t_{Reset}) for DC power to be removed from the XRA00 as the XRA00 will re-synchronize at the next power-up.

Figure 15. Coast Interval

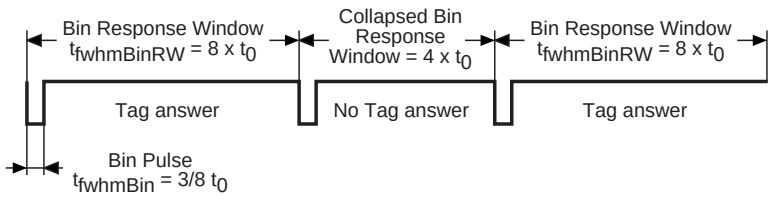


Ping Reply Bin Collapse

The Reader may optionally shorten the Ping transaction time by shortening the Bin response window. The Reader may listen to a XRA00 reply during the Bin response window for a minimum time of $4t_0$ (= $t_{tagscrollDell}$ max), which is half the standard BIN response window time. If no XRA00 response is detected, the Reader can generate the next BIN pulse. This condition may be applied to each of the 8 BIN intervals if the Reader detects no reply from a XRA00. The middle Bin response window shown in Figure 16. has been shortened due to no XRA00 reply.

A Bin response window may not be collapsed (shortened) if an answer from the XRA00 is detected. If the Reader collapses an occupied Bin interval, the reply from the occupying XRA00 may overlap the collapsed Bin response window and continue into the next one. The Reader may decode the overlapping reply as a collision in the next Bin response window and will have to solve the case.

Figure 16. Collapsed Ping Response

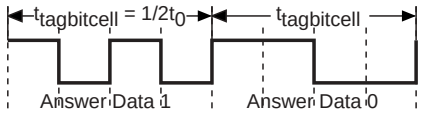


Output Data Transfer from the XRA00 to the Reader

Answer Binary Data Bits 0 and 1. The backscattered answer from the XRA00 is modulated by a selection of one out of two symbols per data bit cell. The data bit cell period $t_{tagbitcell}$ is defined as 2 transitions for a binary data 0, and 4 transitions for a binary data 1 as shown in Figure 17. The nominal data rate for the XRA00 answer is synchronized to twice the Request data rate (defined in Table 4.).

Under this encoding scheme, there are always transitions in the middle of a data bit and the sequence of 0's and 1's remains unchanged when the code is inverted as shown in Figure 19.

Figure 17. XRA00 Answer Binary Data Bit Cell Encoding



Answer Frame from the XRA00 to the Reader.

The XRA00 answers to Reader commands with a backscatter modulation that follows the FSK bit coding scheme as shown in Figure 17. This scheme define two symbols which are binary data 0 and binary data 1, respectively.

After a Reader BIN pulse, the XRA00 waits for a time that depends on the received command before starting to generate the answer. The XRA00 answer consists of an 8 bit Preamble followed by the data bits read from the non-volatile memory. The preamble has a fixed value of 11111110 and is sent as shown in Figure 18. The data bits are sent lowest bit address first.

Figure 18. XRA00 Answer Preamble

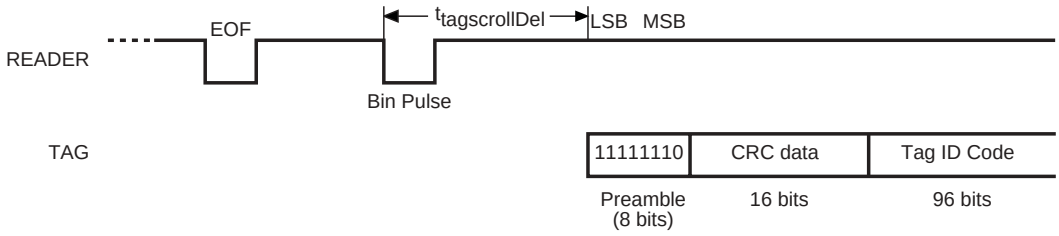
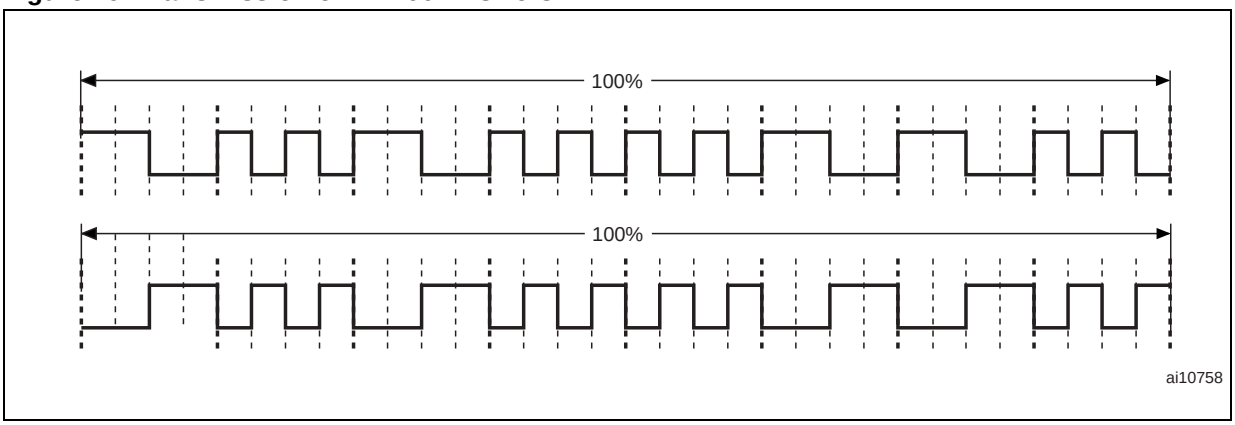


Figure 19. Transmission of XRA00 Answers



XRA00 Answer Bit Cell Variation. Durind the Reader Request Frame command, the XRA00 synchronizes its internal PLL (Phase Lock Loop) to the Master Clock Time Period, t_0, generated by the Reader. Due to the internal PLL drift in the XRA00, the answer data bit cell period $t_{tagbitcell}$ may vary by up to $\pm 1/8t_0$.

Figure 20. XRA00 Answer Bit Cell Variation

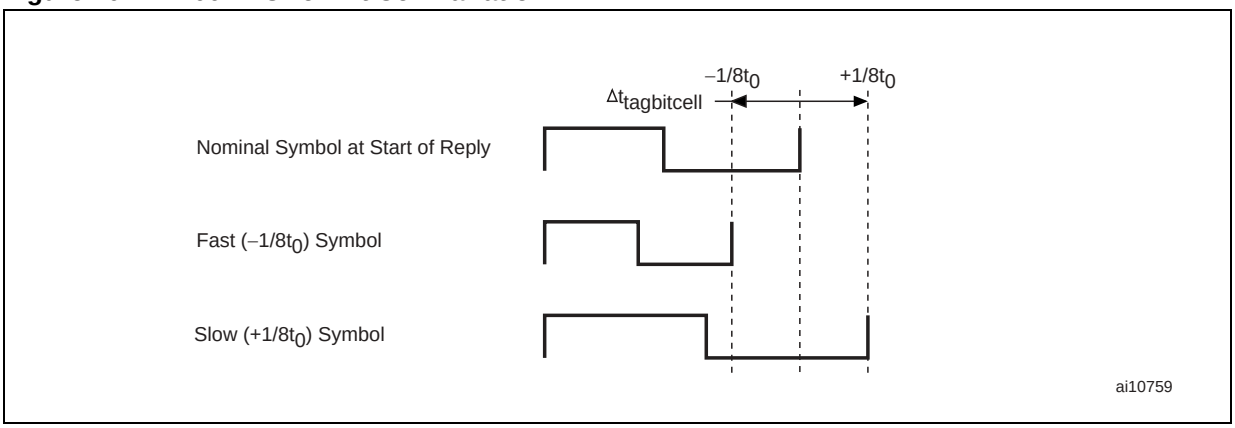


Table 4. XRA00 Backscattered Answer Modulation Parameters

Symbol	Description	Min	Max	Units
t_0	Master Clock Time Period for a single bit sent to the XRA00 North American Operation	12.5	16.6	µs
	Master Clock Time Period for a single bit sent to the XRA00 European Operation **Preliminary Data**	40	66.67	µs
$t_{tagbitcell}$	XRA00 to Reader data bit cell period	1/2 x t_0		µs
$t_{tagbitcellTol}$	XRA00 to Reader data bit cell period Tolerance (measured on 96+16+8 bits)	±1/8 x t_0		µs
2 / t_0	Answer Frame Data Rate ($2/t_0$) for North American Operation	120	160	kbps
	Answer Frame Data Rate ($2/t_0$) for European Operation **Preliminary Data**	30	50	kbps

$t_{tagscrollDel}$	SCROLLID Answer Delay from Reader BIN pulse (nominal value 4.75 x $t_{0)}$	4.68 x t_0	4.82 x t_0	µs
	PINGID Answer Delay from Reader BIN Pulse (nominal value 4.25 x $t_{0)}$	4.18 x t_0	4.32 x t_0	µs
$t_{tagscrollRep}$	XRA00 SCROLL answer duration (96+16+8 bits, nominal value 120 x $t_0/2$)	108 x $t_0/2$	132 x $t_0/2$	µs
t_{erase}	Erasing time		30	ms
t_{pgm}	Programming time		30	ms
t_{Kill}	Kill time		30	ms

Scroll Answer. The duration of a ScrollID answer, $t_{tagscrollRep}$, is illustrated in Figure 21.

The time required from the BIN pulse to the start of a ScrollID or VerifyID answer, $t_{tagscrollDel}$, is illustrated in Figure 22.

Figure 21. XRA00 Scroll Answer Duration

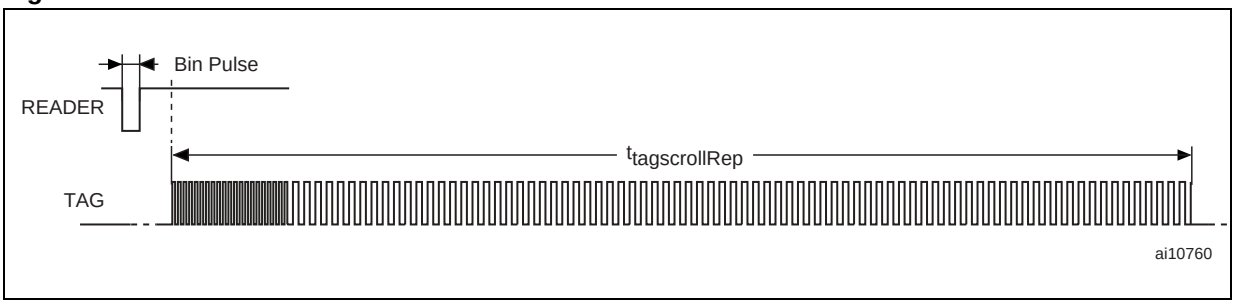
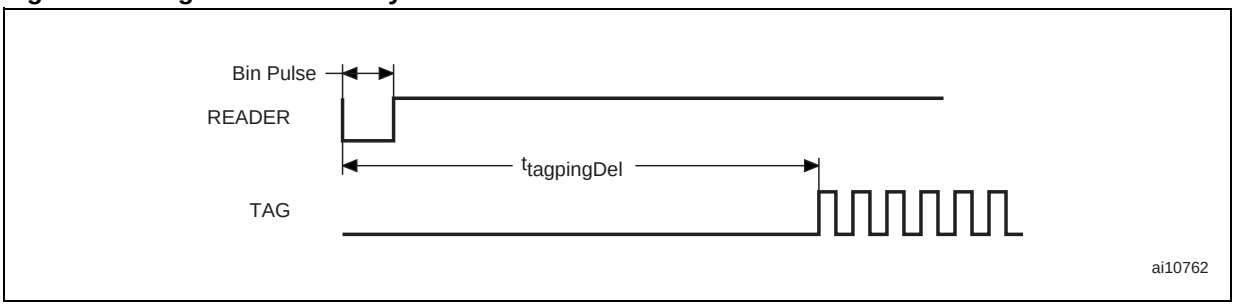


Figure 22. ScrollID Answer Delay

PingID Answer Delay. The time required from a BIN pulse to the start of a PingID answer, $t_{tagpingDel}$, is illustrated in Figure 23.

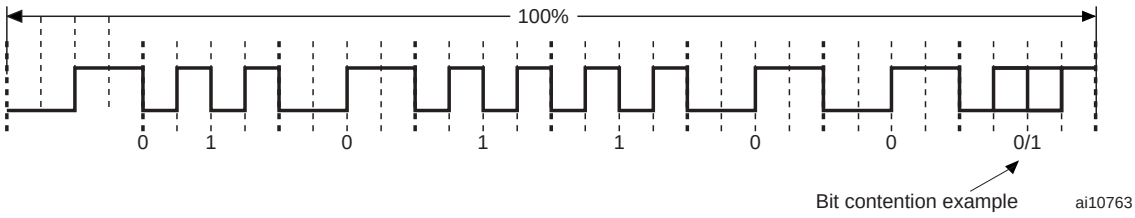
Figure 23. PingID Answer Delay



Contention Detection

Contention detection is essential for most anti-collision algorithms. When two XRA00 devices have the same clock rate and differ by only one bit, the resulting difference in backscatter modulation waveform should be readily detected by the Reader. Figure 24. shows XRA00 devices that present the same backscatter modulation intensity and are communicating simultaneously. Differences in backscatter modulation intensity can also be used to help detect contention.

Figure 24. Contention of Two XRA00 Devices with the Same Clock Rate and a 1-Bit Difference

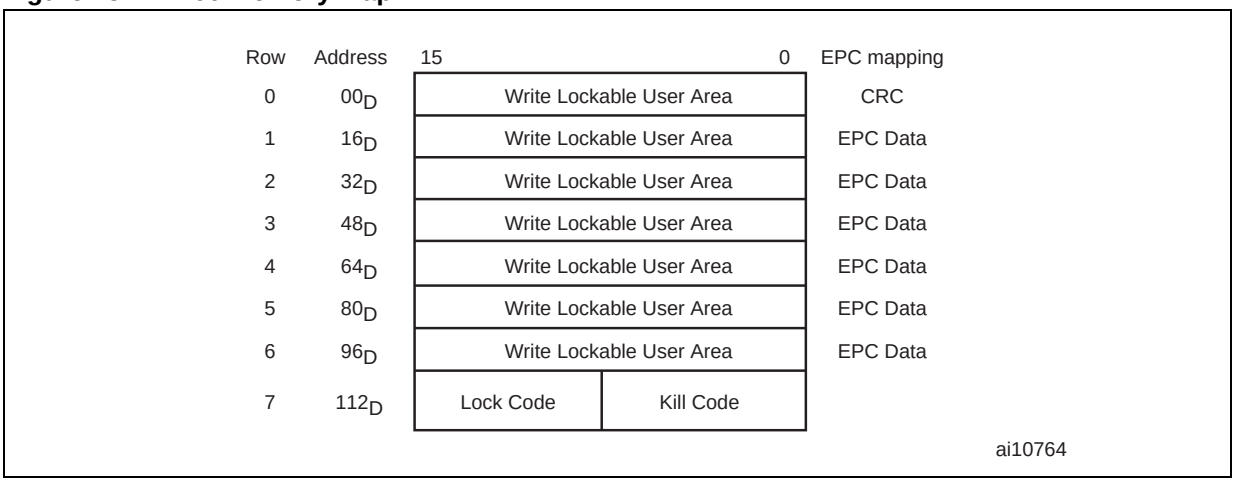


MEMORY MAPPING

The XRA00 is divided into 8 blocks of 16 bits. The device is read bit by bit and written to on a block by block basis (16 bits at a time). The XRA00 memory map is shown in Figure 25.

In the XRA00, the first block is used to store the CRC value as defined in the ePC specification. The next 6 blocks are used to store the 96-bit ePC code that is used during the inventory sequence. The last block is divided into two 8-bit areas, one that contains the Kill Code and the other that contains the Lock Code used to protect the memory data contents.

Figure 25. XRA00 Memory Map



Note: 1. ST may write part of the ePC code.

USER mode

After programming the ePC information, the XRA00 can be locked. Once locked, the XRA00 answers to anti-collision and scroll commands only. The ERASEID, PROGRAMID and VERIFY-ID commands are de-activated.

COMMAND-REPLY

System communications follow a two-phase command-reply pattern where the Reader initiates the transaction (Reader Talks First, RTF). In the first phase, the Reader provides power to one or more passive XRA00 device(s) with continuous wave RF energy. The XRA00 device(s) power(s) up in the "Awake" state, where it is/they are ready to process commands. The Reader transmits amplitude-modulated information to the field using the Reader-to-XRA00 encoding scheme described in the Input Data Transfer from the Reader to the XRA00 (Request Frame) paragraph. On completion of the transmission, the Reader ceases the modulation and continues to apply the RF energy to power the XRA00 device(s) during the reply phase. The XRA00 device(s) communicate(s) with the Reader via backscatter modulation during this period, with the bit encoding scheme described in the Answer Frame from the XRA00 to the Reader paragraph.

Basic commands are designed to limit the amount of state information the XRA00 device(s) have/has to store between transactions. XRA00 devices on the margin of the RF field are powered unreliably and therefore cannot maintain a library of previous transactions with the Reader. Consequently, the basic command format centers on the notion of using "atomic" transactions with the XRA00 field. This means that enough information is encased in each command for XRA00 devices to respond appropriately without having to refer to previous transactions.

XRA00 State Diagram

In the state diagram shown in Figure 26., the Power Up state is entered from any other state when power is first applied, or when power is no longer sufficient for the XRA00 to operate normally as described in Figure 10.

Power Up State. The XRA00 enters the power up state on application of power, or when power falls below the level required to operate the XRA00 internal logic. When power becomes acceptable for operation, the XRA00 moves to the Awake state.

Awake State. In the Awake state, the XRA00 interprets commands. It reacts to the Reader Request Frame and parameters and switches to the appropriate state. The Awake State is entered from the Power Up State but can also be entered from the Asleep State on receipt of a valid Talk Command.

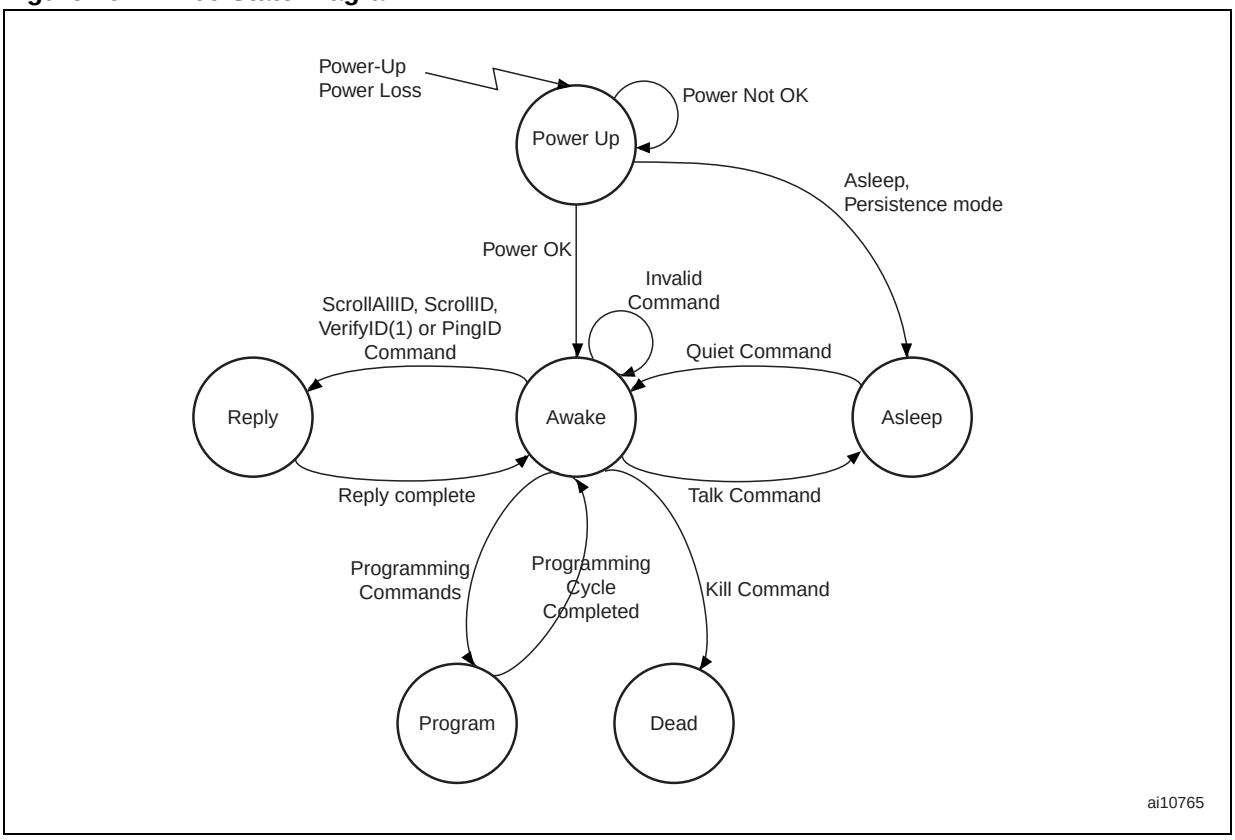
Reply State. The XRA00 switches to the Reply state when, after receiving a valid Request Frame, it has to generate a response. On completion of the Answer Frame, the XRA00 returns to the Awake State.

Asleep State. The XRA00 switches from the Awake state to the Asleep state on receipt of the Quiet Command. In the Asleep state, the XRA00 will only respond to the Talk command. Other commands are ignored.

If power is removed from the XRA00, the device enters the Persistence mode which allows it to switch back to the Asleep state when the device is powered up again.

Dead State. The XRA00 enters the Dead state on receipt of a valid Kill command with the correct Destruct Code sequence. In the Dead State the XRA00 is Erased and does not provide valid ePC data to the Reader.

Figure 26. XRA00 State Diagram



GENERAL COMMAND FORMAT

The XRA00 is expected to have limited oscillator (PLL) stability. In the Request Frame format, the Reader provides a serie of pulses to synchronize the XRA00's internal oscillator at the beginning of each transaction. Answer Frames from the XRA00 are structured such that the Reader can interpret the information transmitted at whatever clock rate the XRA00 is able to provide. This scheme is similar in concept to auto-synchronization schemes used in magnetic card or barcode Readers.

Two classes of Request Frames are provided:

- Basic Commands: they provide XRA00 identification, sorting, inventory, etc. when XRA00s are placed on goods in the supply chain.
- Programing Commands: they support XRA00 data initialization and programming by the final tag user prior to the entry of the tagged items in the supply chain.

READER COMMAND STRUCTURE - (REQUEST FRAME COMMAND FORMAT)

The format of a basic command from the Reader to the XRA00 is composed of 7 fields and 5 pieces of parity information as shown below:

[SPINUP][SOF][CMD][P1][PTR][P2][LEN][P3] [VALUE][P4][P5][EOF]

The Reader transmits the SPINUP field first, and the EOF field is transmitted last. Within each field, the LSB is transmitted first. The field definitions are given in Table 5.

Programming commands have the same format as basic commands (see Table 5.), except for a few additional pulses (see Figure 34.) for an example of a programming command).

Table 5. Request Frame Command Field Definitions

Command Field	Number of bits	Field Description
[SPINUP]	20	Every Basic command is prefixed by a series of logical zeros (‘0’) for XRA00 timing. The synchronization circuitry on the XRA00 uses this part of the message to establish its onboard timing for reading/decoding messages and clocking subsequent replies to the Reader.
[SOF]	1	Start of Frame indicator. A logical one (‘1’)
[CMD]	8	8-bit field that specifies the command being sent to the XRA00 devices. (See Basic Command Encoding below.) With 8 bits there could be up to 256 commands. The XRA00 command set only has six commands, the remaining address space is reserved.
[$P_{1]}$	1	Odd Parity of the [CMD] field data.
[PTR]	8	8-bits - Pointer to a location (or bit index) in the XRA00 address range. The bit index starts at the LSB and works up. [PTR] is the starting point for XRA00 devices to attempt a match with data specified in the [VALUE] field. (Defined below.) The [PTR] field ranges from 0 to 255.
[P2]	1	Odd Parity of the [PTR] field data.
[LEN]	8	8-bits - Equal to the length of the data being sent in the [VALUE] field. (Defined below). The [LEN] Field is always greater than zero.
[P3]	1	Odd Parity of the [LEN] field data.
[VALUE]	Variable	1 to 96 bits of data for XRA00 devices. In PingID, ScrollID, Quiet, or Kill commands, this is the data that the XRA00 will attempt to match against its own address. The first bit received by the XRA00 in the [VALUE] field will be compared to the XRA00 memory at the location contained in the [PTR] field.
[P4]	1	Odd Parity of the [VALUE] field data.
[P5]	1	Odd Parity of all of the Parity fields.
[EOF]	1	End of Frame indicator. A logical one (‘1’).

Command Encoding

For encoding the two sets of commands, Basic and Programming, are also distinguished. Table 6. shows how Basic Commands are encoded while Table 7. shows the encoding of Programming Commands.

Table 6. Basic Command Encoding

Basic Commands [CMD]	8-Bit Pattern Hex MSB <- LSB	8-Bit Pattern Binary MSB <- LSB	Reply from XRA00
SCROLLID	0x01	$0000\ 0001_b$	“ScrollID Reply”
QUIET	0x02	$0000\ 0010_b$	None
KILL	0x04	$0000\ 0100_b$	None
PINGID	0x08	$0000\ 1000_b$	“PingID Reply”
TALK	0x10	$0001\ 0000_b$	None
SCROLLALLID	0x34	$0011\ 0100_b$	“ScrollID Reply”

Table 7. Programming Command Encoding

Programming Commands [CMD]	8-Bit Pattern Hex MSB <- LSB	8-Bit Pattern Binary MSB <- LSB	Reply from XRA00
ERASEID	0x32	$0011\ 0010_b$	None
PROGRAMID	0x31	$0011\ 0001_b$	None
VERIFYID	0x38	$0011\ 1000_b$	“ScrollID Reply”

BASIC COMMANDS - OVERVIEW

The XRA00 provides six Basic commands, described in the following paragraphs.

ScrollID

The ScrollID command is a Basic command that gives rise to a response from the XRA00.

When the ScrollID command is issued, the XRA00 responds if the data sent by the Reader in the [VALUE] field matches the XRA00's internal memory starting at the location specified by the [PTR] field. Data in the [VALUE] field is compared to the XRA00 memory, from the lowest to the highest address. Only XRA00 devices that match all of the bits in the [VALUE] field reply to the Reader. XRA00 devices that fail the match or fail a parity test on any of the parity bits do not modulate.

The XRA00 devices that match the data sent by the Reader reply by sending back an 8-bit preamble, a 16-bit CRC for error checking followed by the entire 96-bit ePC code.

- Any unlocked XRA00 seeing the command will reply by sending back an 8-bit preamble, 16-bit CRC and its entire 96-bit ePC code, plus the Kill code and Lock code location bits.
- Any locked XRA00 seeing the command will reply by sending back an 8-bit preamble, 16-bit CRC and its entire 96-bit ePC code.

Data sent by the Reader to the XRA00 may be of variable length. ScrollID can be used to look for specific XRA00 devices or test for the presence of specific groups of XRA00 devices in the field. Data sent by the XRA00 has a fixed length.

Example of a ScrollID Command . A Reader issues a command containing the following data:

[CMD] = 00000001_b (ScrollID)
[PTR] = 00000111_b (0x07)
[LEN] = 00001001_b (0x09)
[VALUE] = 000101101_b (0x2D)

XRA00 devices will attempt to check 9 bits of their address data, starting at bit 7, against the data specified in the [VALUE] field. XRA00 devices whose data matches respond with a ScrollID Reply.

Table 8. shows the case of three XRA00 devices. XRA00 1 and XRA00 3 respond to the command but XRA00 2 does not. Underlined bits in XRA00 memory are compared with the [VALUE] data. Here, bits 7 through 15 are compared.

The XRA00 devices start by modulating the lowest memory address data bit onward up to the highest memory address data bit. This means that in Table 8., modulation is from right to left.

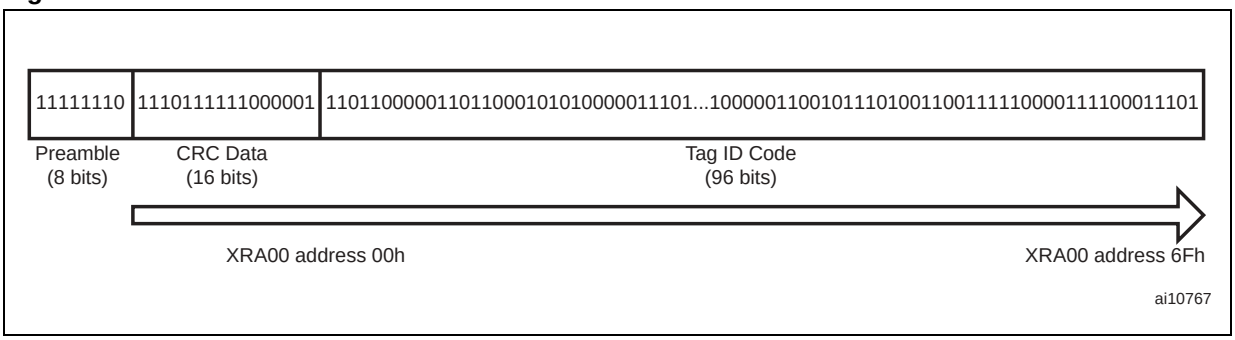
Table 8. Example of a ScrollID Operation

	XRA00 ID Code/Bit Number	XRA00 responds to ScrollID command
	Towards Highest Address Bit ... Lowest Address Bit	
Bit Number	...32109876543210987 6543210	-
XRA00 1 ID	...01000100000101101 1101010$_b$	YES
XRA00 2 ID	...10011110000100101 0010010$_b$	NO (bit 10 fails to match)
XRA00 3 ID	...10110101000101101 1110111$_b$	YES

ScrollID Answer Frame Description

The XRA00 devices that respond to a ScrollID command reply by modulating an eight bit preamble (11111110) followed by a 16-bit CRC and the entire XRA00 96-bit ePC code as shown in Figure 27. The XRA00 devices start by modulating from the lowest to the highest memory address. The XRA00 ScrollID Answer Frame structure is given in Figure 27. The 16-bit CRC data contained in the ScrollID Answer Frame is calculated accordingly and stored into the XRA00 memory during the XRA00 programming process.

Figure 27. ScrollID Answer Frame Structure



ScrollAllID

The ScrollAllID command is a Basic command that gives rise to a response from the XRA00.

When this command is sent, the [VALUE], [PTR] and [LEN] fields are ignored by the XRA00. This command is similar to the ScrollID command described above, but for the discrimination.

- Any unlocked XRA00 seeing the command will reply by sending back an 8-bit preamble, 16-bit CRC and its entire 96-bit ePC code, as well as the Kill code and Lock code location bits.
- Any locked XRA00 seeing the command will reply by sending back an 8-bit preamble, 16-bit CRC and its entire 96-bit ePC code.

The XRA00 devices start by modulating the lowest memory address bit onward up to the highest memory address bit.

Example of a ScrollAllID Command. A Reader issues a command containing the following data:

[CMD] = 00110100_b (ScrollAllID)
[PTR] = 00000111_b (0x07)
[LEN] = 00001001_b (0x09)
[VALUE] = 000101101_b (0x2D)

The XRA00 devices will ignore all the field contents. Even though a data check takes place the results of the check are ignored and all XRA00s that receive the ScrollAllID command respond with a ScrollID Reply.

In Table 9., XRA00 devices 1, 2 and 3 respond to the command. Underlined bits in XRA00 memory are compared with the [VALUE] data but the result is not used.

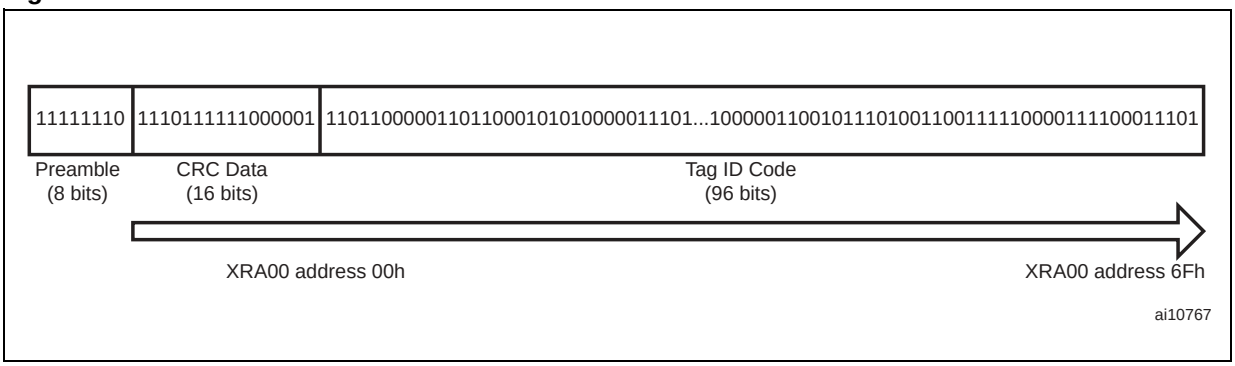
Table 9. Example of a ScrollAllID Operation

	XRA00 ID Code/Bit Number	XRA00 respond to ScrollAllID command
	Towards Highest Address Bit ... Lowest Address Bit	
Bit Number	...32109876543210987654321 0$_b$	-
XRA00 1 ID	...01000100000101101 1101010$_b$	YES
XRA00 2 ID	...10011110000100101 0010010$_b$	YES (even though bit 10 fails to match)
XRA00 3 ID	...10110101000101101 1110111$_b$	YES

ScrollAllID Answer Frame Description

XRA00 devices that respond to a ScrollAllID command reply by modulating an eight bit preamble (7Fh) followed by a 16-bit CRC and the entire XRA00 96-bit ePC code. The XRA00 devices start by modulating the lowest memory address data bit onward up to the highest memory address data bit. The XRA00 ScrollAllID Answer Frame structure is given in Figure 28. The 16-bit CRC data contained in the ScrollAllID Answer Frame is calculated accordingly and stored into the XRA00 memory during the XRA00 programming process.

Figure 28. ScrollAllID Answer Frame Structure



Kill

The Kill command is a Basic command that gives rise to an invalid response from the XRA00 to the ePC Reader queries.

XRA00 devices whose data starting at the location specified by the [PTR] field (must be cleared to '0') matches the entire [VALUE] field sent by the Reader (that is, the 16-bit CRC, 96-bit ePC code and an 8-bit Kill Code) are erased and do not provide valid ePC data to the Reader.

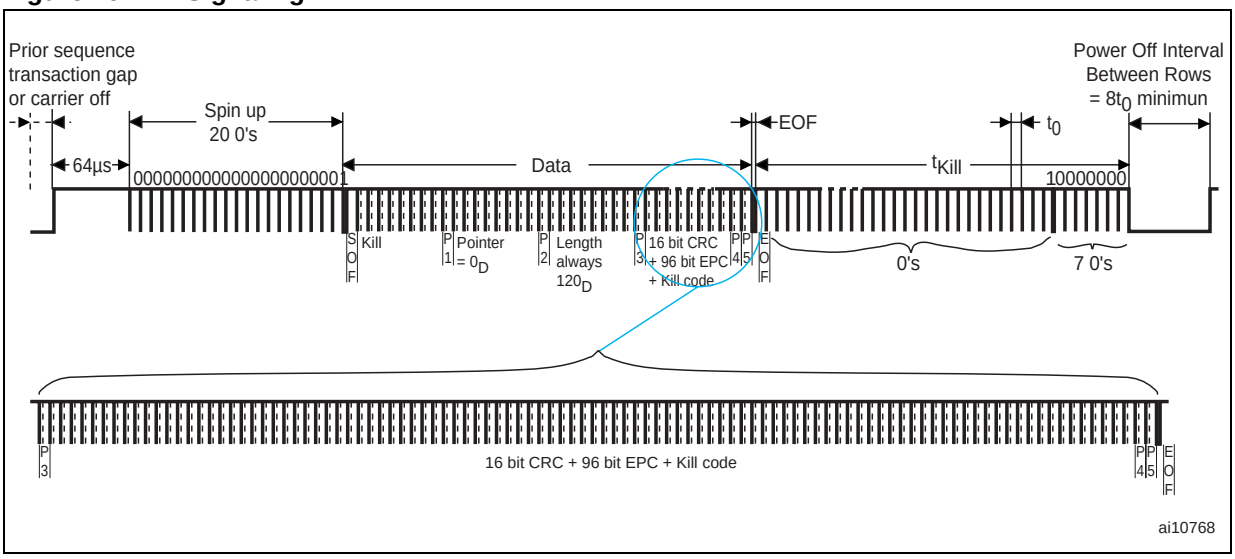
Data in the [VALUE] field is compared to XRA00 memory, from the lowest to the highest XRA00 memory address. XRA00 devices whose data do not match or that fail a parity test on any of the parity bits enter the Persistence mode.

- Killing a XRA00 can be done whether the XRA00 is locked or not, assuming that the correct Kill Code is issued during the instruction
- The Kill Code can be 00h

The time required to Kill a XRA00 is t_{Kill} (see Table 4., XRA00 Backscattered Answer Modulation Parameters for timings). It is anticipated that the Kill command will require higher field strengths from the Reader, and will therefore be a short-range operation.

The Reader to XRA00 Request Frame for a Kill command is similar to the Request Frame for a EraseID or ProgramID command.

Figure 29. Kill Signaling



PingID

The PingID command is a Basic command that gives rise to a response from the XRA00.

When the command is sent, the XRA00 will respond if the data sent by the Reader in the [VALUE] field matches the data in the XRA00's internal memory starting at the location specified by the [PTR] field. Data in the [VALUE] field is compared to the XRA00 memory, from the lowest to the highest memory address. XRA00 devices whose data matches all of the bits in the [VALUE] field will reply to the Reader. XRA00 devices whose data does not match or that fail a parity test on any of the parity bits will not modulate.

The PingID command is used as part of a multi-XRA00 anti-collision algorithm described in detail hereafter.

XRA00 devices that match the data sent by the Reader respond with 8 address bits, from a point designated by two parameters supplied by the Reader, in increasing address order.

Each XRA00 response is placed in one of 8 Bin Response Windows delineated by BIN pulses sent by the Reader.

Example of a PingID Command. A Reader issues a PingID command containing the following data:

[CMD] = 00001000_b (PingID)
[PTR] = 00000111_b (0x07)
[LEN] = 00001001_b (0x09)
[VALUE] = 000101101_b (0x2D)

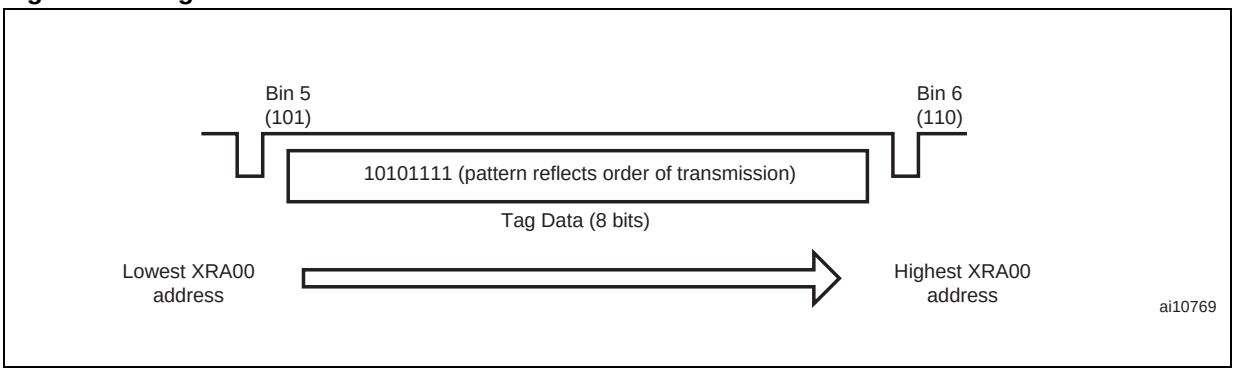
The XRA00 devices will attempt to check 9 bits of their address data, starting at bit 7 against the data specified in the [VALUE] field.

In the example shown in Table 10., the underlined bits in the XRA00 ID code are compared with the [VALUE] data sent by the Reader. Bits shown in Italic are modulated and returned to the Reader during one of the Bin Response Windows. The lowest 3 bits of the response determine the response bin number.

Table 10. Example of PingID Operation

	XRA00 ID Code/Bit Position	XRA00 responds to PingID command	Bin for response	8-Bit response
	Towards Highest Address Bit ... Lowest Address Bit			MSB LSB
Bit Number	...32109876543210987 6543210	-	-	-
XRA00 1 ID	...*01000100*00010110 1101010$_b$	YES	Bin 4 (100_b)	01000100_b
XRA00 2 ID	...10011110*00010*0*101*0010010$_b$	NO (bit 10 does not match)	-	-
XRA00 3 ID	...*11110101*00010110 1110110$_b$	YES	Bin 5 (101_b)	11110101_b
XRA00 4 ID	...*10110000*00010110 1110111$_b$	YES	Bin 0 (000_b)	10110000_b

Figure 30. PingID Answer Frame Structure for XRA00 3



PingID Answer Frame

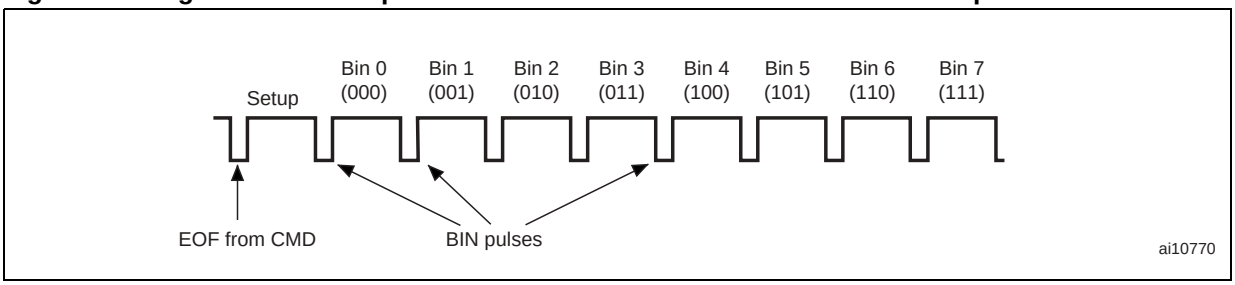
The PingID command is used in the anti-collision algorithm. This command requires that the XRA00 devices that match the data sent by the Reader reply with 8 modulated data bits in one of 8 Bin Re-

sponse Windows delineated by BIN pulses from the Reader after a Setup time.

The 3 bits of XRA00 memory that come immediately after the matched data determine the particular Bin Response Window for an XRA00 reply. XRA00 devices where these 3 bits are equal to '000' respond in the first Bin Response Window, XRA00 devices where the 3 bits are equal to '001' reply in the second Bin Response Window... XRA00 devices where the 3 bits are equal to '111' respond in the eighth Bin Response Window. These Bin Response Window are also called "bins" and numbered from 0 through to 7 as shown in Figure 31.

As described in the Ping Reply Bin Collapse paragraph, the Reader may shorten a BIn Response Window if no tag answer is detected.

Figure 31. PingID Answer Response Period - Reader Modulations Define Response Bins



Quiet

XRA00 devices that match the data sent by the Reader enter the Asleep state where they no longer respond to Reader commands. They remain in the Asleep state until they receive the appropriate Talk command or after the Persistance mode time limit is exceeded (even if power has been removed from the XRA00).

Example of a Quiet Command. A Reader issues a Quiet command containing the following data:

[CMD] = 00000010_b (Quiet)
[PTR] = 00000111_b (x07)
[LEN] = 00001001_b (0x09)
[VALUE] = 000101101_b (0x2D)

XRA00 devices will attempt to check 9 bits of their address data, starting from bit 7, against the data specified in the [VALUE] field. XRA00 devices whose data matches enter the Asleep state and remain in this state.

Once in the Asleep state the XRA00 devices will fail to respond to any command until they receive a Talk command or the Persistence mode limit time is exceeded.

The XRA00 devices do not return any response to the Quiet command.

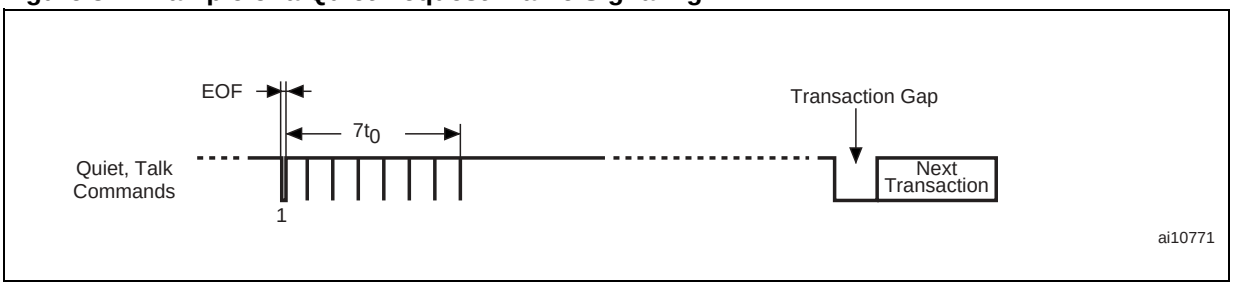
In the example illustrated in Table 11., the underlined XRA00 memory bits are compared with the [VALUE] data sent by the Reader.

After issuing the Quiet command, the Reader must transmit seven 0's after the EOF for the XRA00 to execute the Quiet command. Once the seven 0's have been sent, the Reader is allowed to start a new transaction.

Table 11. Example of a Quiet Operation

	XRA00 ID Code/Bit Position	XRA00 execute Quiet command and become inactive
	Towards Highest Address Bit Lowest Address Bit	
Bit Number	...32109876543210987 6543210	-
XRA00 1 ID	...01000100000101101 1101010$_b$	YES
XRA00 2 ID	...10011110000100101 0010010$_b$	NO (bit 10 does not match)
XRA00 3 ID	...10110101000101101 1110110$_b$	YES
XRA00 4 ID	...10110000000101101 1111011$_b$	YES

Figure 32. Example of a Quiet Request Frame Signaling



Talk

XRA00 devices that match the data sent by the Reader return to the Awake state, where they will respond to commands from the Reader.

XRA00 devices inactivated by the Quiet command can be reactivated by the Talk command.

The Talk command follows the same rules as the Quiet, PingID and ScrollID commands for the selection of the XRA00 devices. An individual XRA00 or a group of XRA00 devices can be brought out of the Asleep state, as required.

Example Talk Command. A Reader issues a Talk command containing the following data:

[CMD] = 00110010_b (Talk)

[PTR] = 00000111_b (0x07)

[LEN] = 00001001_b (0x09)

[VALUE] = 000101101_b (0x2D)

The XRA00 devices will attempt to check 9 bits of their address data, starting from bit 7, against the data specified in the [VALUE] field. The XRA00 devices with matching data revert from the Asleep to the Awake state thus becoming responsive to all subsequent Reader commands until a new Quiet command is received.

The XRA00 devices do not return any response to the Talk command.

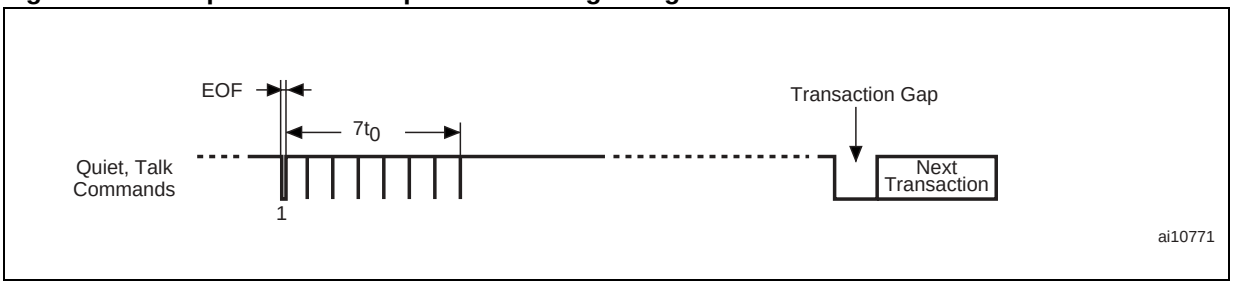
In the example illustrated in Table 12., the underlined XRA00 memory bits are compared with the [VALUE] data sent by the Reader.

After issuing the Talk command the Reader must transmit seven 0's after the EOF for the XRA00 to execute the Talk Command. Once the seven 0's have been sent, the Reader must immediately issue a transaction gap.

Table 12. Example of a Talk Operation

	XRA00 ID Code/Bit Position	XRA00 executes the Talk command and enters the Awake state
	Towards Highest Address Bit ... Lowest Address Bit	
Bit Number	...32109876543210987 6543210	-
XRA00 1 ID	...01000100000101101 1101010$_b$	YES
XRA00 2 ID	...10011110000100101 0010010$_b$	NO (bit 10 does not match)
XRA00 3 ID	...10110101000101101 1110110$_b$	YES
XRA00 4 ID	...10110000000101101 1110111$_b$	YES

Figure 33. Example of aTalk Request Frame Signaling



PROGRAMMING COMMANDS - OVERVIEW

Programming commands use the same command structure and field definitions as the Basic commands, but are issued only by an XRA00 programmer.

An XRA00 programmer may be similar to a Reader, except that it can execute Programming commands in addition to Basic commands. Programming commands are used to program the contents of the XRA00 non-volatille memory, and to verify these contents before locking them. All Programming commands are disabled once the manufacturer has locked the XRA00 data contents. The programming range is approximately 25% of the maximum read range. The programming distance depends on the tag antenna design, tag materials, programmer antenna design, RF power level and system configuration.

VerifyID

The VerifyID command is used to examine the contents of a memory block as part of a programming cycle in order to allow the manufacturer programmer to verify that the entire memory block has been programmed correctly into the XRA00. XRA00 devices that have been LOCKED will not answer to the VerifyID command. The VerifyID command addresses all bits in the XRA00 memory that are transmited to the programmer in the same Answer Frame format as the ScrollAllID Reply.

EraseID

The EraseID command resets all bits in the XRA00 to the value "0". This command is a bulk erase of the entire memory array. The EraseID operation is normally executed prior to the ProgramID command. The EraseID command is not executed on XRA00 devices that have been LOCKED. The data sent by the Programmer in the [PTR] and [VAL] fields are not used by the XRA00 and should be set to "0". The [LEN] field should be set to the value “1”, and the [VAL] field should contain a single "0". Upon receipt of a valid EraseID command, the XRA00 executes the appropriate internal timing sequences required to erase the memory.

See Figure 34. for the EraseID command signaling sheme.

ProgramID

The XRA00 is programmed 16 bits at a time. Programming is only allowed if the XRA00 is not locked. The data is sent to the XRA00 using the ProgramID command. The [PTR] field contains the memory row address to be programmed and the [VAL] field contains the 16 bits of data to be programmed. The [PTR] field value must be set as specified in Table 13.

See Figure 34. for the ProgramID command signaling sheme.

The [LEN] field must be set to the value 16 (00010000_b), indicating that 16 bits are programmed.

Upon receipt of a valid ProgramID command, the XRA00 executes the appropriate internal timing sequences required to program the memory.

Table 13. Programming Row Selection

[PTR] Value	[PTR] Value MSB LSB	Row to be Programmed
00_D	00000000_b	row 0, bits 0-15
16_D	00010000_b	row 1, bits 16-31
32_D	00100000_b	row 2, bits 32-47
48_D	00110000_b	row 3, bits 48-63
64_D	01000000_b	row 4, bits 64-79
80_D	01010000_b	row 5, bits 80-95
96_D	01100000_b	row 6, bits 96-111
112_D	01110000_b	row 7, bits 112-127

Lock Function

The Lock function is implemented by programming a specific value into the lock bits of the XRA00, using the ProgramID command. In order to lock the XRA00, the 8 upper bits of the row 7 must be programmed with the value A5h, as shown in Table 14. and Table 15.

If a value different from A5h is programmed in the 8 upper bits of the row 7, the tag in NOT LOCKED, and the XRA00 will return this value in response to any ScrollID, ScrollAllID or Verify command.

Table 14. Row 7 of an Unlocked or Erased Memory

Row 7	Lock Bit bit8bit 1								Kill Code bit8bit1							
bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15. Row 7 of a Locked Memory (Showing Lock Code A5h)

Row 7	Lock Bit bit8bit 1								Kill Code bit8bit1							
bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Value	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0

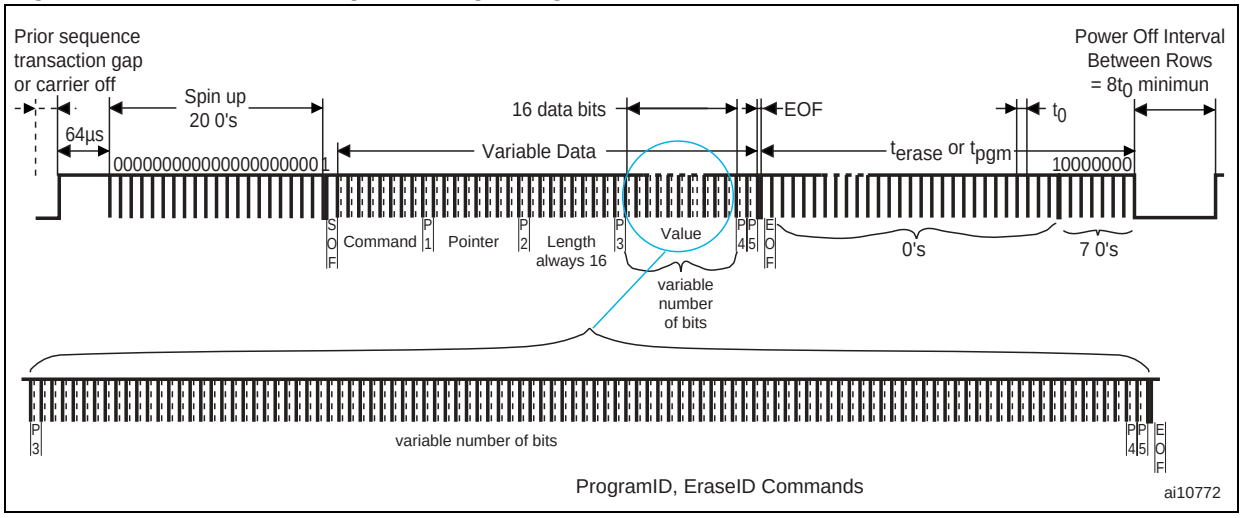
EraseID and ProgramID Timing

The time required to erase or program a XRA00 is t_{erase} and t_{pgm}, respectively. See Table 4., XRA00 Backscattered Answer Modulation Parameters for values.

The Reader to XRA00 Request Frame is much like the Basic Command frame. The differences between the two are listed below:

- The Programmer must send 0's after the [EOF] for the duration of the program or erase time, t_{pgm} or t_{erase}.
- The ProgramID and EraseID operations are terminated by a "1" at the end of t_{erase} or t_{pgm}.
- The Programmer must transmit seven 0's after the terminating "1" to allow the XRA00 to perform an orderly shutdown of the erase/ program sequence.
- Transmission of subsequent programming commands must be preceded by an XRA00 carrier off interval of at least 8 x t_0.

Figure 34. EraseID and ProgramID Signaling



ANTI-COLLISION ALGORITHM

The PingID command divides a population of XRA00 devices into eight sub-populations based on their ID code by binning XRA00 responses into eight separate time slices, or Bin Response Windows. This binning provides the basis for an anti-collision algorithm that probes the binary ID code three bits at a time. Individual XRA00 devices can be isolated from large populations in the field of the Reader by issuing multiple PingID commands to the field, analyzing the responses and eventually issuing the appropriate ScrollID command.

Figure 35. is a binary tree representation of the first four LSBs in the XRA00 address space. Although only the four first levels are shown, the binary tree structure applies to the entire XRA00 ID code (96 bits for a Class-1b XRA00).

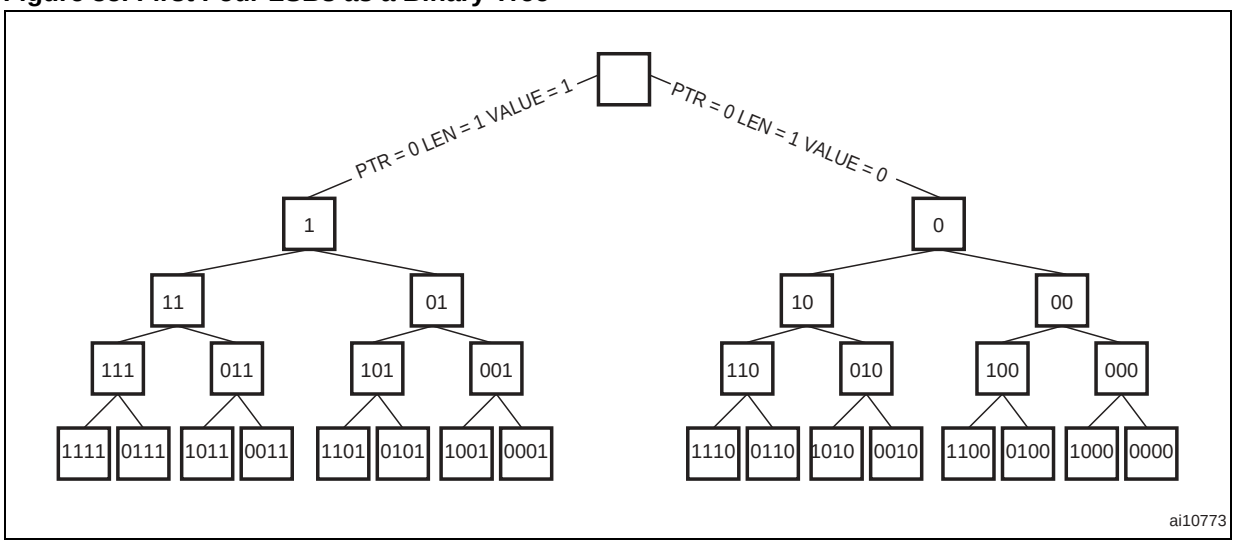
A PingID command with [PTR]=0, [LEN]=1 and [VALUE]=0 will probe the right half of this tree (the '0' branch) through the first four bits of the XRA00 memory.

Similarly, a PingID command with [PTR]=0, [LEN]=1 and [VALUE]=1 will probe the left half of this tree (the '1' branch) through the first four bits of the XRA00 memory.

For the PingID command with [PTR]=0, [LEN]=1 and [VALUE]=0, XRA00 devices whose LSBs are 0000_b respond in bin 0, XRA00 devices whose LSBs are 0010_b respond in bin 1... and XRA00 devices whose LSBs are 1110_b respond in bin 7. Readers can look for backscatter modulation from the XRA00 devices in each of the bins and learn about the XRA00 population even if collisions make reading the 8 bits of data sent by the XRA00 devices difficult.

The presence of backscatter in a given bin merely indicates that one or more XRA00 device(s) match(es) the query. The bin number tells the Reader what the next three MSBs of the XRA00 addresses will be. The bin contents also indicate the next 5 bits of the responding XRA00 devices.

Figure 35. First Four LSBs as a Binary Tree



Anti-Collision Example

Consider two XRA00 devices having their lowest address programmed with 0111_b and 1011_b, respectively.

Query 1

[CMD] = 00001000_b(PingID)
[PTR] = 00000000_b(0x00)
[LEN] = 00000001_b(0x01)
[VALUE] = 1_b(1)

This command probes the left half of the tree shown in Figure 35. The [VALUE] field of 1, matches the first bit of both XRA00 devices in the example ($011\mathbf{1}_b$ and $101\mathbf{1}_b$), so that they will both respond.

During the reply interval, the XRA00 devices modulate the next 8 bits of their address data that come just after the matched portion on the higher address side. The bin in which they modulate is determined by the three LSBs of the data they modulate. At the Reader, backscatter modulation is observed in bins 3 (011_b) and 5 (101_b) (as shown in Figure 36.). Since multiple XRA00 devices can modulate in each of these bins, contention may be observed but the Reader knows that there are two distinct populations of XRA00 devices present whose first four LSBs are 0111_b and 1011_b, respectively.

Using this information, the Reader may issue a second PingID command to explore the population of XRA00 devices in bin 3, reserving the XRA00 devices detected in bin 5 for later analysis:

Query 2

[CMD] = 00001000_b(PingID)
[PTR] = 00000000_b(0)
[LEN] = 00000100_b(4)
[VALUE] = 0111_b(7)

This command explores 3 bits farther into the tree towards the highest memory location from the memory address containing the bits 0111_b. In Figure 37., the bold borders show the branches that contain the XRA00 devices. The two branches shown in the second half of the drawing contain groups of XRA00 devices that match Query 2. These are the same XRA00 devices that responded to the first query in bin 3.

In this new query, the XRA00 modulation during the reply interval will take place in bins 1 (response 0010111_b), 6 (response 1100111_b) and 7 (response 1110111_b) as shown in Figure 38. and in bold in Figure 37. The Reader knows 7 address bits of these XRA00 devices and at least 4 bits of information concerning the other XRA00 branch affected by Query 1 but reserved for later analysis.

Although it is not the fastest way to isolate and identify XRA00 devices, the Reader may continue with this method and use the PingID command to follow a branch through the XRA00 ID space until it has explored the entire XRA00 address and 16-bit CRC of the XRA00 address.

The recommended way to perform an analysis of a population of XRA00 devices is to take advantage of the Reader's ability to detect contention in the reply intervals. The "divide by eight" feature of the PingID command makes it possible to very quickly reduce the number of XRA00 devices replying in each bin. Simulations with populations of 100 XRA00 devices show that with random addresses, an average of less than 4 PingID commands are needed to isolate one XRA00 device. If only one XRA00 replies in a given bin, the Reader can decode the 8 bits of information sent from the XRA00 and issue a ScrollID command to that XRA00 using the [PTR] [LEN] and [VALUE] data that successfully isolated the XRA00.

Figure 36. Reader Modulations and XRA00 Backscatter During PingID Reply for Query 1

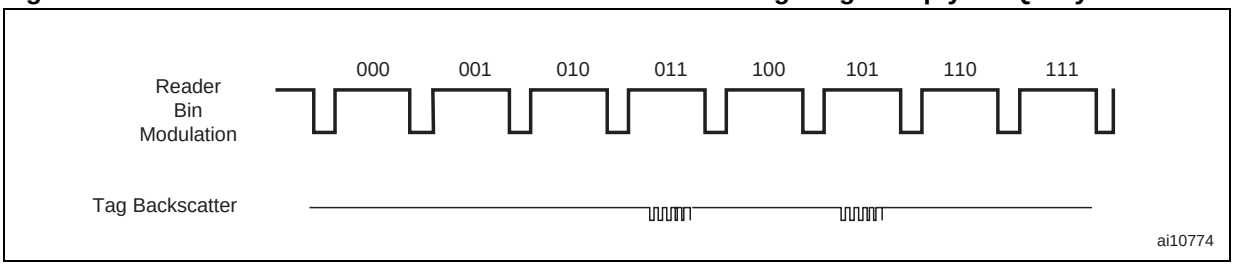


Figure 37. Query Tree for the Two PingID Sequence

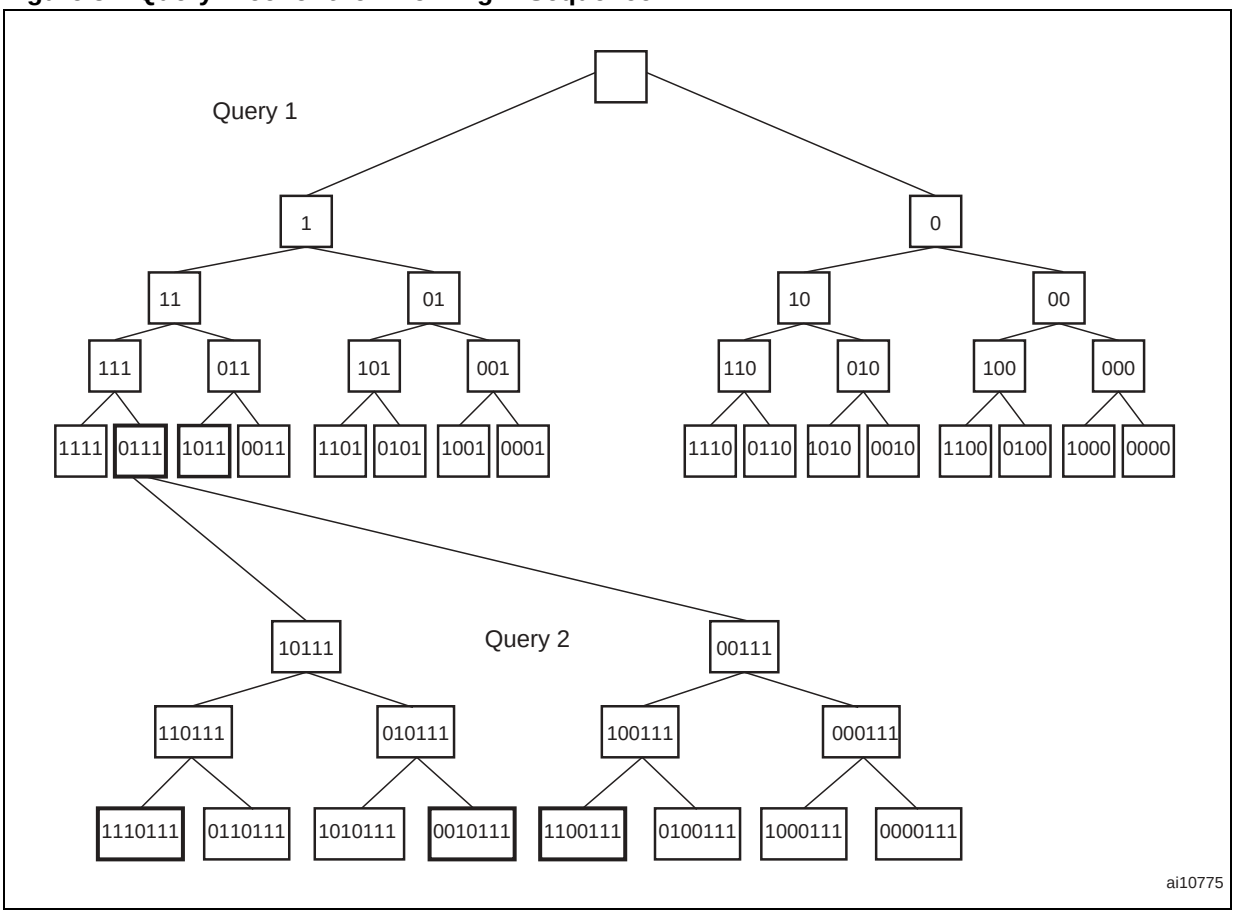
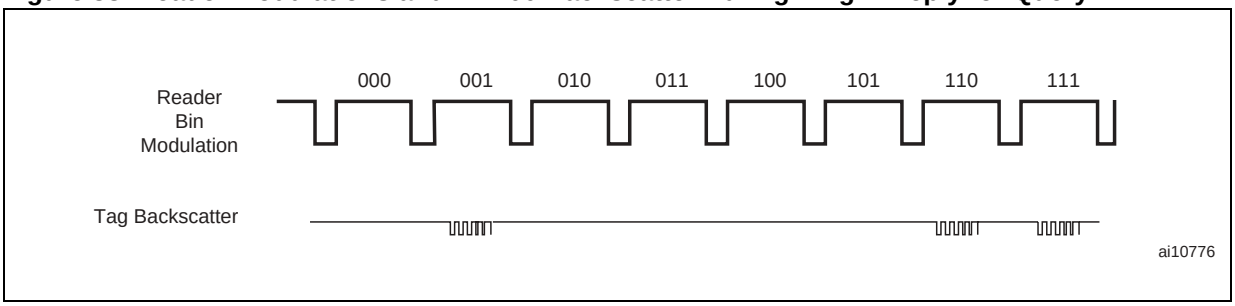


Figure 38. Reader Modulations and XRA00 **Backscatter During PingID Reply for Query 2**



ANTI-COLLISION FEATURES

Several features of this anti-collision approach deserve mention:

- Each transaction with the XRA00 field is a self-contained operation. A command - reply pair is an atomic transaction requiring no knowledge of previous events from a XRA00 for it to reply. This feature greatly enhances robustness for passive XRA00 devices in noisy environments or at marginal RF power levels.
- Related to this, the Reader maintains information about the progress through the binary tree. Branches that show XRA00 signals, but are not immediately explored may be held in memory and later examined to improve the overall throughput.
- Readers with widely varying capabilities can make use of the same protocol.
  - A sophisticated Reader that can perform contention detection within a bin can perform very rapid sorts of groups of XRA00 devices. XRA00 devices can be quickly isolated using a series of PingID commands, and then read using the ScrollID command.
  - Simple Readers without the ability to detect contention (for example, a Reader with only an analogue filter to look for "XRA00-like" modulation) can still sort and identify XRA00 devices using only the PingID command.

XRA00 IMPEDANCE PARAMETERS

The XRA00 parameters are specified in Tables 16 and 17.

Table 16. XRA00 Parameters

Symbol	Description	Conditions	Min	Max	Unit
t_{STG}	Storage Temperature	Wafer	15	25	°C
				23	months
V_{OP}	Minimum Operating voltage on the antenna	F_C = 915MHz, T = 25°C, Regulated Internal V_{DD} = 1.65V	0.5		Vrms
V_{ESD}	Electrostatic Discharge Voltage (1)	Machine Model	–50(2)	+50(2)	V
			–200(3)	+200(3)	V
		Human Body Model	–400(2)	+400(2)	V
			–2500(3)	+2500(3)	V

Note: 1. Mil. Std. 883 - Method 3015.
2. V_{ESD} values for 6-inch wafers.
3. V_{ESD} values for 8-inch wafers.

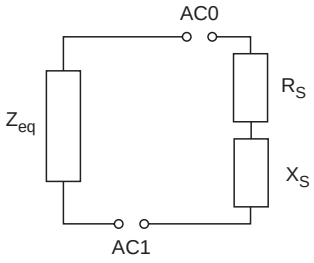
Table 17. 6-inch Wafer XRA00 Impedance Parameters

Equivalent Serial Model for 6-inch wafers (See Figure 39.)
Measurement conditions T = +25°C, Regulated Internal V_{DD} = 1.65V Typical Value Characterized only.
F_c = 868MHz, R_S = 7.4Ω, X_S = -218Ω F_c = 915MHz, R_S = 6.7Ω, X_S = -197.4Ω

Table 18. 8-inch Wafer XRA00 Impedance Parameters

Equivalent Serial Model for 8-inch wafers (See Figure 39.)
Measurement conditions T = +25°C, Regulated Internal V_{DD} = 1.65V Typical Value Characterized only.
F_c = 915MHz, R_S = 7Ω, X_S = -184Ω

Figure 39. XRA00 Input Impedance, Equivalent Serial Circuit



$Z_{eq} = R_S + jX_S$ ai10778

PART NUMBERING

Table 19. Ordering Information Scheme

Example: XRA00 - W4I / XXX

Device Type

XRA00

Delivery Form

W4I = 180µm ± 15µm unsawn Inkless wafer

SBN18I = 180µm ± 15µm Bumped and Sawn Inkless Wafer

Customer Code

XXX = Customer Code, given by STMicroelectronics

Note: Initial delivery state: devices on wafers are shipped from the factory with the memory contents cleared to all “0’s” (00h).

For a list of the available options, please see the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 20. Document Revision History

Date	Version	Revision Details
15-Dec-2004	0.1	First Issue
21-Oct-2005	2	V_{ESD} values for 8-inch wafers added to Table 16., XRA00 Parameters. Parallel model removed. Table 18., 8-inch Wafer XRA00 Impedance Parameters added.