

DATA SHEET

TDA8793

**8-bit, low-power, 3 V, 100 Msps
Analog-to-Digital Converter (ADC)**

Preliminary specification
Supersedes data of 1998 May 14
File under Integrated Circuits, IC02

1999 Oct 06

8-bit, low-power, 3 V, 100 Msp/s Analog-to-Digital Converter (ADC)

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FEATURES

- 8-bit low-power ADC (170 mW typical)
- 2.7 to 3.6 V operation
- Sampling rate up to 100 Msp/s
- Track-and-hold circuit
- CMOS/TTL compatible digital inputs and outputs
- Internal references
- Adjustable full scale range possibility with external reference
- Power-down mode; 5 mW.

GENERAL DESCRIPTION

The TDA8793 is an 8-bit low-power Analog-to-Digital Converter (ADC) which includes a track-and-hold circuit and internal references. The device converts an analog input signal, up to 100 MHz, into 8-bit binary codes at a maximum sample rate of 100 Msp/s. All digital inputs and output are TTL/CMOS compatible. A sine wave clock input signal can also be used.

The Power-down mode enables the device power consumption to be reduced to 5 mW.

APPLICATIONS

- Radio communications
- Digital data storage read channels
- Medical imaging
- Digital instrumentation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	output stages supply voltage		2.7	3.0	3.6	V
I_{CCA}	analog supply current	operating	32	40	48	mA
		standby	0	5	100	μ A
I_{CCD}	digital supply current	operating	13	16	22	mA
		standby	0	0.65	1.1	mA
I_{CCO}	output stages supply current		–	0.1	–	mA
INL	integral non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	± 0.8	tbf	LSB
DNL	differential non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	± 0.25	tbf	LSB
$f_{CLK(max)}$	maximum clock input frequency		100	–	–	MHz
P_{tot}	total power dissipation	$V_{CC} = 3$ V	–	170	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8793HL	LQFP32	plastic low profile quad flat package; 32 leads; body $5 \times 5 \times 1.4$ mm	SOT401-1

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BLOCK DIAGRAM

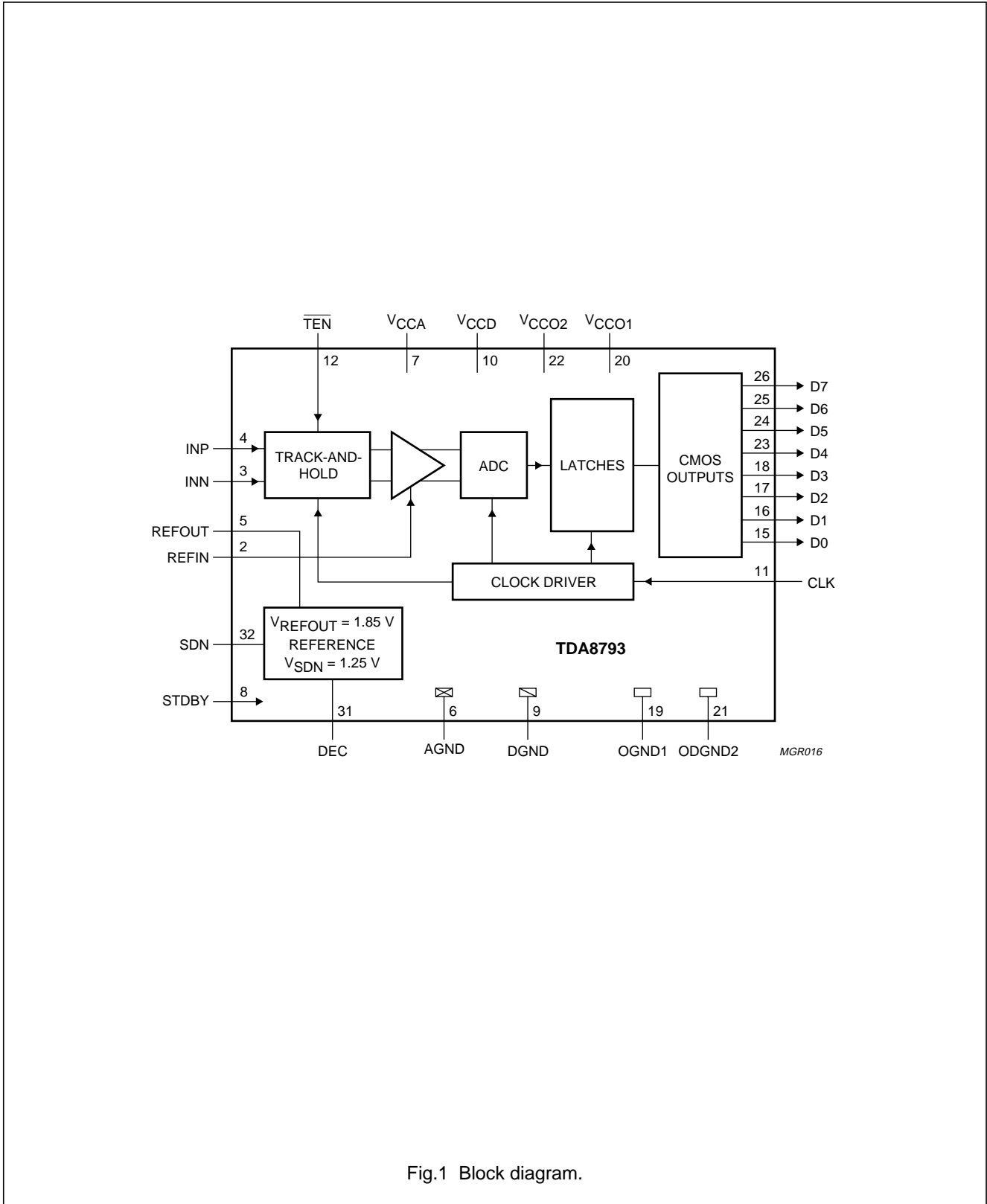


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
REFIN	2	reference input for ADC
INN	3	negative input
INP	4	positive input
REFOUT	5	reference for AC coupling
AGND	6	analog ground
V _{CCA}	7	analog supply voltage
STDBY	8	standby mode input
DGND	9	digital ground
V _{CCD}	10	digital supply voltage
CLK	11	clock input
TEN	12	track enable input (active LOW)
n.c.	13	not connected
n.c.	14	not connected
D0	15	data output bit 0 (LSB)
D1	16	data output bit 1

SYMBOL	PIN	DESCRIPTION
D2	17	data output bit 2
D3	18	data output bit 3
OGND1	19	output ground 1
V _{CCO1}	20	output supply voltage 1
OGND2	21	output ground 2
V _{CCO2}	22	output supply voltage 2
D4	23	data output bit 4
D5	24	data output bit 5
D6	25	data output bit 6
D7	26	data output bit 7 (MSB)
n.c.	27	not connected
n.c.	28	not connected
n.c.	29	not connected
n.c.	30	not connected
DEC	31	decoupling
SDN	32	stabilized decoupling node

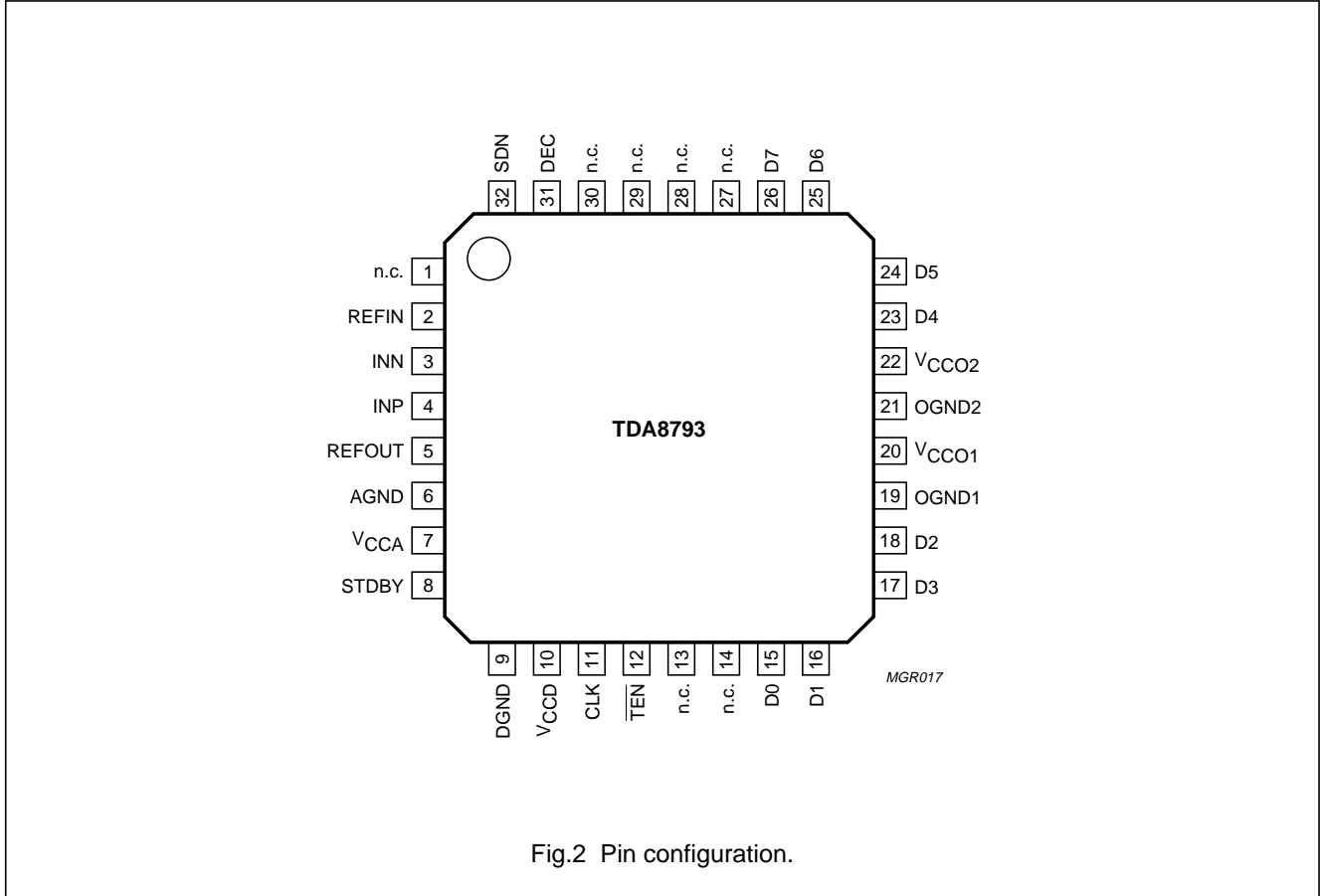


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		-0.3	+7.0	V
V_{CCD}	digital supply voltage		-0.3	+7.0	V
V_{CCO}	output stages supply voltage		-0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		-1.0	+1.0	V
	V_{CCO} and V_{CCD}		-1.0	+1.0	V
	V_{CCA} and V_{CCO}		-1.0	+1.0	V
$V_{INP, INN}$	input voltage range	referenced to AGND	-0.3	+7.0	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	-	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	94	K/W

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CHARACTERISTICS

$V_{CCA} = V_7$ to $V_6 = 2.7$ to 3.6 V; $V_{CCD} = V_{10}$ to $V_9 = 2.7$ to 3.6 V; $V_{CCO} = V_{20}$ (or V_{22}) to V_{19} (or V_{21}) = 2.7 to 3.6 V; AGND to DGND and OGND shorted together; V_{CCA} to $V_{CCD} = -0.15$ to $+0.15$ V; V_{CCD} to $V_{CCO} = -0.15$ to $+0.15$ V; V_{CCA} to $V_{CCO} = -0.15$ to $+0.15$ V; $T_{amb} = 0$ to 70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$ V and $T_{amb} = 25$ °C; single-ended input; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	output stages supply voltage		2.7	3.0	3.6	V
I_{CCA}	analog supply current		32	40	48	mA
I_{CCD}	digital supply current		13	16	22	mA
I_{CCO}	output stages supply current	$f_i = \text{ramp input}$	–	0.1	tbf	mA
		$f_i = 20$ MHz	–	4	tbf	mA
Internal reference (pin SDN); note 1						
V_{ref}	reference voltage		1.21	1.25	1.29	V
V_{reg}	line regulation voltage	$2.7 < V_{CCA} < 3.6$ V	–	0.4	3	mV
TC	temperature coefficient		–	18	–	ppm/K
I_L	load current		–1	–	–	mA
Internal reference (pin REFOUT)						
$V_{o(ref)}$	reference voltage		1.76	1.82	1.88	V
$V_{o(reg)}$	line regulation voltage	$2.7 < V_{CCA} < 3.6$ V	–	1.5	4	mV
TC	temperature coefficient		–	18	–	ppm/K
I_L	load current		–1	–	–	mA
Adjustable full scale input (pin REFIN); see Figs 3, 4, and 7						
I_{ref}	input current	$V_{REFIN} = 1.25$ V	–	–0.87	–	mA
Clock input (pin CLK); note 2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{CLK} = 0$	–2	–	+2	μ A
I_{IH}	HIGH-level input current	$V_{CLK} = V_{CCD}$	–	–	5	μ A
t_r	clock rise time		0.75	–	tbf	ns
t_f	clock fall time		0.75	–	tbf	ns
Z_i	input impedance	$f_{CLK} = 100$ MHz	–	32	–	k Ω
C_i	input capacitance	$f_{CLK} = 100$ MHz	–	2	–	pF
Standby input (pin STDBY); see Table 1						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{STDBY} = 0$	–5	–	–	μ A
I_{IH}	HIGH-level input current	$V_{STDBY} = V_{CCD}$	–	–	5	μ A

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Track enable input (pin $\overline{\text{TEN}}$); see Table 2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{TEN} = 0$	–5	–	–	μA
I_{IH}	HIGH-level input current	$V_{TEN} = V_{CCD}$	–	–	5	μA
Inputs (pins INP and INN); analog input voltage referenced to AGND; $V_{REFIN} = 1.27\text{ V}$; see Table 3						
$V_{i(p-p)}$	input voltage range (peak-to-peak value)	$V_i = V_{INP} - V_{INN}$; $T_{amb} = 25\text{ }^\circ\text{C}$	0.90	0.97	1.040	V
ΔT_{CI}	input voltage range drift		–	0.5	–	mV/K
$V_{i(os)}$	input offset voltage	output code = 127	–25	–	+25	mV
Z_i	input impedance	$f_{INP} = 50\text{ MHz}$	–	90	–	$k\Omega$
C_i	input capacitance	$f_{INP} = 50\text{ MHz}$	–	2	–	pF
I_{IL}	LOW-level input current	$V_{INP} = V_{REFOUT} + 0.5$	–1	–	–	μA
		$V_{INP} = V_{REFOUT} - 0.5$	–1	–	–	μA
I_{IH}	HIGH-level input current	$V_{INP} = V_{REFOUT} + 0.5$	–	–	40	μA
		$V_{INP} = V_{REFOUT} - 0.5$	–	–	40	μA
Adjustable full scale range; $V_{REFIN} = 1.2\text{ to }1.35\text{ V}$; see Fig.3						
$V_{i(p-p)}$	input voltage range (peak-to-peak value)	$V_i = V_{INP} - V_{INN}$; $T_{amb} = 25\text{ }^\circ\text{C}$	–	1	–	V
Voltage controlled regulator input pin V_{REFIN} (referenced to AGND); note 3						
$V_{i(ref)}$	reference voltage		tbf	1.25	tbf	V
$I_{i(ref)}$	input current on pin V_{REFIN}		–	tbf	1.1	mA
Outputs; ADC data outputs						
V_{OL}	LOW-level output voltage	$I_O = 1\text{ mA}$	–	–	0.5	V
V_{OH}	HIGH-level output voltage	$I_O = -0.4\text{ mA}$	$V_{CCO} - 0.5$	–	V_{CCO}	V
C_L	output load capacitance		–	–	10	pF
$\delta v/\delta t$	slew rate	10% to 90%; $C_L = 10\text{ pF}$	–	1.2	–	V/ns
Switching characteristics; note 2; see Table 1						
$f_{CLK(min)}$	minimum clock frequency	track = LOW	–	–	6	MHz
$f_{CLK(max)}$	maximum clock frequency		100	–	–	MHz
$t_{W(CLKH)}$	clock pulse width HIGH		4	–	–	ns
$t_{W(CLKL)}$	clock pulse width LOW		4	–	–	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Analog signal processing; note 3; see Figs 4, 5, 6 and 7							
INL	integral non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	±0.8	tbf	LSB	
DNL	differential non-linearity	ramp input; $f_{CLK} = 2$ MHz; $V_{CCA} = V_{CCD} = 3$ V	–	±0.25	tbf	LSB	
S/N	signal-to-noise ratio (full scale)	without harmonics; $f_{CLK} = 100$ MHz					
		$f_i = 20$ MHz	42	45	–	dB	
		$f_i = 50$ MHz	–	45	–	dB	
$B_{W(-3dB)}$	–3 dB analog bandwidth		–	350	–	MHz	
THD	total harmonics distortion	$f_i = 20$ MHz	–	–56	–	dB	
		$f_i = 50$ MHz	–	–52	–	dB	
$H_{fund(FS)}$	full scale fundamental harmonics	$f_{CLK} = 100$ MHz					
		$f_i = 20$ MHz	–	–	0	dB	
		$f_i = 50$ MHz	–	–	0	dB	
$H_{D2(FS)}$	second harmonic distortion (full scale) all components included	differential inputs; $f_{CLK} = 100$ MHz	$f_i = 20$ MHz	–	66	–	dB
			$f_i = 50$ MHz	–	57	–	dB
		single-ended input; $f_{CLK} = 100$ MHz	$f_i = 20$ MHz	–	66	–	dB
			$f_i = 50$ MHz	–	55	–	dB
$H_{D3(FS)}$	third harmonic distortion (full scale) all components included	differential inputs; $f_{CLK} = 100$ MHz	$f_i = 20$ MHz	–	64	–	dB
			$f_i = 50$ MHz	–	61	–	dB
		single-ended input; $f_{CLK} = 100$ MHz	$f_i = 20$ MHz	–	64	–	dB
			$f_i = 50$ MHz	–	59	–	dB
SFDR	spurious free dynamic range	$f_{CLK} = 100$ MHz				dB	
		$f_i = 20$ MHz	–	57	–	dB	
		$f_i = 50$ MHz	–	54	–	dB	
EB	effective bits	$f_{CLK} = 100$ MHz; note 4				bits	
		$f_i = 20$ MHz	7.0	7.4	–	bits	
		$f_i = 50$ MHz	–	7.2	–	bits	
Data timing; $f_{CLK} = 100$ MHz; $C_L = 10$ pF; see Fig.8							
t_{ds}	sampling delay		–	–	1.5	ns	
t_h	output hold time		3	–	–	ns	
t_d	output delay time		–	5	8	ns	

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Notes

1. It is possible to use the reference output voltage (pin SDN) to drive other analog circuits under the limits indicated.
2. In addition to a good layout of the digital and analog grounds, it is recommended that the rise and fall times of the clock must be not less than 0.75 ns.
3. It is possible with an external reference voltage connected to REFIN pin to adjust the ADC input range. The input range variation will be fixed.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 k acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (nyquist frequency). Conversion to signal-to-noise ratio: $SINAD = 6.02 \times EB + 1.76$ dB.

Table 1 Standby selection

PIN STDBY	D0 TO D7	I _{CCA} + I _{CCD}
LOW	inactive	56 mA
HIGH	active; output logic state LOW	0.7 mA

Table 2 Track-and-hold selection

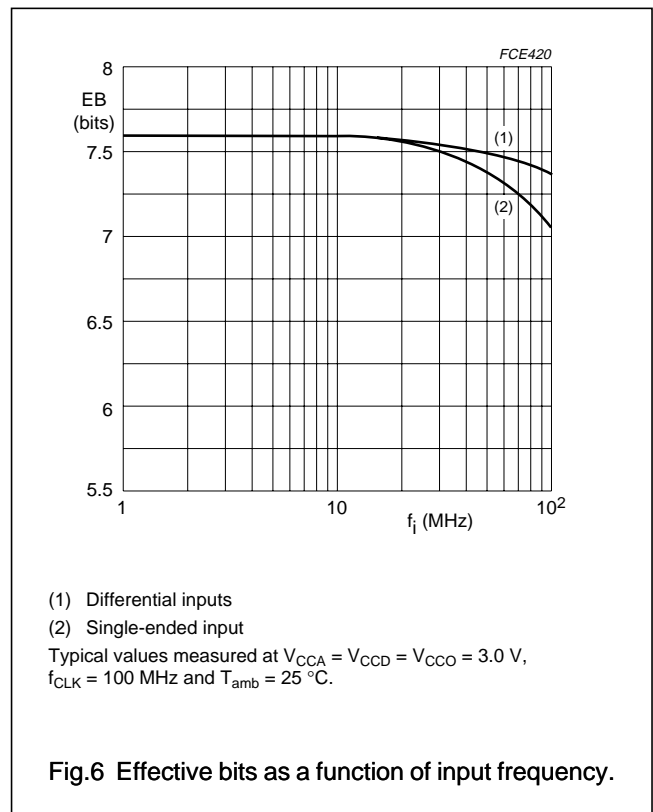
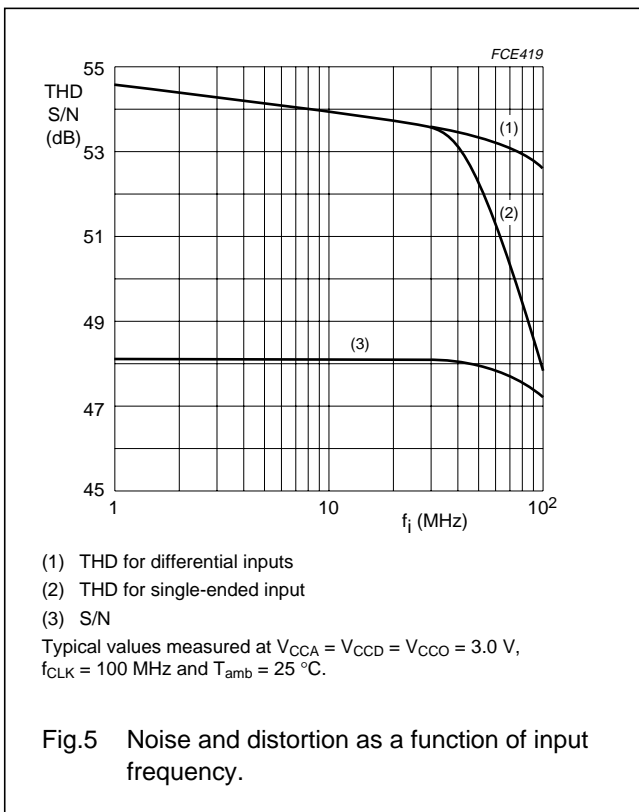
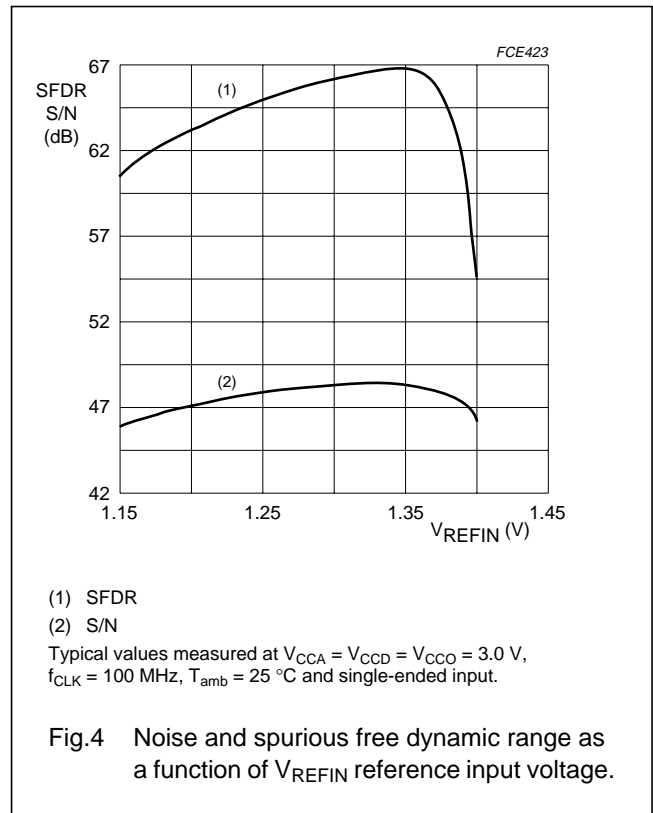
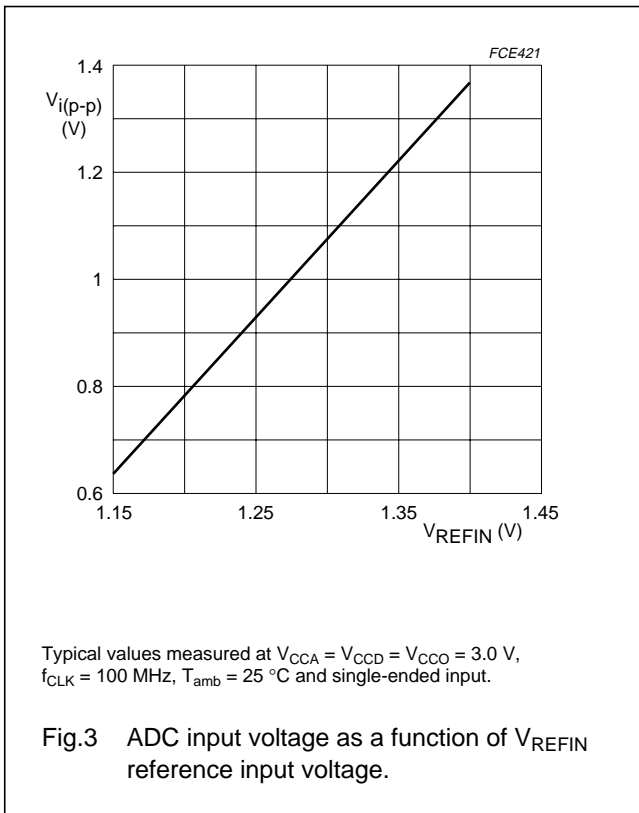
PIN TEN	TRACK-AND-HOLD
LOW	active
HIGH	inactive; tracking mode

Table 3 Output coding and input voltage (typical values; referenced to AGND); V_{REFIN} = 1.27 V

STEP	V _{INP} (V)	V _{INN} (V)	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.6	>2.1	0	0	0	0	0	0	0	0
0	1.6	2.1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
...
127	1.85	1.85
...
254	1	1	1	1	1	1	1	0
255	2.1	1.6	1	1	1	1	1	1	1	1
Overflow	>2.1	<1.6	1	1	1	1	1	1	1	1

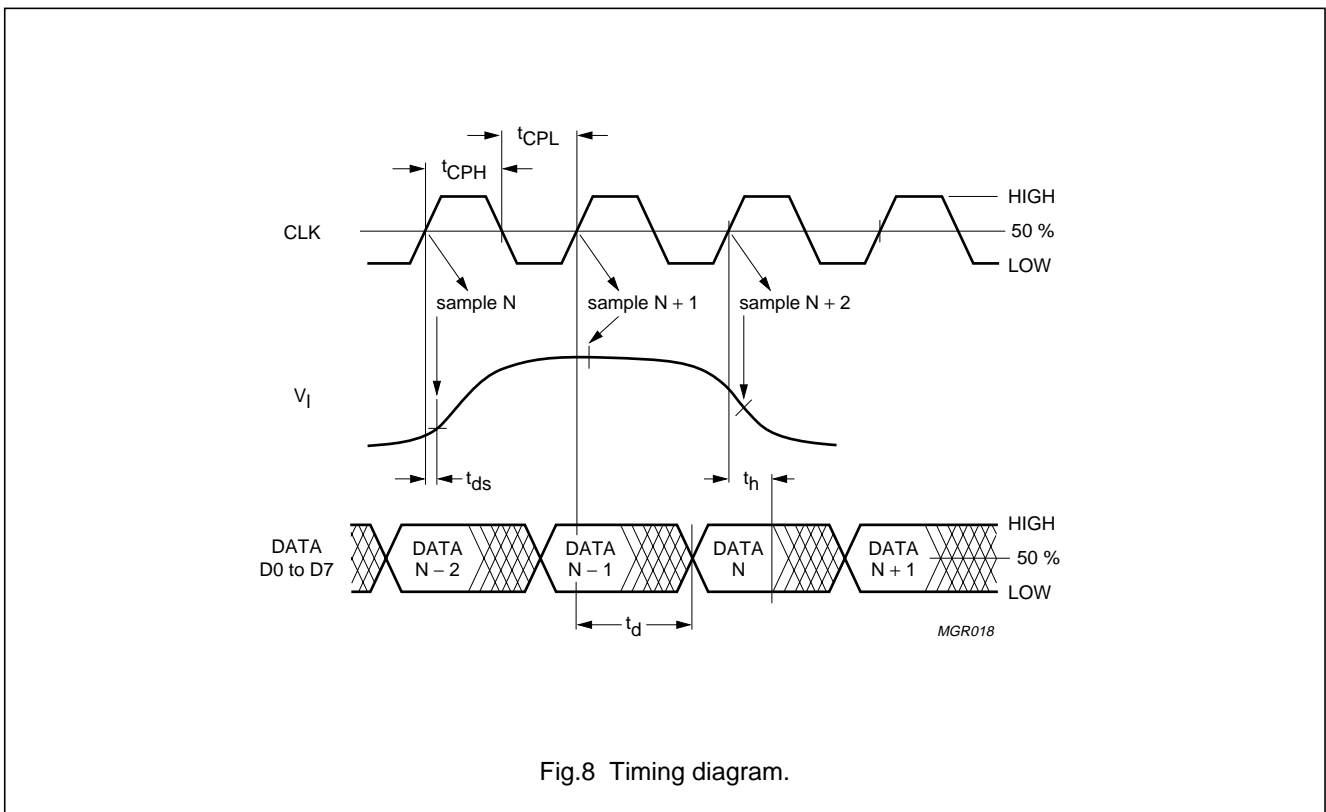
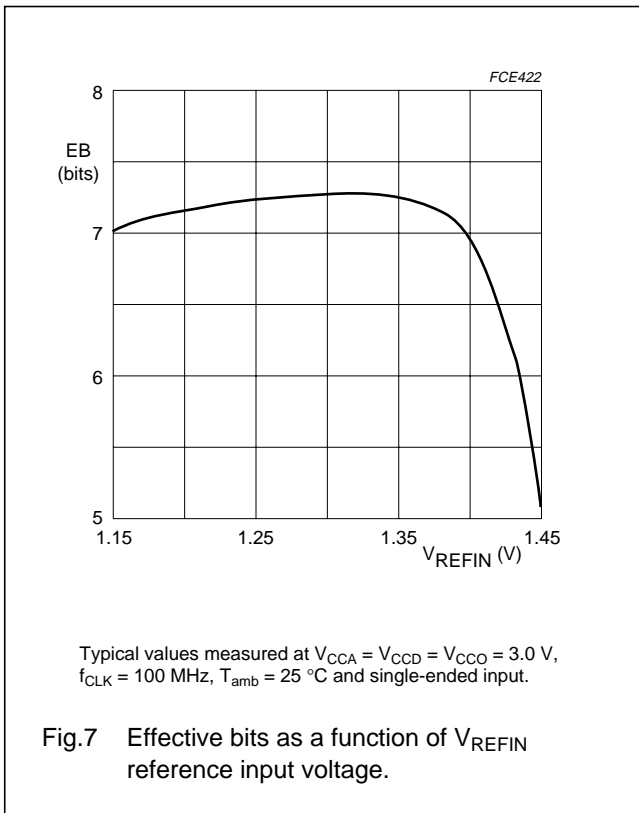
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APPLICATION INFORMATION

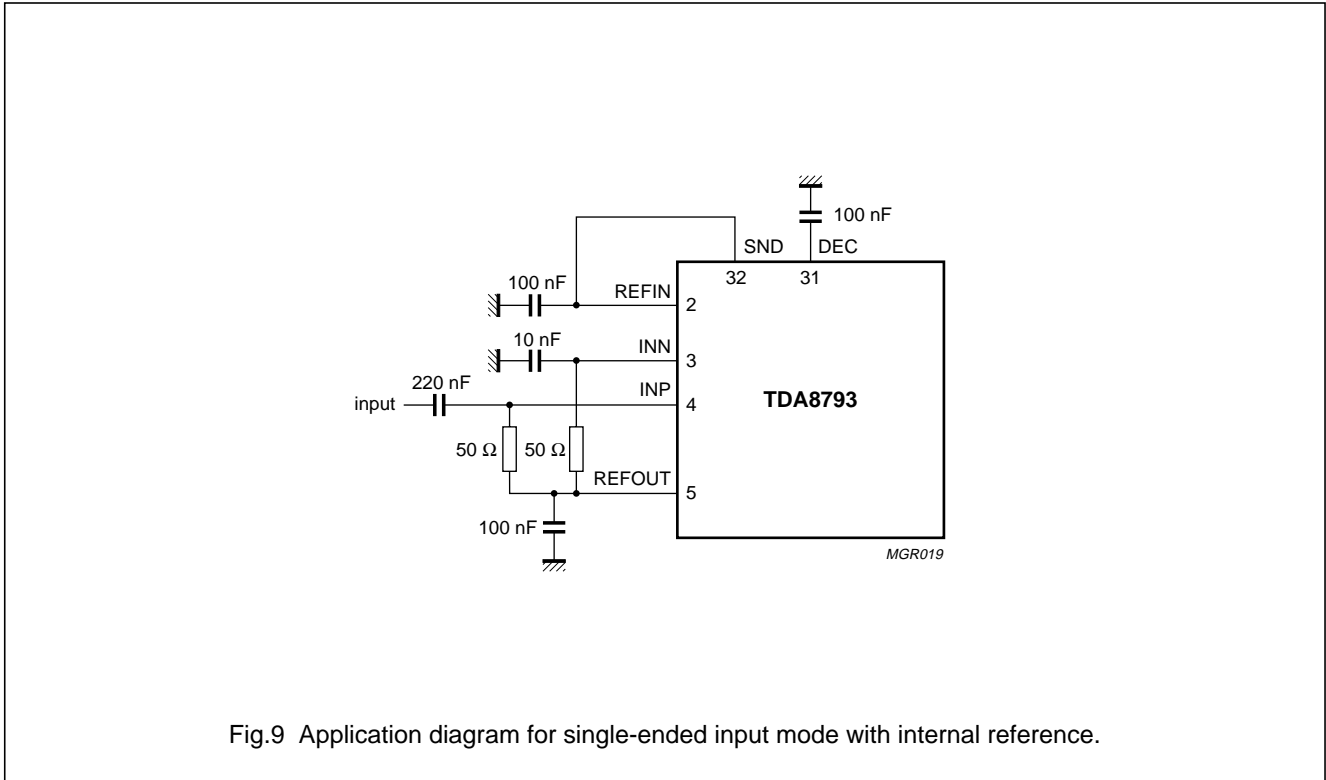


Fig.9 Application diagram for single-ended input mode with internal reference.

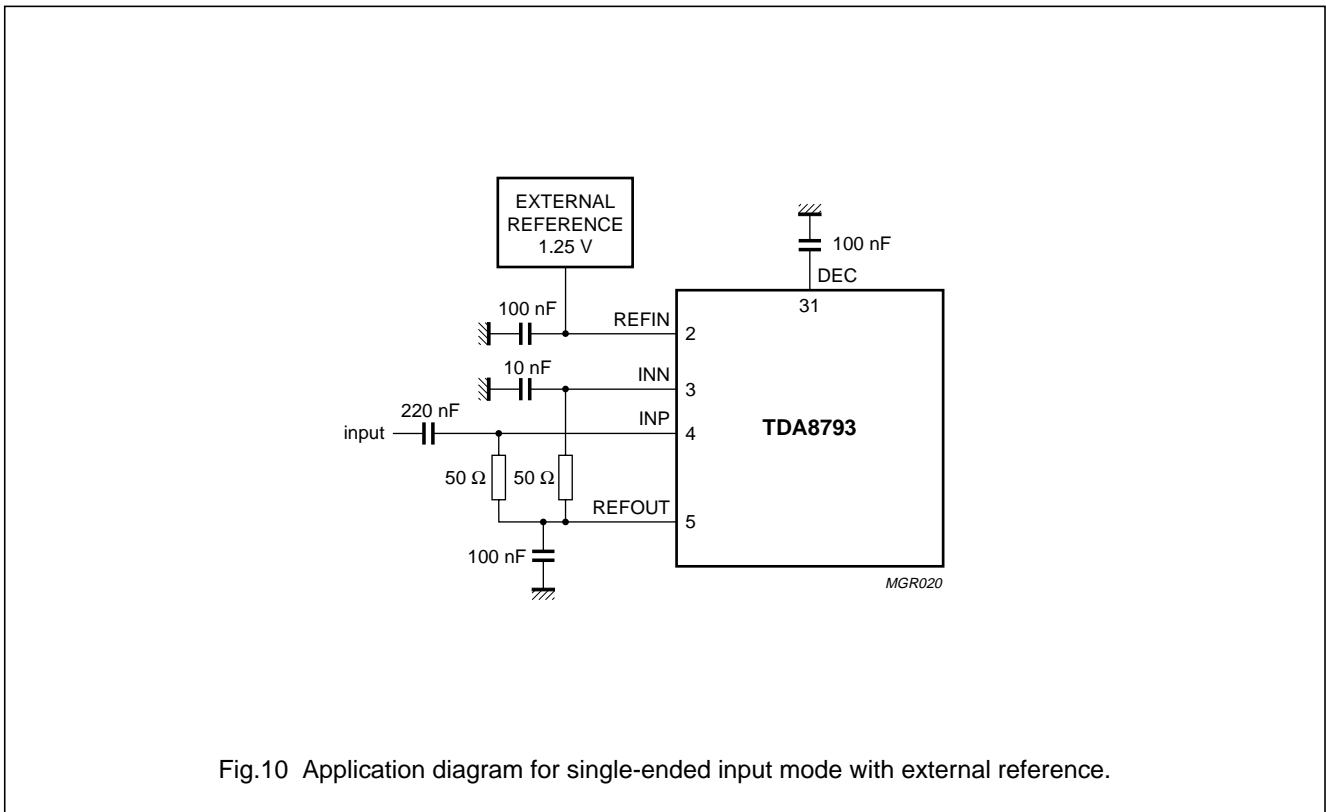


Fig.10 Application diagram for single-ended input mode with external reference.

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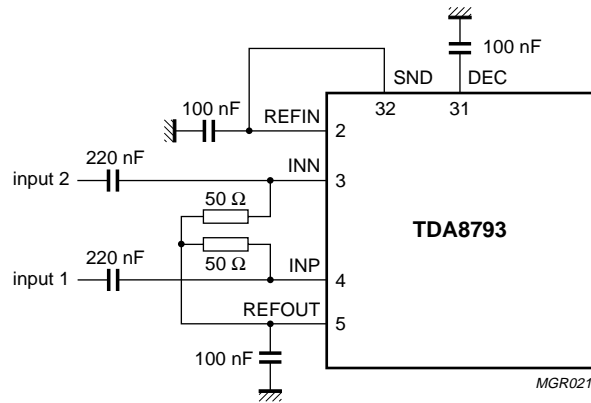


Fig.11 Application diagram for differential input mode with internal reference.

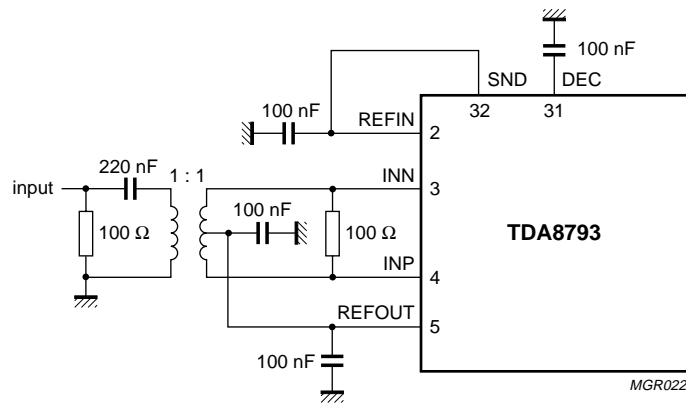


Fig.12 Application diagram for differential input mode using a transformer.

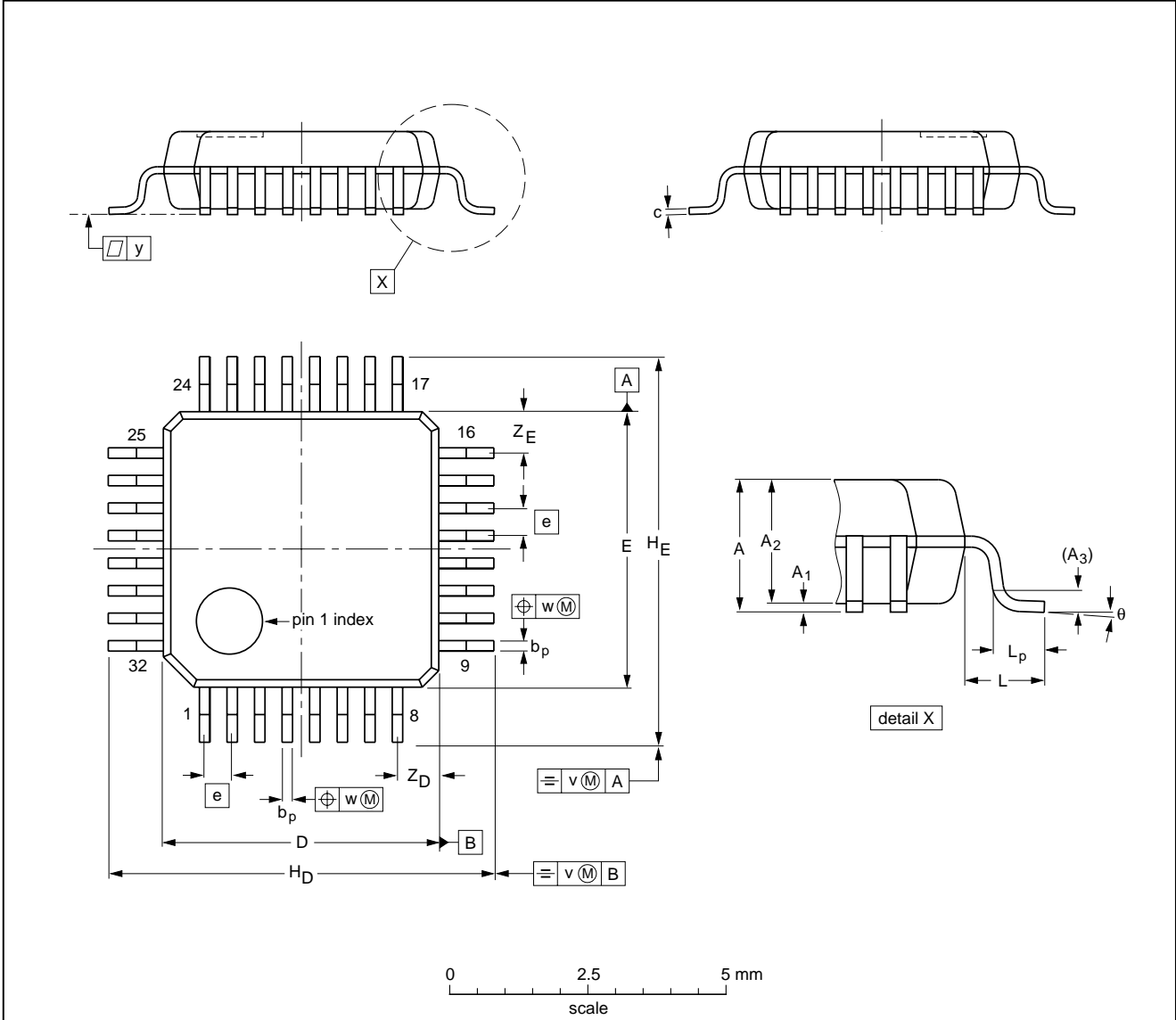
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PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm

SOT401-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						95-12-19 97-08-04

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

8-bit, low-power, 3 V, 100 Msps
Analog-to-Digital Converter (ADC)

TDA8793

NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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