NEC

MOS INTEGRATED CIRCUIT

μPD46128953-X

128M-BIT CMOS MOBILE SPECIFIED RAM
4M-WORD BY 32-BIT
ADDRESS / DATA MULTIPLEXED
EXTENDED TEMPERATURE OPERATION

Description

The μPD46128953-X is a high speed, low power, 134,217,728 bits (4,194,304 words by 32 bits) CMOS Mobile Specified RAM featuring synchronous burst read and synchronous burst write function.

The μPD46128953-X realizes high performance with the SDR interface, command and data inputs / outputs are synchronized the rising edge of clock.

The μPD46128953-X is fabricated with advanced CMOS technology using one-transistor memory cell.

Features

- 4,194,304 words by 32 bits organization
- Low voltage operation: 1.7 to 2.0 V (1.85±0.15 V)
- Operating ambient temperature: T_A = –25 to +85 °C
- Synchronous burst mode
  - Burst length : 8 double words (Wrap)
  - Burst sequence : Linear burst
  - Maximum clock frequency : 83 / 66 MHz
- SDR (Single Data Rate) Architecture
  One data transfers per one clock cycle
  All inputs/outputs are synchronized with the positive edge of the clock
- Write data mask (DM) for write operation
- Output Enable: /OE pin
- Chip Enable input: /CE1 pin
- Standby Mode input: CE2 pin
- Standby Mode 1: Normal standby (Memory cell data hold valid)
- Standby Mode 2: Density of memory cell data hold is variable

μPD46128953	Clock frequency MHz (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current	
				At operating mA (MAX.)	At standby μA (MAX.)
-E12X Note	83	1.7 to 2.0	–25 to +85	60	T.B.D.
-E15X	66			55	

Note Under consideration

Document No. M17506EJ1V1DS00 (1st edition)
Date Published September 2005 CP (K)
Printed in Japan

Ordering Information

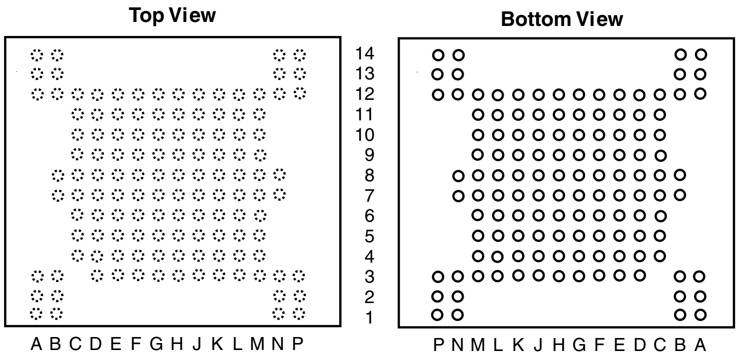
μPD46128593-X is mainly shipping by wafer.
Please consult with our sales offices for package samples and ordering information.

Pin Configuration

The following is pin configuration of package sample.

/xxx indicates active low signal.

127-pin PLASTIC FBGA (13.0 x 11.5)



Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	NC	NC											NC	NC
13	NC	NC											NC	NC
12	NC	NC	NC	DQ26	DQ25	DQ24	V_{DD}	$V_{SS}Q$	DQ23	DQ22	A/DQ21	NC	NC	NC
11			DQ28	DQ27	NC	NC	NC	NC	NC	V_{SS}	A/DQ20	A/DQ19		
10			DQ29	NC	NC	NC	NC	NC	A/DQ15	A/DQ7	A/DQ14	A/DQ18		
9			DQ30	NC	NC	NC	NC	A/DQ6	A/DQ13	A/DQ12	A/DQ5	A/DQ17		
8		NC	DQ31	/WE	CE2	NC	NC	NC	A/DQ4	$V_{DD}Q$	NC	A/DQ16	NC	
7		NC	NC	CLK	/ADV	/WAIT	NC	V_{DD}	A/DQ3	$V_{DD}Q$	A/DQ11	$V_{DD}Q$	NC	
6			NC	DM0	DM1	NC	NC	A/DQ1	A/DQ9	A/DQ10	A/DQ2	$V_{SS}Q$		
5			V_{SS}	NC	NC	NC	NC	$V_{SS}Q$	/OE	A/DQ0	A/DQ8	NC		
4			NC	NC	NC	NC	NC	NC	NC	/CE1	NC	NC		
3	NC	NC		NC	DM2	DM3	V_{DD}	V_{SS}	NC	NC	NC	NC	NC	NC
2	NC	NC											NC	NC
1	NC	NC											NC	NC

A/DQ0 to A/DQ021	: Address inputs , Data inputs/ outputs	/WAIT	: Wait output
DQ22 to DQ31	: Data inputs / outputs	DM0 to DM3	: Write data mask input
/CE1	: Chip select input	V_{DD}	: Power supply
CE2	: Standby mode input	V_{SS}	: Ground
/WE	: Write enable input	$V_{DD}Q$	: Power supply for DQ
/OE	: Output enable input	$V_{SS}Q$	: Ground for DQ
CLK	: Clock input	NC [Note]	: No Connection
/ADV	: Address valid		

Note Some signals can be applied because this pin is not internally connected.

Remark Refer to **10. Package Drawing** for the index mark.

Pin Function

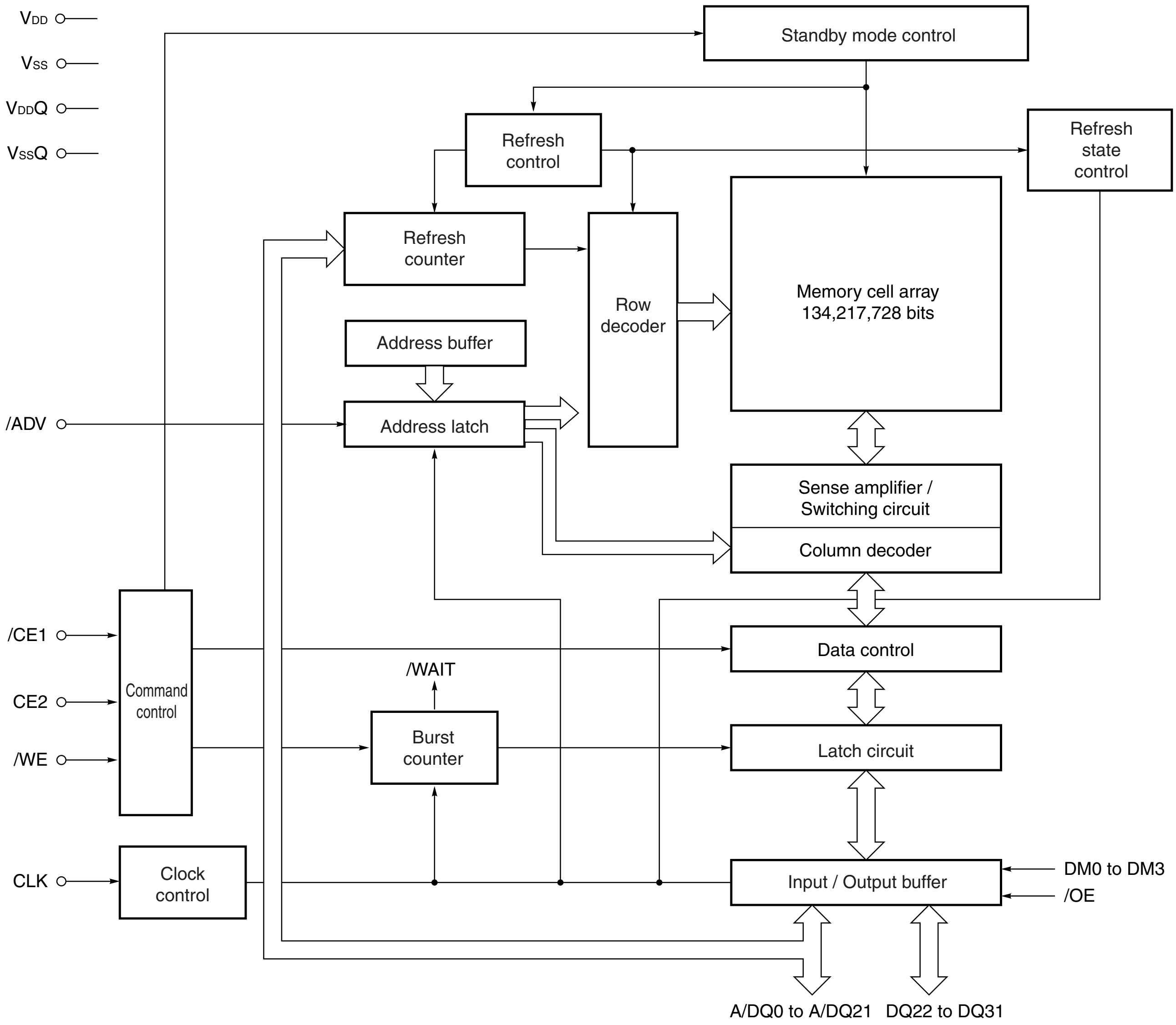
(1/2)

Symbol	Description
A/DQ0 to A/DQ21	Synchronous address input/data input/output These pins are used as address input pins and data input/output pins. When they are used as address input pins, the input address is latched at the rising edge of CLK. When the address is latched, the setup time and hold time must be satisfied at the rising edge of CLK. When they are used as data input/output pins, the input data is latched at the rising edge of CLK. When data is input, the setup time and hold time must be satisfied at the rising edge of CLK. Data is output from these pins at the rising edge of CLK.
DQ22 to DQ31	Synchronous data input/output. While the A/DQ pins function as address input pins and data input/output pins, these pins function only as data input/output pins. The input data is latched at the rising edge of CLK. When data is input, the setup time and hold time must be satisfied at the rising edge of CLK. Data is output at the rising edge of CLK.
CLK	Input clock. Addresses and control signals are latched in synchronization with this signal. All the synchronous input signals must satisfy the setup time and hold time at the rising edge of CLK.
/ADV	Synchronous address valid input signal. An address is latched at the rising edge of CLK while /ADV is LOW. When the address is latched, the setup time and hold time must be satisfied at the rising edge of CLK. Note: This signal serves as an asynchronous signal when the mode register set or read.
/CE1	Synchronous chip enable input. This device is active while /CE1 is LOW. When inputting /CE1, the setup time and hold time must be satisfied at the rising edge of CLK. **Remark** This signal serves as an asynchronous signal when the mode register set or read.
CE2	Asynchronous power-down mode input When this signal is made LOW, the device enters the power-down mode status. CE2 is not synchronized with the clock. It is an asynchronous signal.
/OE	Synchronous output enable input. When this signal is made LOW, read data is output. When inputting /OE, the setup time and hold time must be satisfied at the rising edge of CLK. **Remark** This signal serves as an asynchronous signal when the mode register set or read.
/WE	Synchronous write enable input. When /WE inputs a LOW at the same time as /ADV, the device recognizes a write operation. When inputting /WE, the setup time and hold time must be satisfied at the rising edge of CLK. **Remark** This signal serves as an asynchronous signal when the mode register is set or read.

(2/2)

Symbol	Description
DM0 to DM3	Synchronous write data mask input. These signals can mask write data during burst write. To input data mask, the setup time and hold time must be satisfied at the rising edge of CLK. Data mask can be controlled in byte units. DM0: A/DQ0 to ADQ7 DM1: A/DQ8 to ADQ15 DM2: A/DQ16 to ADQ21, DQ22 to DQ23 DM3: DQ24 to DQ31
/WAIT	Synchronous wait output. /WAIT is a status signal (output) that indicates the preparation for starting burst read/burst write This pin outputs a LOW while the internal circuit is busy, and a HIGH when it is ready. The wait signal is output at the rising edge of CLK.
V_{DD}	Supply voltage: Usually, the supply voltage is 1.85 V. Refer to **DC Characteristics and Recommended Operation Conditions**.
V_{SS}	Supply voltage: Ground
$V_{DD}Q$	Supply voltage: Supply voltage for DQ. Usually, this voltage is 1.85 V. Refer to **DC Characteristics and Recommended Operation Conditions**.
$V_{SS}Q$	Supply voltage: Ground for DQ.
NC	No connection Some signals can be applied because this pin is not internally connected.

Block Diagram



Truth Table

Mode	/CE1	CE2	CLK	/ADV	/OE	/WE	A/DQ0-A/DQ21 , DQ22-DQ31
Deselect (Standby Mode 1)	H	H	↑	×	×	×	High-Z
Power Down (Standby Mode 2) [Note1]	×	L	×	×	×	×	High-Z
Output Disable	L	H	↑	×	H	×	High-Z
Start Address Latch [Note2]			↑	L	H	×	High-Z
Start Address not Latch [Note3]			↑	H	×	×	Low-Z or High-Z
Read Command input [Note2]			↑	L	H	H	High-Z
Write Command input [Note2]			↑	L	H	L	High-Z
Burst Read Termination [Note4]	L to H		↑	×	×	×	Low-Z to High-Z
Burst Write Termination [Note4]			↑	×	×	×	High-Z

Notes 1. CE2 pin must be fixed HIGH except Standby Mode 2 (refer to **2.3 Standby Mode Status Transition**).

2. Start address latch and read/write command input are performed at the next rising edge of clock when /ADV is transferred HIGH to LOW.

3. It is impossible that Start address latch and read/write command input are performed at the first rising edge of clock during /ADV is fixed HIGH.

4. Refer to **3.6 Burst Read Termination**, **3.7 Burst Write Termination**.

Remark H, HIGH: V_{IH}, L, LOW: V_{IL}, ×: V_{IH} or V_{IL}
For read/write operation, refer to **7 Timing Charts.**

CONTENTS

1. Initialization

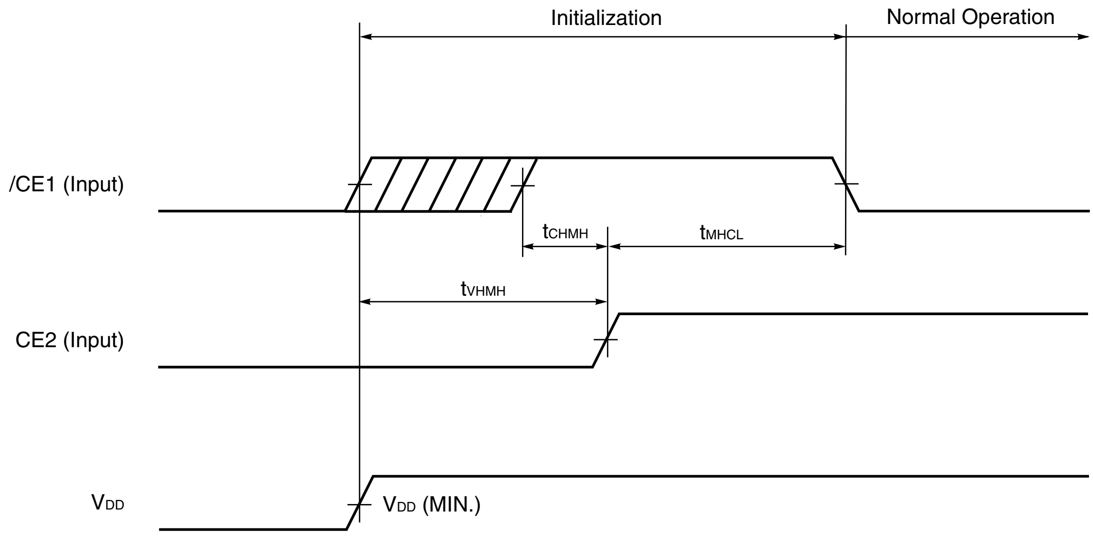
Initialize the μPD46128953-X at power application using the following sequence to stabilize internal circuits.

(1) Following power application, make CE2 HIGH after fixing CE2 to LOW for the period of t_{VHMH}.
Make /CE1 HIGH before making CE2 HIGH.

(2) /CE1 and CE2 are fixed HIGH for the period of t_{MHCL}.

Normal operation is possible after the completion of initialization.

Figure 1-1. Initialization Timing Chart



Cautions 1. Make CE2 LOW when starting the power supply.

2. t_{VHMH} is specified from when the power supply voltage reaches the prescribed minimum value (V_{DD} (MIN.)).

Initialization Timing

Parameter	Symbol	MIN.	MAX.	Unit
Power application to CE2 LOW hold	t_{VHMH}	50		μs
/CE1 HIGH to CE2 HIGH	t_{CHMH}	0		ns
Following power application CE2 HIGH hold to /CE1 LOW	t_{MHCL}	300		μs

2. Partial Refresh

2. 1 Standby Mode

In addition to the regular standby mode (Standby Mode 1) with a 128M bits density, Standby Mode 2, which performs partial refresh, is also provided.

2. 2 Density Switching

In Standby Mode 2, the densities that can be selected for performing refresh are 64M bits, 32M bits, 16M bits, and 0M bit.

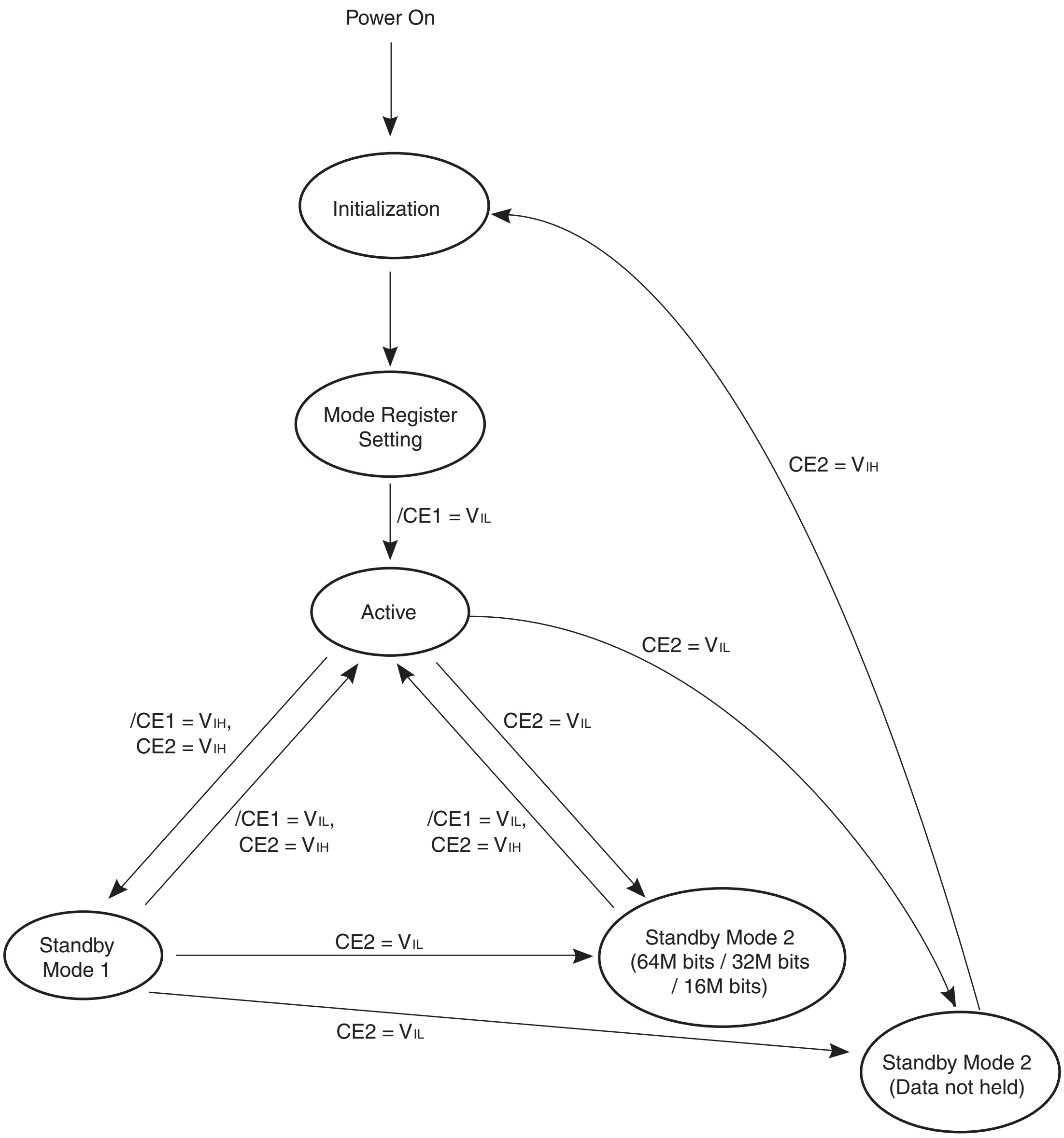
The density for performing refresh can be set with the mode register. Once the refresh density has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application. (For how to perform mode register settings, refer to section **4. Mode Register Settings**.)

2. 3 Standby Mode Status Transition

In Standby Mode 1, /CE1 and CE2 are HIGH. In Standby Mode 2, CE2 is LOW. In Standby Mode 2, if 0M bit is set as the density, it is necessary to perform initialization the same way as after applying power, in order to return to normal operation from Standby Mode 2. When the density has been set to 64M bits, 32M bits, or 16M bits in Standby Mode 2, it is not necessary to perform initialization to return to normal operation from Standby Mode 2.

For the timing charts, refer to **Figure 9-1. Standby Mode 2 (data hold: 64M bits / 32M bits / 16M bits) Entry / Exit Timing Chart**, **Figure 9-2. Standby Mode 2 (data not held) Entry / Exit Timing Chart**.

Figure 2-1. Standby Mode State Machine



2. 4 Addresses for Which Partial Refresh Is Supported

Data hold density	Correspondence address
64M bits	000000H to 1FFFFFH
32M bits	000000H to 0FFFFFH
16M bits	000000H to 07FFFFH

3. Burst Operation

3. 1 Features of Burst Operation

Function		Features
Burst Length		8 double words
Burst Wrap		Wrap
Burst Sequence		Linear
Valid Clock Edge		CLK Rising Edge
Latency Count	Read Latency	6, 7, 8
	Write Latency	5, 6, 7

3. 2 Latency

Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through Mode Register Set sequence after power-up. Once RL is set through Mode Register Set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL–1.

Latency Count

Grade	Clock Frequency	Read Latency	Write Latency Note
-E12X	<83 MHz	7, 8	6, 7
-E15X	<66 MHz	6, 7, 8	5, 6, 7

Note Write Latency = Read Latency–1

Figure 3-1. Latency Configuration (Read)

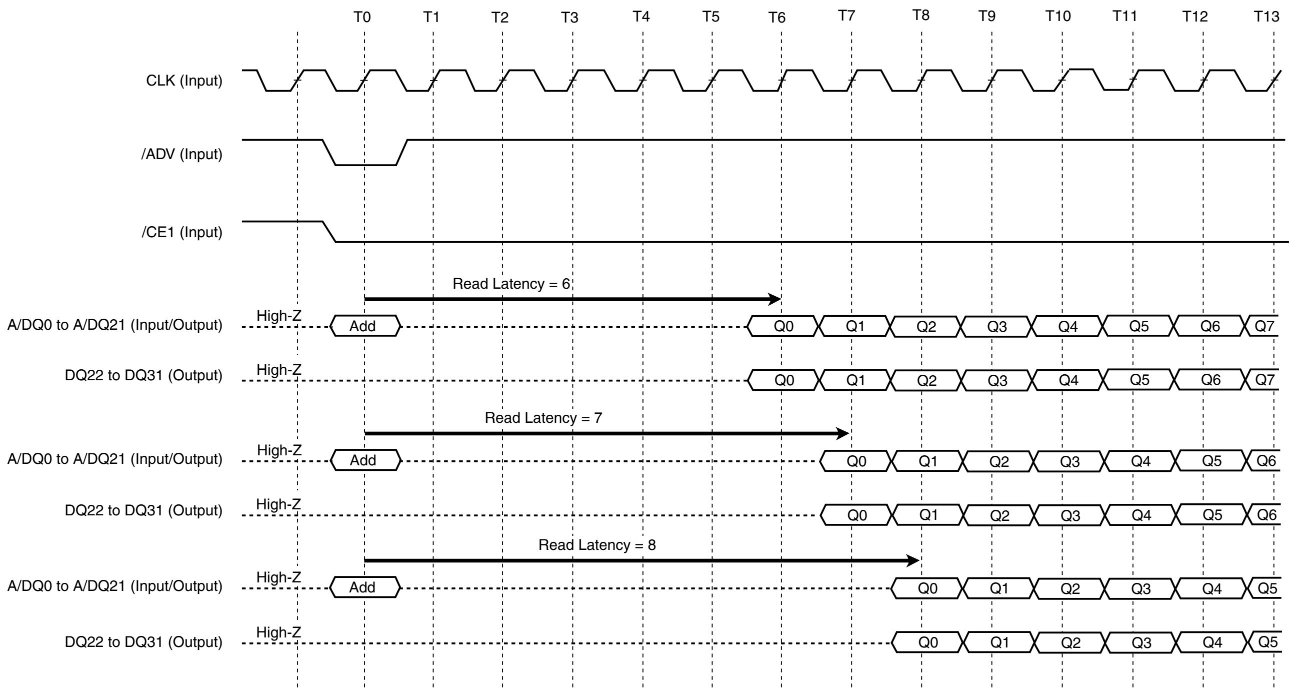
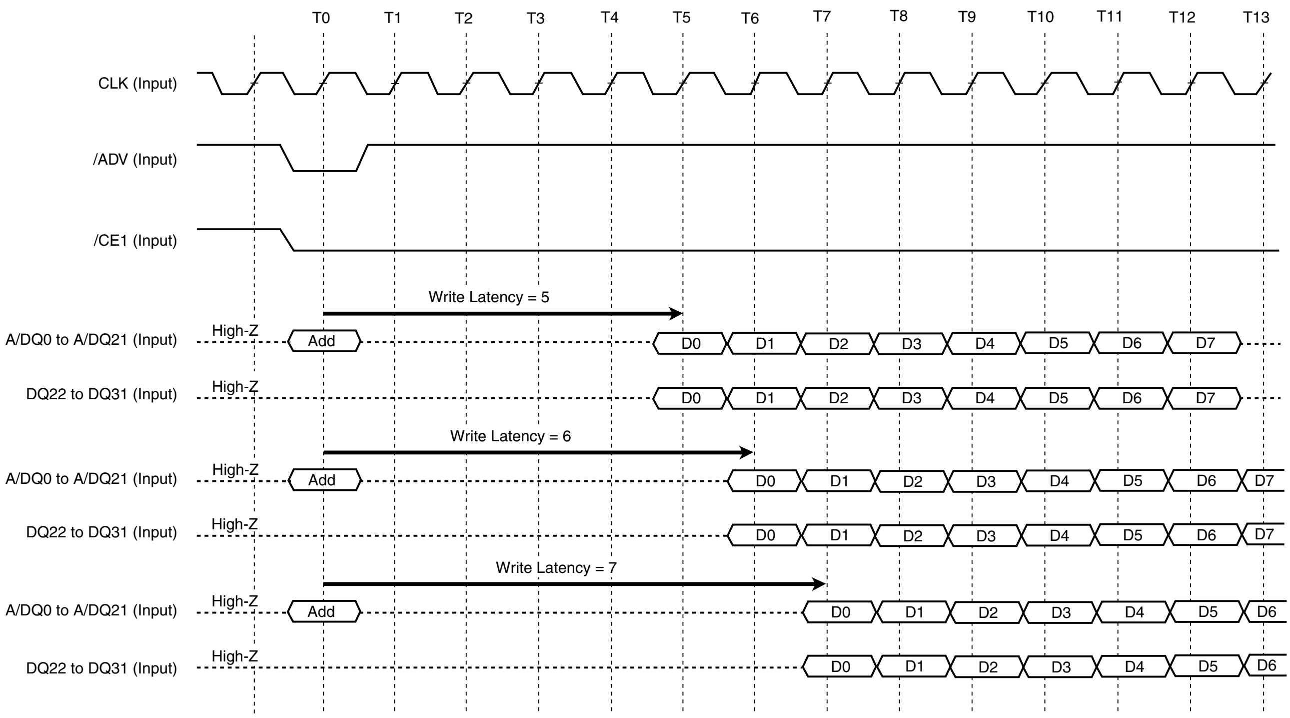


Figure 3-2. Latency Configuration (Write)



3. 3 Burst Length, Burst Sequence, Wrap Around

The burst length is 8 double words and the corresponding address is (A/DQ2, A/DQ1, A/DQ0). A burst operation that extends over addresses higher than A/DQ3 cannot be executed.

Wrap-around is performed within the burst length of 8 double words. Refer to **Table 3-1. Burst Sequence**.

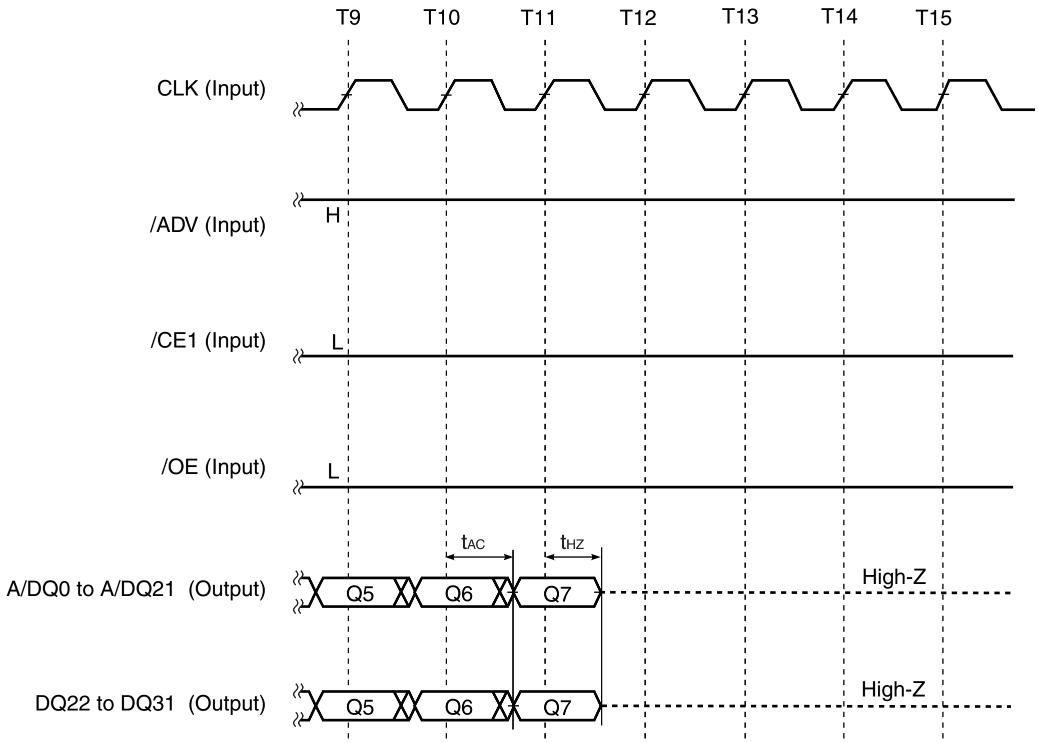
Table 3-1. Burst Sequence

Start Address (A/DQ2 , A/DQ1, A/DQ0)	Burst Sequence
	Linear , Wrap
	1st data - 2nd data - 3rd data - 4th data - 5th data - 6th data - 7th data - 8th data
(0, 0, 0)	(0, 0, 0) - (0, 0, 1) - (0, 1, 0) - (0, 1, 1) - (1, 0, 0) - (1, 0, 1) - (1, 1, 0) - (1, 1, 1)
(0, 0, 1)	(0, 0, 1) - (0, 1, 0) - (0, 1, 1) - (1, 0, 0) - (1, 0, 1) - (1, 1, 0) - (1, 1, 1) - (0, 0, 0)
(0, 1, 0)	(0, 1, 0) - (0, 1, 1) - (1, 0, 0) - (1, 0, 1) - (1, 1, 0) - (1, 1, 1) - (0, 0, 0) - (0, 0, 1)
(0, 1, 1)	(0, 1, 1) - (1, 0, 0) - (1, 0, 1) - (1, 1, 0) - (1, 1, 1) - (0, 0, 0) - (0, 0, 1) - (0, 1, 0)
(1, 0, 0)	(1, 0, 0) - (1, 0, 1) - (1, 1, 0) - (1, 1, 1) - (0, 0, 0) - (0, 0, 1) - (0, 1, 0) - (0, 1, 1)
(1, 0, 1)	(1, 0, 1) - (1, 1, 0) - (1, 1, 1) - (0, 0, 0) - (0, 0, 1) - (0, 1, 0) - (0, 1, 1) - (1, 0, 0)
(1, 1, 0)	(1, 1, 0) - (1, 1, 1) - (0, 0, 0) - (0, 0, 1) - (0, 1, 0) - (0, 1, 1) - (1, 0, 0) - (1, 0, 1)
(1, 1, 1)	(1, 1, 1) - (0, 0, 0) - (0, 0, 1) - (0, 1, 0) - (0, 1, 1) - (1, 0, 0) - (1, 0, 1) - (1, 1, 0)

3. 4 Burst Read End

The memory output goes into a high impedance state after completion of the burst read operation of the eighth double word. Therefore, no data is output from the memory even if CLK is kept input while /CE1 = LOW after the burst read operation of 8 words has been completed.

Figure 3-3. Burst Read End

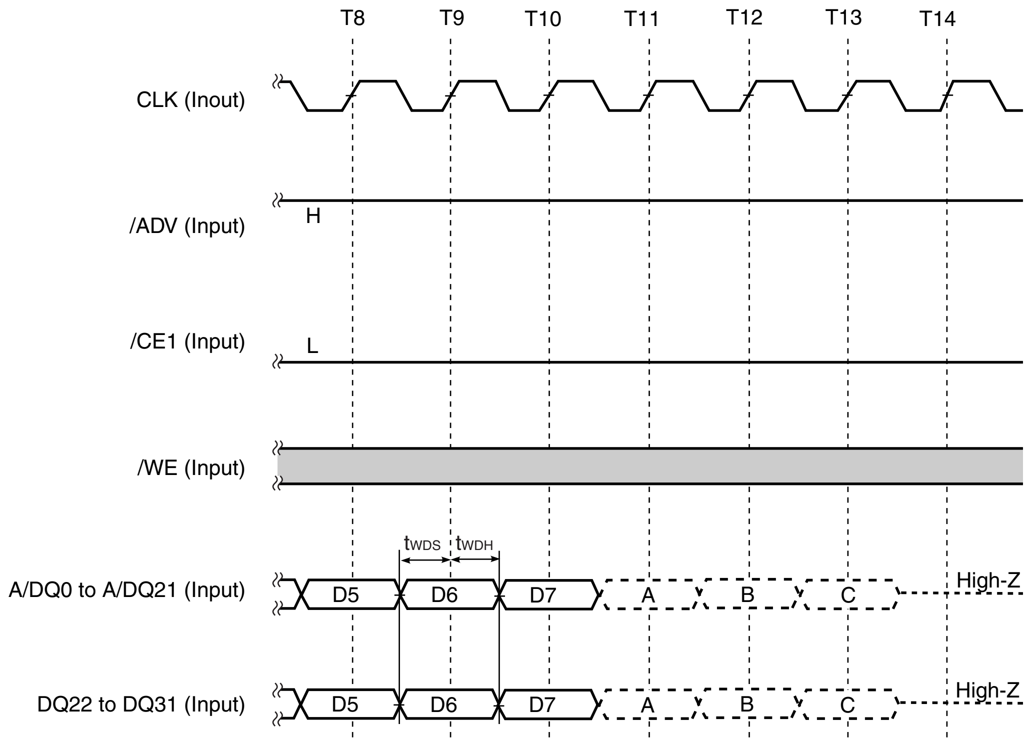


Remark Memory output goes into a high impedance state after the last data (Q7) read by the burst operation has been output.

3. 5 Burst Write End

The memory does not input write data to internal circuits even if CLK is kept input with /CE1 = LOW and write data is input from the controller after completion of a burst write operation of 8 double words.

Figure 3-4. Burst Write End

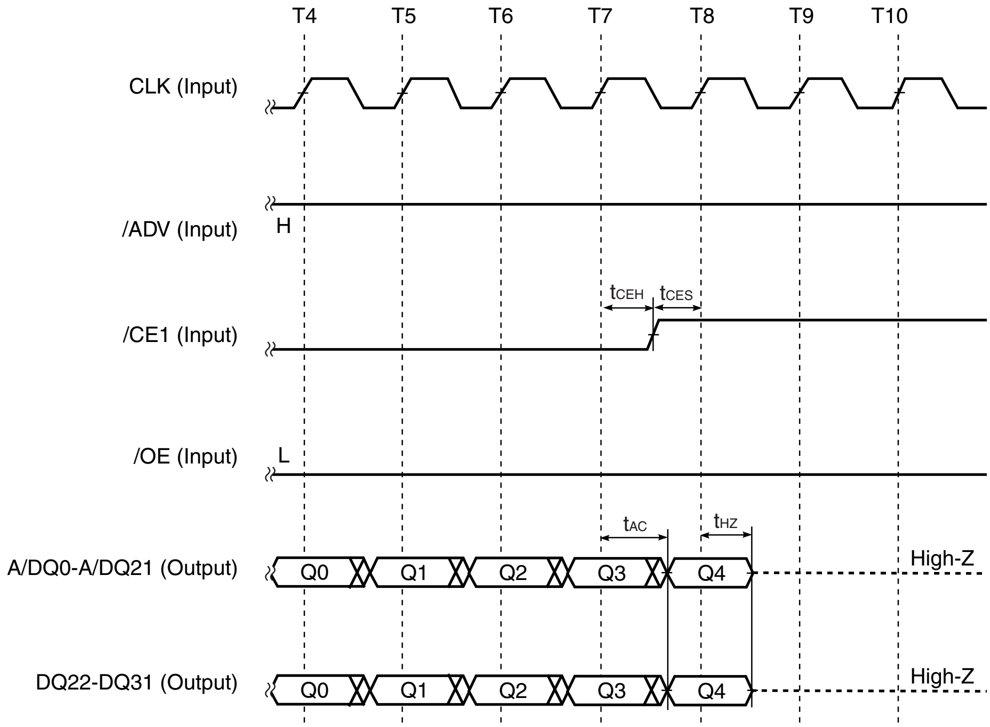


Remark The memory does not input any write data to internal circuits even if write data (A, B, or C) is input after the last burst write data (D7) has been input, as shown in **Figure 3-4**.

3. 6 Burst Read Termination

A burst read termination is executed when /CE1 is made HIGH during a burst read operation. The command that the burst read termination (/CE1 = HIGH) is recognized at the next rising edge of CLK when /CE1 = HIGH, the read data is output before the command of the burst read termination (/CE1 = HIGH) is input.

Figure 3-5. Burst Read Termination



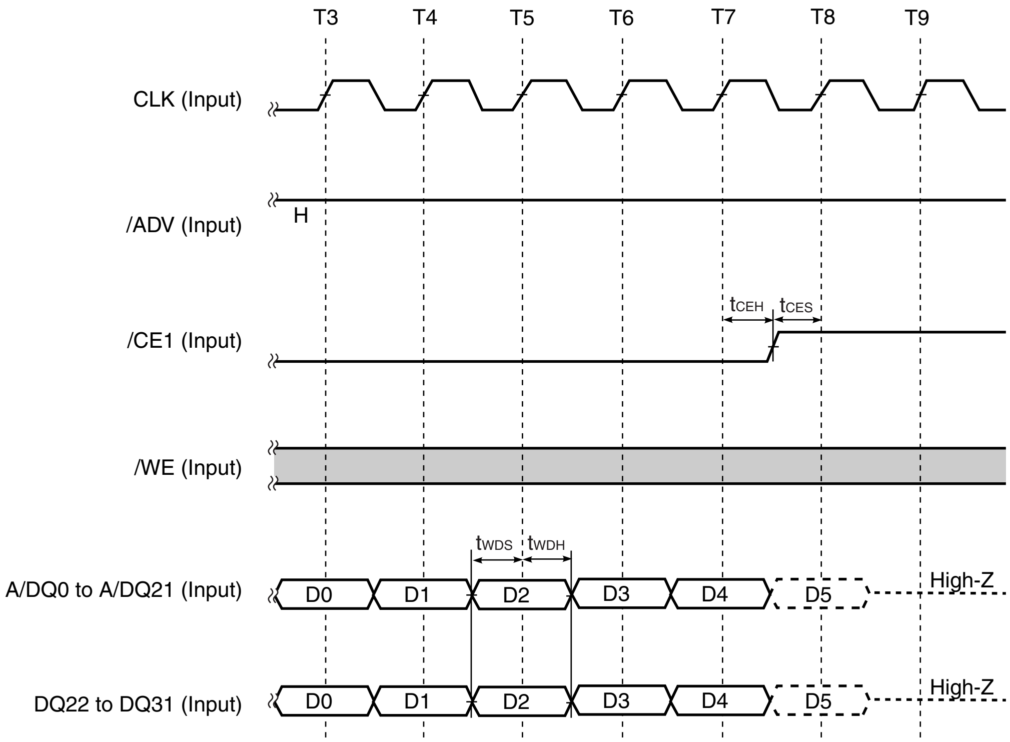
Remark If the burst read termination is performed (/CE1: LOW → HIGH) before the rising edge of CLK in T8, as shown in **Figure 3-5**, determined data is output as the read data (Q4) from the rising edge of CLK in T7.

The burst read termination is valid after the initial read data has been output.
(For the burst read termination, refer to **Figure 7-5. Burst Read Termination Cycle Timing Chart (/CE1 control)**.)

3. 7 Burst Write Termination

A burst write termination is executed when /CE1 is made HIGH during a burst write operation. The command that the burst write termination (/CE1 = HIGH) is recognized at the next rising edge of CLK when /CE1 = HIGH, the write data is written before the command of the burst write termination (/CE1 = HIGH) is input.

Figure 3-6. Burst Write Termination



Remark If the burst write termination is performed (/CE1: LOW → HIGH) before the rising edge of CLK in T8, as shown in **Figure 3-6**, the write data is input to memory at the rising edge of CLK in T7. The write data input in cycle T8 (D5) is invalid.

The burst termination is valid after the initial write data has been input.
(For the burst write termination refer to **Figure 7-6. Burst Write Termination Cycle Timing Chart (/CE1 control)**.)

3. 8 /WAIT signal behavior

/WAIT is a status signal (output) that indicates the preparation for starting burst read/burst write
This pin outputs a LOW while the internal circuit is busy, and a HIGH when it is ready.
The wait signal is output at the rising edge of CLK.

Table 3-2. Relation Between Internal Operation of Memory and /WAIT Output

Internal Operation of Memory	/WAIT output
Preparation for burst read/burst write in progress	LOW
Completion of preparation for burst read/burst write	HIGH

3. 9 /WAIT output

The /WAIT output is enabled after specified time from CLK. /WAIT output is transferred LOW to HIGH one cycle before 1st burst read data output and 1st burst write data input.

Figure 3-7. /WAIT Output Timing (Read Cycle)

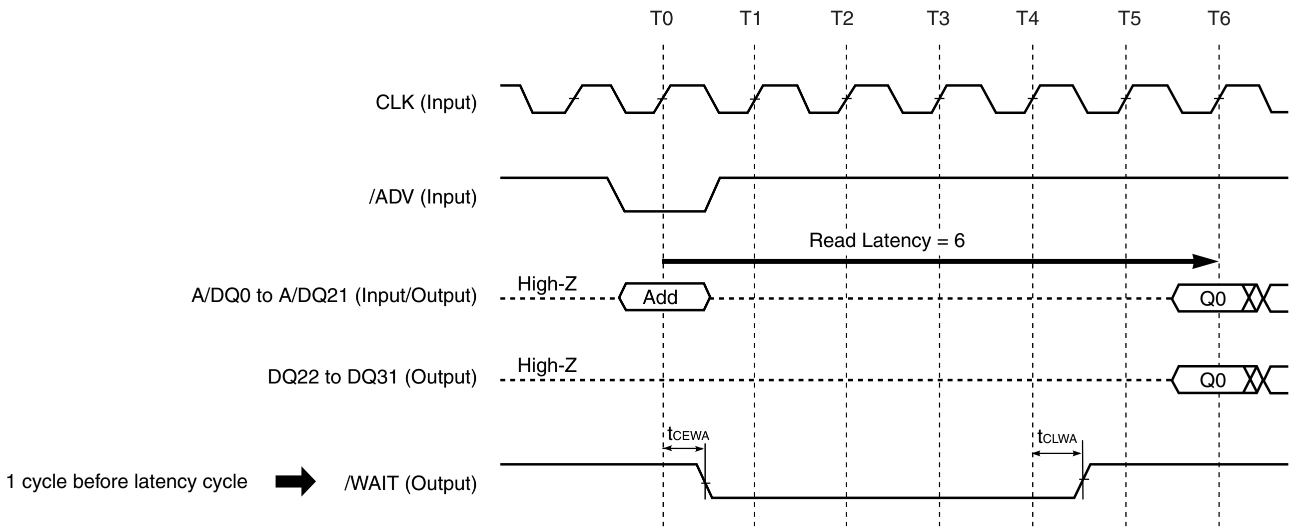
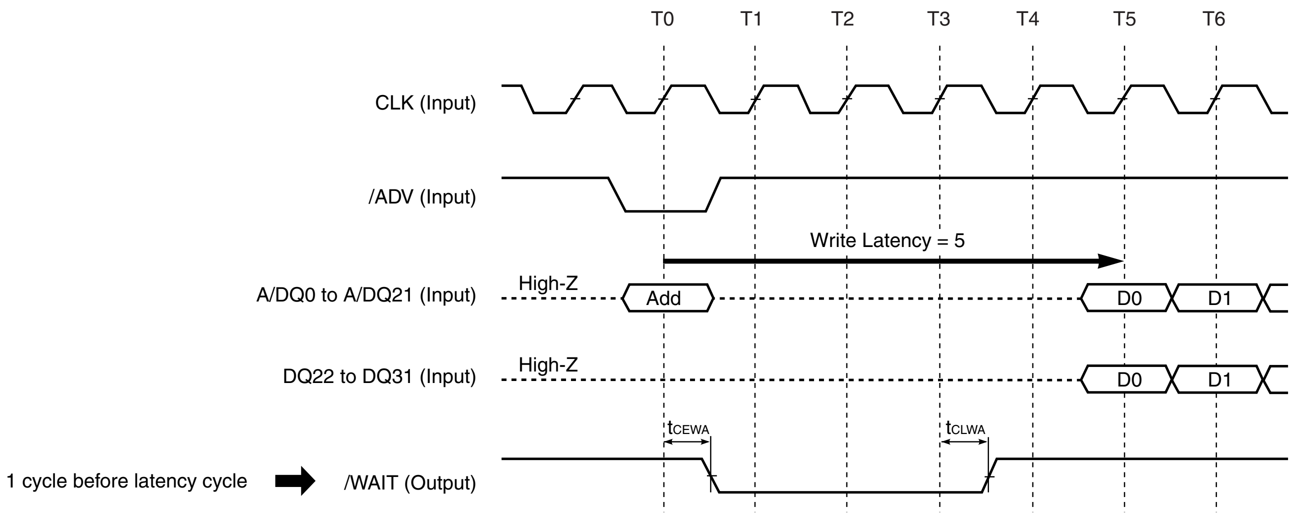


Figure 3-8. /WAIT Output Timing (Write Cycle)



4. Mode Register Settings

The default value of the mode register of the μPD46128953-X is undefined upon power application. Therefore, be sure to set the mode register after power application and initialization.

4. 1 Mode Register Setting Method

Each mode can be set by performing a total of six cycles of operations in succession after reading the most significant address (3FFFFFH) – two consecutive cycles for writing any data and three consecutive cycles for writing specific data (codes 1 to 3) – by an asynchronous access (with CLK fixed HIGH or LOW).

Table 4-1. Mode Register Settings

Cycle	Operation	Address	Data
1st cycle	Read	3FFFFFH	Don't care
2nd cycle	Write	3FFFFFH	Don't care
3rd cycle	Write	3FFFFFH	Don't care
4th cycle	Write	3FFFFFH	Code 1 (A/DQ0 = 1)
5th cycle	Write	3FFFFFH	Code 2
6th cycle	Write	3FFFFFH	Code 3

Codes 1 to 3 are set at the register. The register has a function to latch an address and data necessary for instruction execution, and does not occupy the memory.

Whether the mode register is set or read can be selected by code 1 in the 4th bus cycle. If setting of the mode register is selected (A/DQ0 = 1) by code 1 in the 4th bus cycle, the contents of the mode register are set by code 2 in the 5th bus cycle and code 3 in the 6th bus cycle.

The command contents are shown in **Table 4-2. Mode Register Code 1 Definition (4th cycle)**, **Table 4-3. Mode Register Code 2 Definition (5th cycle)**, and **Table 4-4. Mode Register Code 3 Definition (6th cycle)**.

For the timing chart and flowchart, refer to **Figure 8-1. Mode Register Setting Timing Chart** and **Figure 8-2. Mode Register Setting Flowchart**.

If reading the mode register is selected by code 1 in the 4th bus cycle (A/DQ = 0), the contents of the mode register currently set in the 5th and 6th bus cycles can be read. If the mode register is read before it is set, any (undefined) data is read.

For the mode register, refer to **4.2 Mode Register Reading**.

4. 1. 1 Cautions for Setting Mode Register

When the mode register is set, the status of the internal counter is identified by the toggle operation of /CE1 and /OE. When setting a mod entry, therefore, perform a toggle operation of /CE1 in each cycle (one read cycle and five write cycles).

In the 1st bus cycle (read cycle), perform a toggle operation of /OE in the same manner as /CE1. If an illegal address or data is written or if an address and data are written in an incorrect sequence, the mode register is not correctly set.

If the most significant address (3FFFFFH) is read (in the 1st bus cycle), written (2nd bus cycle), and then written (3rd bus cycle), a sequence of setting/reading the mode register is started. Therefore, setting of the mode register cannot be stopped after the 4th bus cycle. If the normal sequence is executed up to the 5th bus cycle, setting of the mode register cannot be stopped until the 6th bus cycle is completed.

Once the mode register has been set, the setting is retained while power is supplied and CE2 = HIGH, until it is re-set. If data is not retained by turning off the power or making CE2 LOW (except partial), however, the setting of the mode register is undefined. Re-set the register after power application or when returning from a data non-retention status.

For the timing chart and flowchart, refer to **Figure 8-1. Mode Register Setting Timing Chart** and **Figure 8-2. Mode Register Setting Flowchart**.

Table 4-2. Mode Register Code1 Definition (4th Bus Cycle)

Data Code	Symbol	Function	Value	Description
A/DQ0	RW	Mode Register Setting / Mode Register Reading	0	Mode Register Reading
			1	Mode Register Setting
A/DQ21 to A/DQ1	–	–	All “1”	Reserved
DQ31 to DQ22	–	–	All “1”	Reserved

Table 4-3. Mode Register Code2 Definition (5th Bus Cycle)

Data Code	Symbol	Function	Value	Description
A/DQ1 to A/DQ0	PR	Partial Refresh Density	00	32M
			01	16M
			10	64M
			11	0M
A/DQ4 to A/DQ2	BL	Burst length	000	Reserved
			001	Reserved
			010	8 double words
			011	Reserved
			100	Reserved
			101	Reserved
			110	Reserved
			111	Reserved
A/DQ5	M	Function Mode	0	Synchronous Burst
			1	Reserved
A/DQ7 to A/DQ6	DS	Driver Strength	00	Strong
			01	Reserved
			10	Weak
			11	Middle
A/DQ21 to A/DQ8	–	–	All “1”	Reserved
DQ31 to DQ22	–	–	All “1”	Reserved

Table 4-4. Mode Register Code3 Definition (6th Bus Cycle)

Data Code	Symbol	Function	Value	Description
A/DQ2 to A/DQ0	RL	Read Latency	000	Reserved
			001	Reserved
			010	Reserved
			011	Reserved
			100	6
			101	7
			110	8
			111	Reserved
A/DQ3	N/A	N/A	1	Reserved
A/DQ4	SW	Single Write	0	Burst Read & Burst Write
			1	Reserved
A/DQ5	VE	Valid Clock Edge	0	Reserved
			1	Rising Edge
A/DQ6	RP	Reset to Asynchronous	1	Reserved
A/DQ7	WC	/WE Control	0	/WE Pulse Control
			1	Reserved
A/DQ21 to A/DQ8	–	–	1	Reserved
DQ31 to DQ22	–	–	1	Reserved

4. 1. 2 Mode Register Setting/Reading

Select whether to set the mode register or read the set contents of the register by this item.

If 1 is input to A/DQ0 in the 4th cycle, the mode register setting mode is set. If 0 is input to A/DQ0 in the 4th cycle, the mode register reading mode is set.

For how to read the mode register, refer to **4.2 Mode Register Reading**.

4. 1. 3 Partial refresh Density

The partial refresh area is set by this item. If 00 are input to A/DQ1 and A/DQ0 in the 5th cycle, it is set that 32M bits are retained. If 01 are input to A/DQ1 and A/DQ0 in the 5th cycle, it is set that 16M bits are retained. If 10 are input to A/DQ1 and A/DQ0 in the 5th cycle, it is set that 64M bits are retained. If 11 are input to A/DQ1 and A/DQ0 in the 5th cycle, it is set that all bits are not retained.

4. 1. 4 Burst length

The burst length is set by this item. If 010 are input to A/DQ4, A/DQ3, and A/DQ2 in the 5th cycle, the burst length is set to 8. This product supports only a burst length of 8.

4. 1. 5 Function mode

The burst read mode is set by this item. If 0 is input to A/DQ5 in the 5th cycle, the burst mode is set.
Be sure to input 0 to A/DQ5.

4. 1. 6 Driver strength

The output driver strength is set by this item. If 00 are input to A/DQ7 and A/DQ6 in the 5th cycle, the output driver strength is set to Strong. If 11 are input to A/DQ7 and A/DQ6 in the 5th cycle, the output driver strength is set to Middle. If 10 are input to A/DQ7 and A/DQ6 in the 5th cycle, the output driver strength is set to Weak.

4. 1. 7 Read Latency

The read latency count is set by this item. If 100 are input to A/DQ2, A/DQ1, and A/DQ0 in the 6th cycle, the read latency is set to 6. If 101 are input to A/DQ2, A/DQ1, and A/DQ0 in the 6th cycle, the read latency is set to 7. If 110 are input to A/DQ2, A/DQ1, and A/DQ0 in the 6th cycle, the read latency is set to 8. Write latency is automatically set RL-1.

4. 1. 8 Single Write

The write mode is set by this item, if 0 is input to A/DQ4 in the 6th cycle, the write mode is set to burst write.
Be sure to input 0 to A/DQ4.

4. 1. 9 Valid Clock Edge

The valid clock edge (Rising edge or Falling edge) is set in the burst mode. If 1 is input to A/DQ5 in the 6th cycle, rising edge is set to valid clock edge.

4. 1. 10 Reset to Asynchronous

This function is not available now and reserved for future function. Be sure to input 1 to A/DQ6.

4. 1. 11 /WE control

The input timing of /WE is set by this item. If 0 is input to A/DQ7 in the 6th cycle, the input timing of /WE is set to be the same as the timing of loading an address (/WE = LOW while /ADV = LOW). Refer to **5.3 Loading Command (read/write)**.
Be sure to input 0 to A/DQ7.

4. 1. 12 Setting of unused bits

Some of the undefined bits are used to enter a test mode that is not disclosed. Therefore, be sure to input 1 to the undefined bits (A/DQ21 to A/DQ1 and DQ31 to DQ22 in the 4th cycle, A/DQ21 to A/DQ8 and DQ31 to DQ22 in the 5th cycle, and A/DQ3, A/DQ21 to A/DQ8, and DQ31 to DQ22 in the 6th cycle).

4. 2 Mode Register Reading

If 0 is set to A/DQ0 in the 4th cycle after reading the most significant address (3FFFFFH) – two consecutive cycles for writing any data, it is possible to read current setting value of code 2 in the 5th cycle and current setting value of code 3 in the 6th cycle

Table 4-5. Mode Register Settings

Cycle	Operation	Address	Data
1st cycle	Read	3FFFFFH	Don't care
2nd cycle	Write	3FFFFFH	Don't care
3rd cycle	Write	3FFFFFH	Don't care
4th cycle	Write	3FFFFFH	Code 1 (A/DQ0 = 0)
5th cycle	Read	3FFFFFH	Code 2
6th cycle	Read	3FFFFFH	Code 3

Codes 1 to 3 are written to the register. The register has a function to latch an address and data necessary for instruction execution, and does not occupy the memory.

For the timing chart and flowchart, refer to **Figure 8-3. Mode Register Read Timing Chart** and **Figure 8-4. Mode Register Read Flowchart**.

4. 2. 1 Cautions for Setting Mode Register

When the mode register is set, the status of the internal counter is identified by the toggle operation of /CE1 and /OE. When setting the mode register, therefore, perform a toggle operation of /CE1 in each cycle (one read cycle, three write cycles, and two mode register read cycles). In the 1st bus cycle (read cycle) and 5th and 6th bus cycles, perform a toggle operation of /OE in the same manner as /CE1. If an illegal address or data is written or if the codes are written in an incorrect sequence, reading the mode register fails and the mode register is not read correctly.

If the most significant address (3FFFFFH) is read (in the 1st bus cycle), written (2nd bus cycle), and then written (3rd bus cycle), a sequence of setting/reading the mode register is started. Therefore, setting of the mode register cannot be stopped after the 4th bus cycle. If the normal sequence is executed up to the 3rd bus cycle, setting of the mode register cannot be stopped until the 6th bus cycle is completed.

4. 2. 2 Data read from mode register

If reading the mode register is started, the contents of currently set code 2 (partial refresh density, burst length, function mode, and driver strength) can be read in the 5th bus cycle. In the 6th bus cycle, the contents of currently set code 3 (read latency, single write, valid clock edge, reset to asynchronous, and /WE control) can be read. If the mode register is read before it is set, any (undefined) data is output.

Set or read the mode register in compliance with the AC specifications in Table 4-6.

Table 4-6. AC Specification of Mode Register Setting / Reading

Item	Symbol	-E12X, -E15X		Unit
		MIN.	MAX.	
Specification of Mode Register Setting / Reading				
Cycle time	t_{MSC}	90	10000	ns
Address setup time to /ADV = HIGH	t_{AS}	6		ns
Address hold time to /ADV = HIGH	t_{AH}	1		ns
/CE1 setup time to /ADV = HIGH	t_{CS}	6		ns
Address setup time to /OE = LOW	t_{AOSM}	0		ns
/ADV Low pulse width	t_{VPL}	6		ns
/OE to output in low impedance	t_{OLZM}	5		ns
/OE to output valid	t_{ACM}		30	ns
/CE1 to output in high impedance	t_{CHZM}		10	ns
/OE to output in high impedance	t_{OHZM}		10	ns
Write data setup time to /WE = HIGH	t_{DW}	20		ns
Write data hold time to /WE = HIGH	t_{DH}	0		ns
/CE1 HIGH pulse width	t_{CP}	10		ns
/WE LOW pulse width	t_{WP}	50		ns
/OE LOW pulse width	t_{OVL}	50		ns

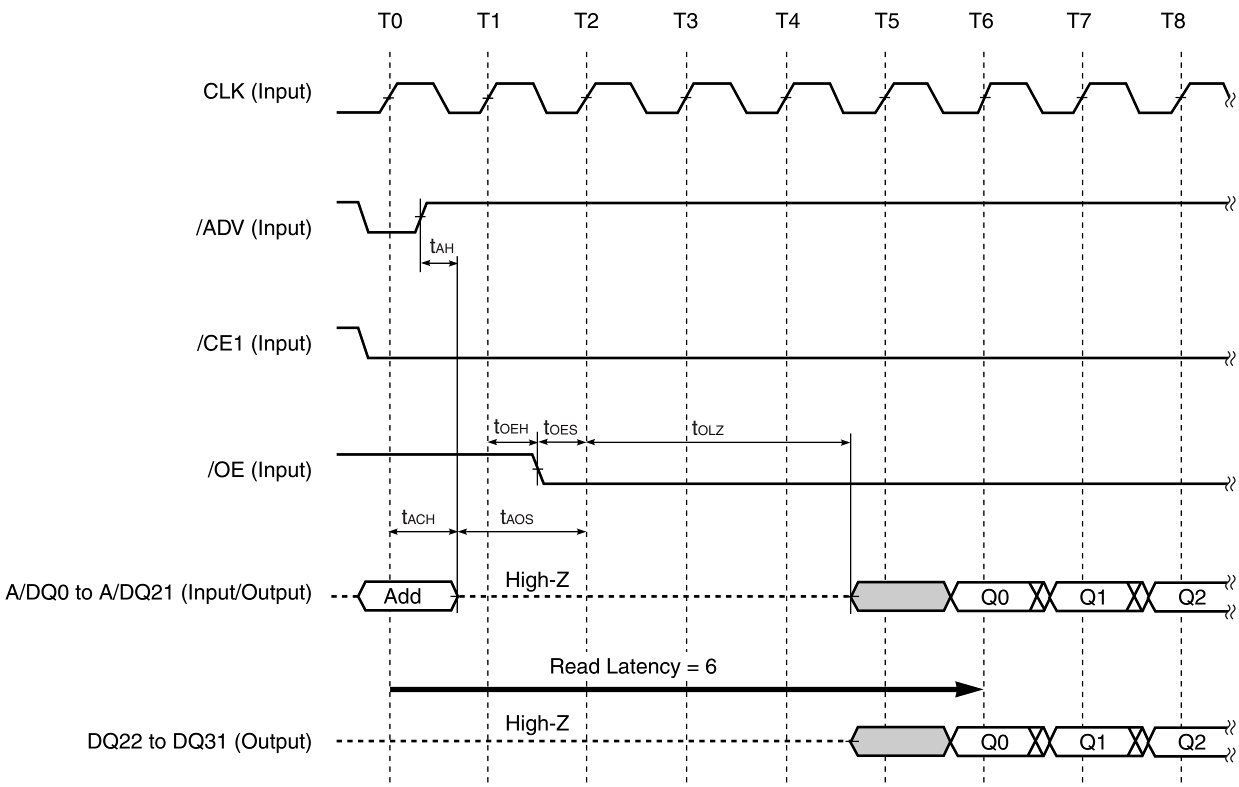
For the timing chart and flowchart, refer to **Figure 8-1. Mode Register Setting Timing Chart**, **Figure 8-2. Mode Register Setting Flowchart**, **Figure 8-3. Mode Register Read Timing Chart** and **Figure 8-4. Mode Register Read Flowchart**.

5. Address, /OE, /WE, DM control

5. 1 Relation of address inputs and /OE control

This product uses only one pin to input an address and input/output DQ. Consequently, a bus fight may occur between an address input from the controller and data output from the memory and, therefore, the timing must be considered. Data is output after specified t_{OLZ} from the first rising edge of CLK when /OE has changes its level from HIGH to LOW. Therefore, complete inputting an address from the controller before the first rising edge of CLK when /OE has changed its level from HIGH to LOW.

Figure 5-1. Address inputs and /OE Timing

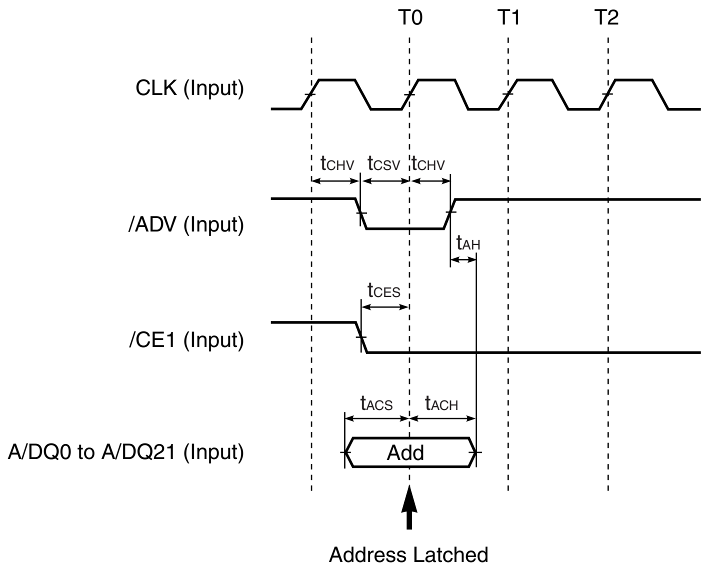


Remark Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

5. 2 Address Latching

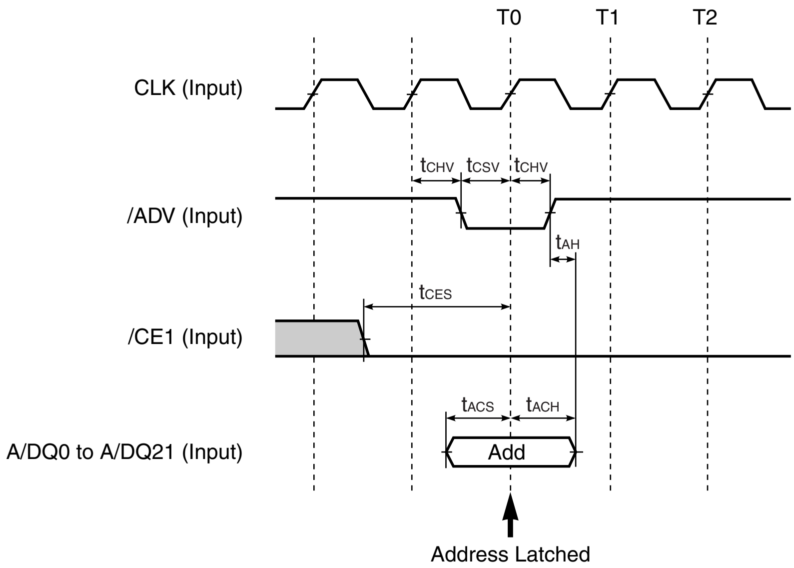
An address is latched at the first rising edge of CLK when /ADV changes its level from HIGH to LOW while /CE1 = LOW. An address can be latched and a read or write operation can be started as soon as the memory has changed its status from standby (/CE1 = HIGH) to active (/CE1 = LOW). If the period in which /ADV = LOW while /CE1 = LOW extends over two or more CLK as shown in Figure 5-4, an address is latched at the first rising edge of CLK after /ADV = LOW.

Figure 5-2. Address Latched Timing 1



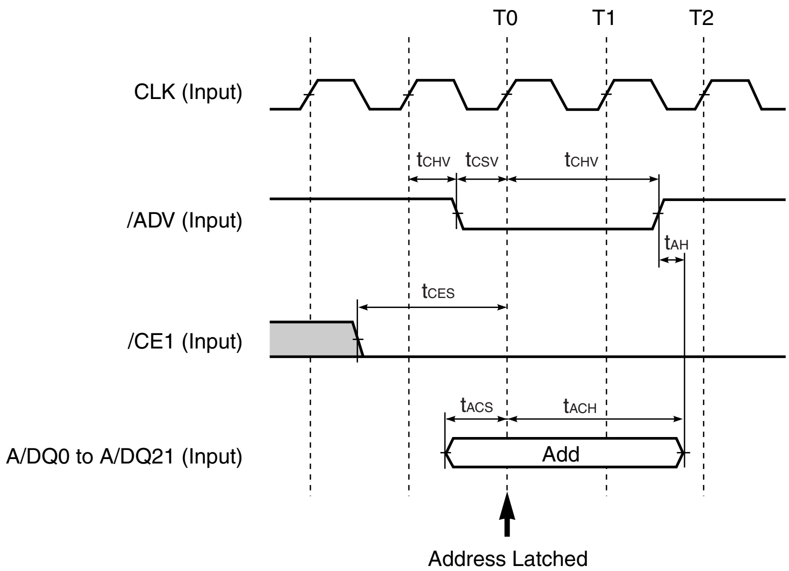
Remark Refer to 6. **Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

Figure 5-3. Address Latched Timing 2



Remark Refer to 6. **Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

Figure 5-4. Address Latched Timing 3

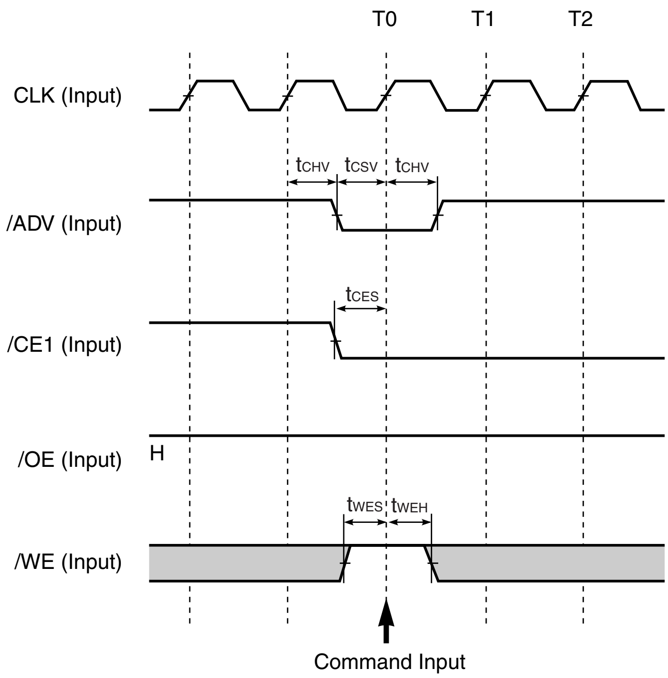


Remark Refer to 6. **Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

5. 3 Read / Write Command Loading

A command (read/write) is loaded in the same timing as an address (refer to **6.2 Address Latching**). If /WE = HIGH at that time, a read operation is started; if /WE = LOW, a write operation is started. Figure 5-5 shows a read operation and Figure 5-6 shows a write operation. If /WE = LOW in the cycle next to that in which an address is loaded as shown in **Figure 5-7**, a write operation is not recognized. The operation in Figure 5-7 is a read operation.

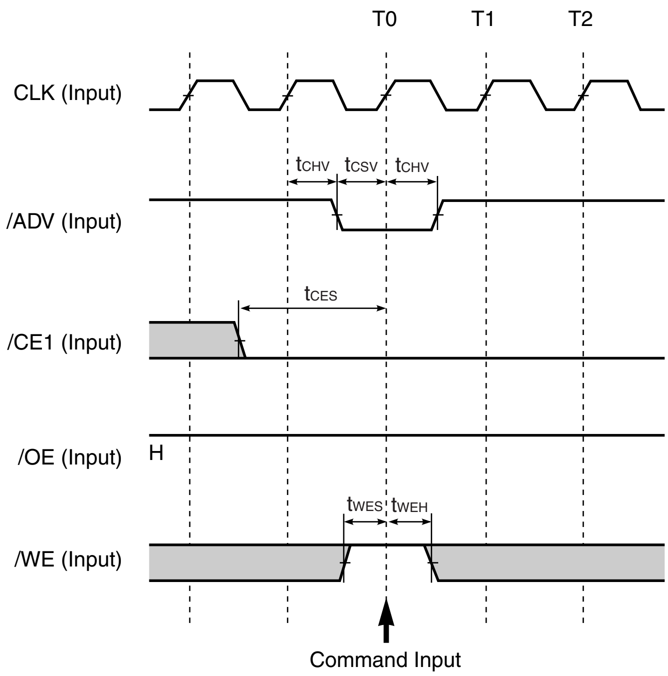
Figure 5-5. Command Loading Timing 1



Remarks 1. Figure 5-5 shows a read operation

2. Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

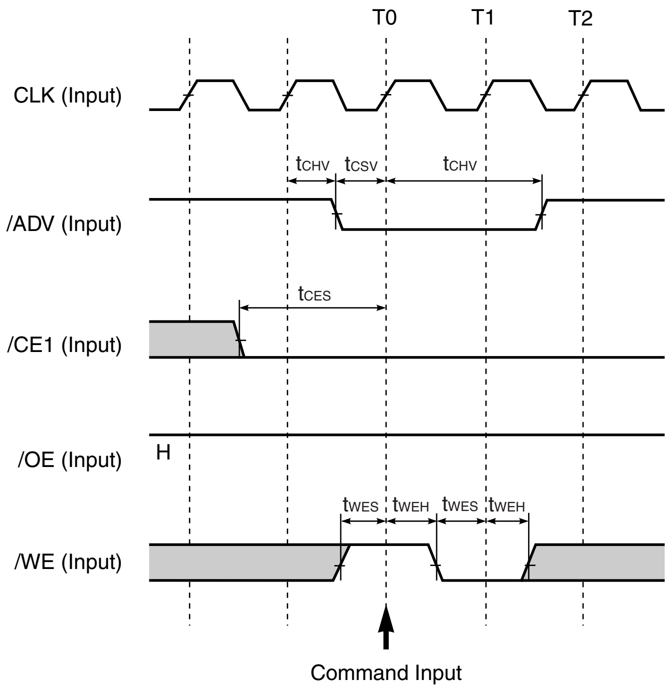
Figure 5-6. Command Loading Timing 2



Remarks 1. Figure 5-6 shows a write operation

2. Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

Figure 5-7. Command Loading Timing 3



Remarks 1. Figure 5-7 shows a read operation

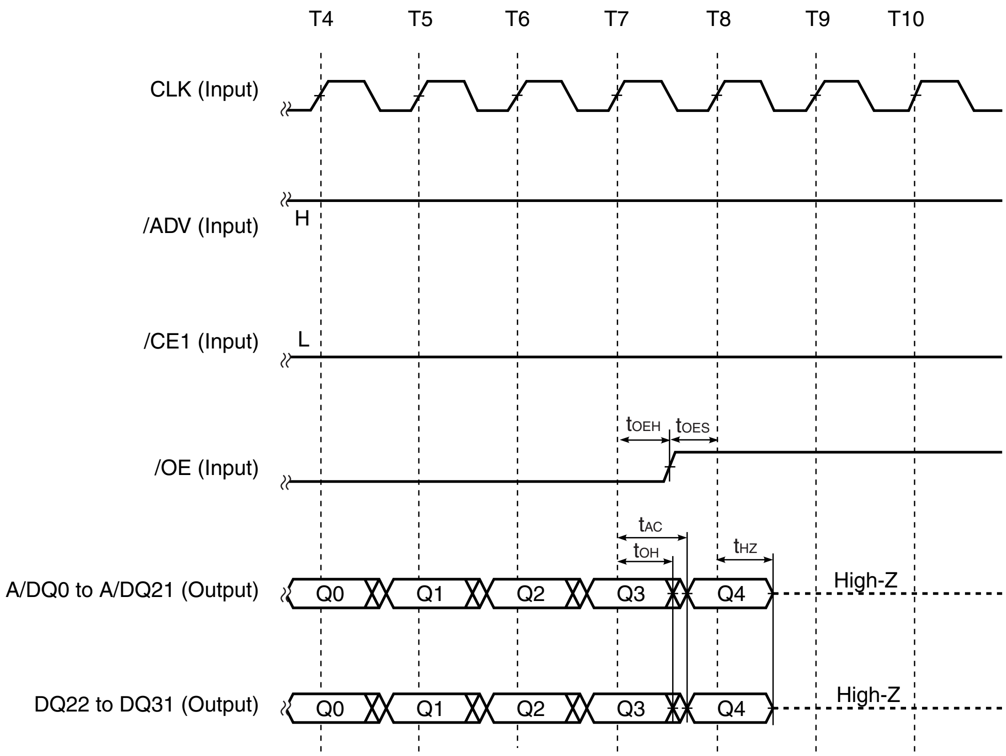
2. Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

5. 4 /OE control during burst read operation

5. 4. 1 /OE HIGH to LOW during burst read operation

The output is controlled depending on the status of /OE (HIGH or LOW) when CLK rises. As shown in **Figure 5-8**, if /OE is made from LOW to HIGH before the rising edge of CLK in T8 during burst read, the read data (Q4) output from the rising edge of CLK in T7 is output. However, the read data that is output from the rising edge of CLK in T8 is not output.

Figure 5-8. /OE HIGH to LOW during burst read operation Timing

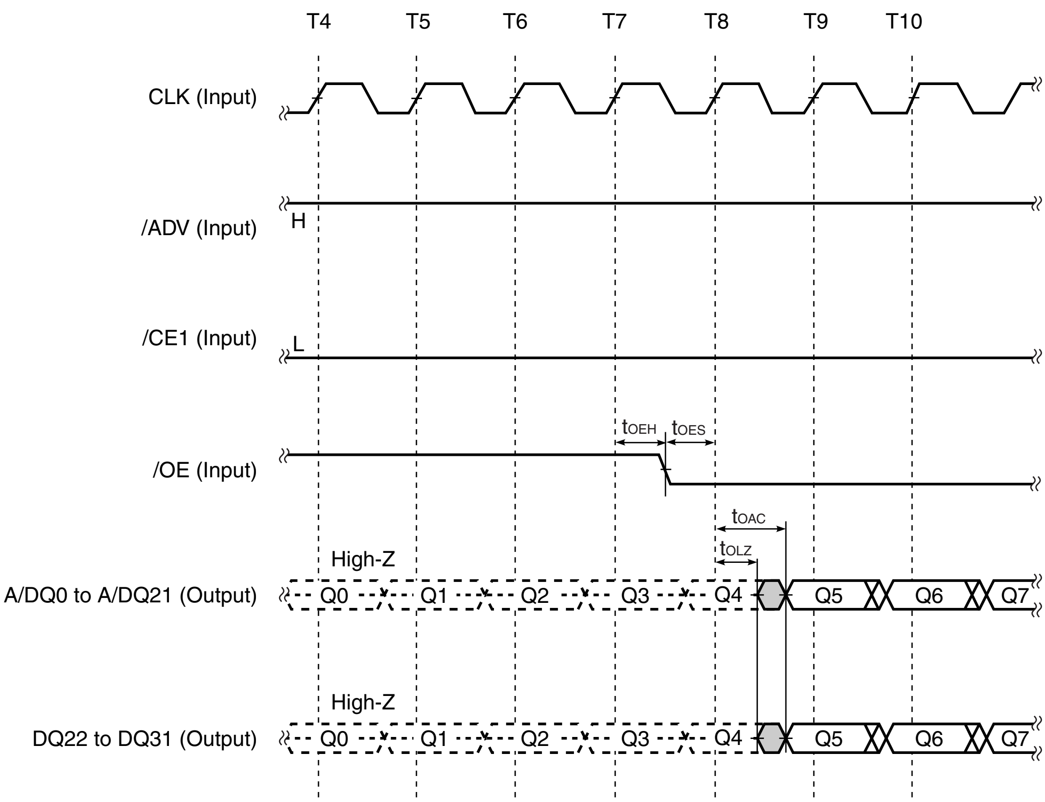


Remark Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

5. 4. 2 /OE LOW to HIGH during burst read operation

The output is controlled depending on the status of /OE (HIGH or LOW) when CLK rises. As shown in Figure 5-9, if /OE is made from HIGH to LOW before the rising edge of CLK in T8 during burst read, the read data (Q5) output from the rising edge of CLK in T8 is output. Because /OE = HIGH until cycle T7, the read data (Q0, Q1, Q2, Q3, and Q4) that should be output when /OE = LOW are not output, but go into a high impedance state.

Figure 5-9. /OE LOW to HIGH during burst read operation Timing



Remark Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification.

5. 5 Write data mask signal (DM) control

This section explains how to control the write data mask signal (DM). DM is a signal that masks input data.

Data mask is valid only in the write cycle. Therefore, data can be masked in the burst write cycle but cannot in the burst read cycle.

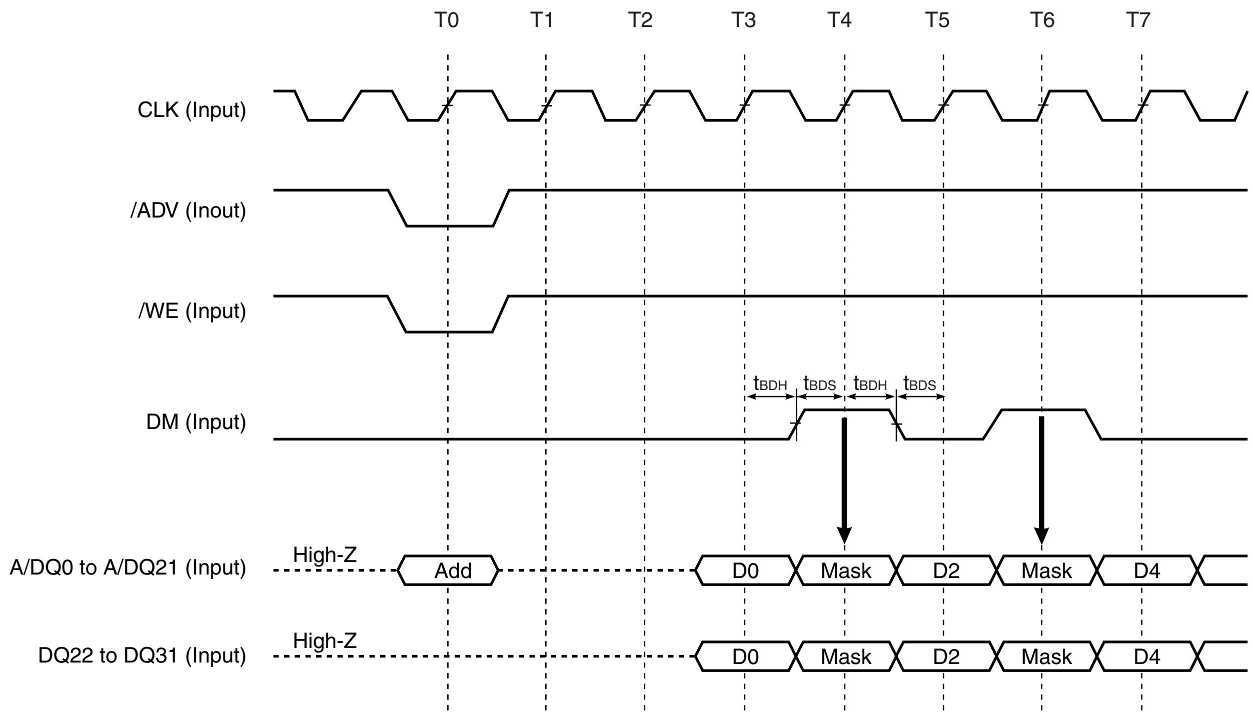
The write data mask signal (DM) controls byte unit with one pin.

- DM0 controls A/DQ7 to A/DQ0.
- DM1 controls A/DQ15 to A/DQ8.
- DM2 controls A/DQ21 to A/DQ16 and DQ23 to DQ22.
- DM3 controls DQ31 to DQ24.

5. 5. 1 Controlling write data mask signal (DM) in write cycle

As shown in **Figure 5-10**, the corresponding write data is masked when the write data mask signal (DM) is HIGH.

Figure 5-10. Command Loading Timing 1



Remark Refer to **6. Electrical Specifications**, **7. Timing Charts** in detail of AC specification

5. 5. 2 Write data mask (DM) truth table

Table 5-1. Write data mask (DM) truth table

Function	DM			
	DM0	DM1	DM2	DM3
All A/DQ and DQ write permission	L			
All A/DQ and DQ write prohibition	H			
A/DQ7 to A/DQ0 write permission	L	×	×	×
A/DQ15 to A/DQ8 write permission	×	L	×	×
DQ23 to DQ22, A/DQ21 to A/DQ16 write permission	×	×	L	×
DQ31 to DQ24 write permission	×	×	×	L
A/DQ7 to A/DQ0 write prohibition	H	×	×	×
A/DQ15 to A/DQ8 write prohibition	×	H	×	×
DQ23 to DQ22, A/DQ21 to A/DQ16 write prohibition	×	×	H	×
DQ31 to DQ24 write prohibition	×	×	×	H

Remark H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

6. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 Note to +2.5	V
Input / Output Supply voltage	$V_{DD}Q$		–0.5 Note to +2.5	V
Input / Output voltage	V_T		–0.5 Note to +2.5	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –1.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD} Note1		1.7	2.0	V
Input / Output Supply voltage	$V_{DD}Q$ Note1		1.7	2.0	V
Input HIGH voltage	V_{IH}		$0.8V_{DD}Q$	$V_{DD}Q$ +0.3	V
Input LOW voltage	V_{IL}		–0.3 Note2	$0.2V_{DD}Q$	V
Operating ambient temperature	T_A		–25	+85	°C

Notes 1. Use same voltage condition (V_{DD} = $V_{DD}Q$).

2. –0.5 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V, Input pins			8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, /WAIT pin			8	pF
Input / Output capacitance	C_{DQ}	V_{DQ} = 0 V, A/DQ, DQ pins			10	pF

Remarks 1. V_{IN} : input voltage, V_{OUT} : output voltage, V_{DQ} : input / output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

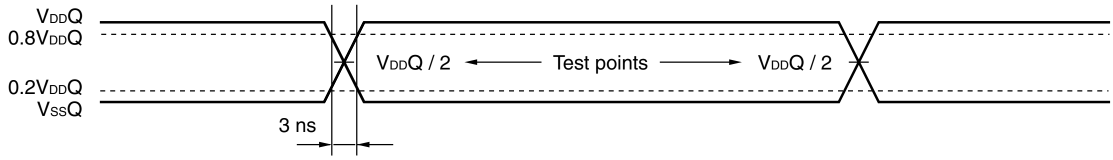
Parameter	Symbol	Test condition		Density of data hold	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to $V_{DD}Q$			–1.0		+1.0	μA
A/DQ, DQ, /WAIT leakage current	I_{LO}	V_{DQ} , V_{OUT} = 0 V to $V_{DD}Q$, /CE1 = V_{IH} or /WE = V_{IL} or /OE = V_{IH}			–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, Burst length = 1, I_{DQ} = 0 mA	frequency = 83 MHz				60	mA
			frequency = 66 MHz				55	
Operating supply Burst current	I_{CCA2}	/CE1 = V_{IL}, Burst length = 8, I_{DQ} = 0 mA	frequency = 83MHz				40	mA
			frequency = 66MHz				35	
Standby supply current	I_{SB1}	/CE1 ≥ $V_{DD}Q$–0.2 V, CE2 ≥ $V_{DD}Q$–0.2 V		128M bits			T.B.D.	μA
	I_{SB2}	/CE1 ≥ $V_{DD}Q$–0.2 V, CE2 ≤ 0.2 V		64M bits			T.B.D.	
				32M bits			T.B.D.	
				16M bits			T.B.D.	
				0M bit			T.B.D.	
Output HIGH voltage	V_{OH}	I_{OH} = –0.5 mA			0.8$V_{DD}Q$			V
Output LOW voltage	V_{OL}	I_{OL} = 1 mA					0.2$V_{DD}Q$	V

Remark V_{IN}: Input voltage, V_{OUT}: output voltage, V_{DQ}: Input / Output voltage

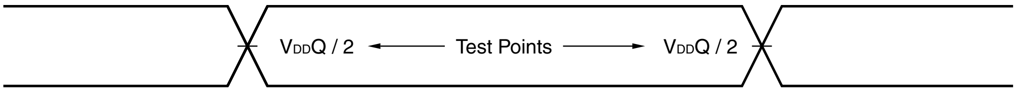
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)



Output Waveform



Output Load

30 pF

Remark C_L includes capacitance of the probe and jig, and stray capacitance.

AC Specifications

(1/2)

Parameter	Symbol	-E12X		-E15X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Clock Specifications							
Cycle frequency	t_{CLK}		83		66	MHz	
CLK HIGH width	t_{CH}	3		3		ns	
CLK LOW width	t_{CL}	3		3		ns	
CLK rise / fall time	t_{CHCL}		3		3	ns	
Address Latching Specifications							
Address hold time from /ADV = HIGH	t_{AH}	1		1		ns	
Address setup time to CLK	t_{ACS}	5		5		ns	
Address hold time to CLK	t_{ACH}	7		7		ns	
/ADV = LOW setup time to CLK	t_{CSV}	5		5		ns	
/ADV = LOW hold time from CLK	t_{CHV}	1		1		ns	
Address setup time to /OE = LOW	t_{AOS}	0		0		ns	
/ADV = LOW pulse width	t_{VPL}	6		6		ns	
/ADV = LOW to next /ADV = LOW	t_{CVCV}		10		10	μs	1
Control Signals Specifications							
/CE1 setup time to CLK	t_{CES}	5		5		ns	
/CE1 hold time to CLK	t_{CEH}	1		1		ns	
/OE setup time to CLK	t_{OES}	5		5		ns	
/OE hold time to CLK	t_{OEH}	1		1		ns	
/WE setup time to CLK	t_{WES}	5		5		ns	
/WE hold time to CLK	t_{WEH}	1		1		ns	

Note 1. t_{CVCV} (MAX.) is applied while /CE1 is being hold at LOW.

(2/2)

Parameter	Symbol	-E12X		-E15X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Specifications							
Burst access time	t_{AC}		8		8	ns	1, 3
Output data hold	t_{OH}	2		2		ns	1
CLK to output in high impedance	t_{HZ}		7		7	ns	2
Write Specifications							
Write data valid of CLK	t_{WDS}	5		5		ns	
Write data hold of CLK	t_{WDH}	1		1		ns	
DM setup time to CLK	t_{BDS}	5		5		ns	
DM hold time to CLK	t_{BDH}	1		1		ns	
/WAIT Specifications							
/WAIT LOW output time from CLK	t_{CEWA}		8		8	ns	1
/WAIT HIGH output time from CLK	t_{CLWA}		8		8	ns	1
/WAIT in high impedance from CLK	t_{CWHZ}		10		10	ns	2
Others							
/OE to output in low impedance	t_{OLZ}	1		1		ns	2
Output time from /OE HIGH to LOW during burst read	t_{OAC}		9		9	ns	1, 3, 4

Notes 1. Output load: 30 pF

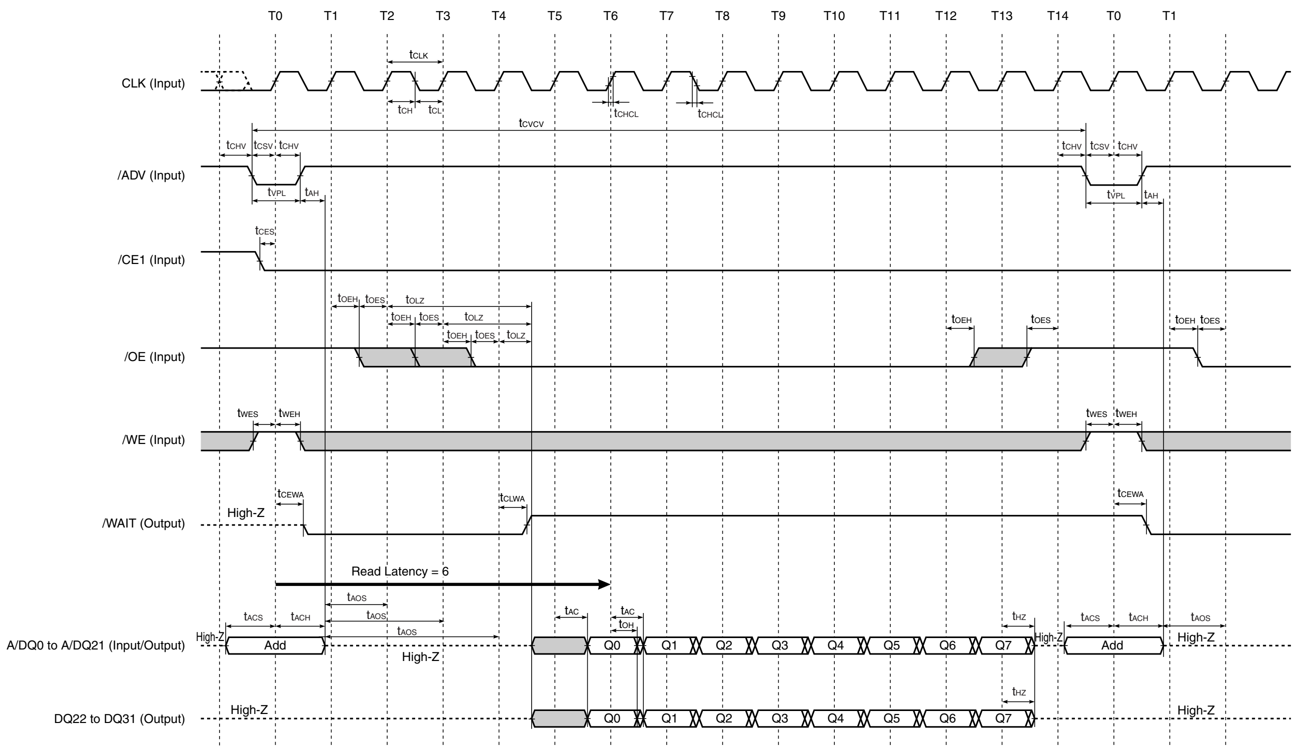
2. Output load: 5 pF

3. In case output driver size is 'Middle'

4. For t_{OAC}, refer to **Figure 5-9.** /OE HIGH to LOW during burst read operation timing.

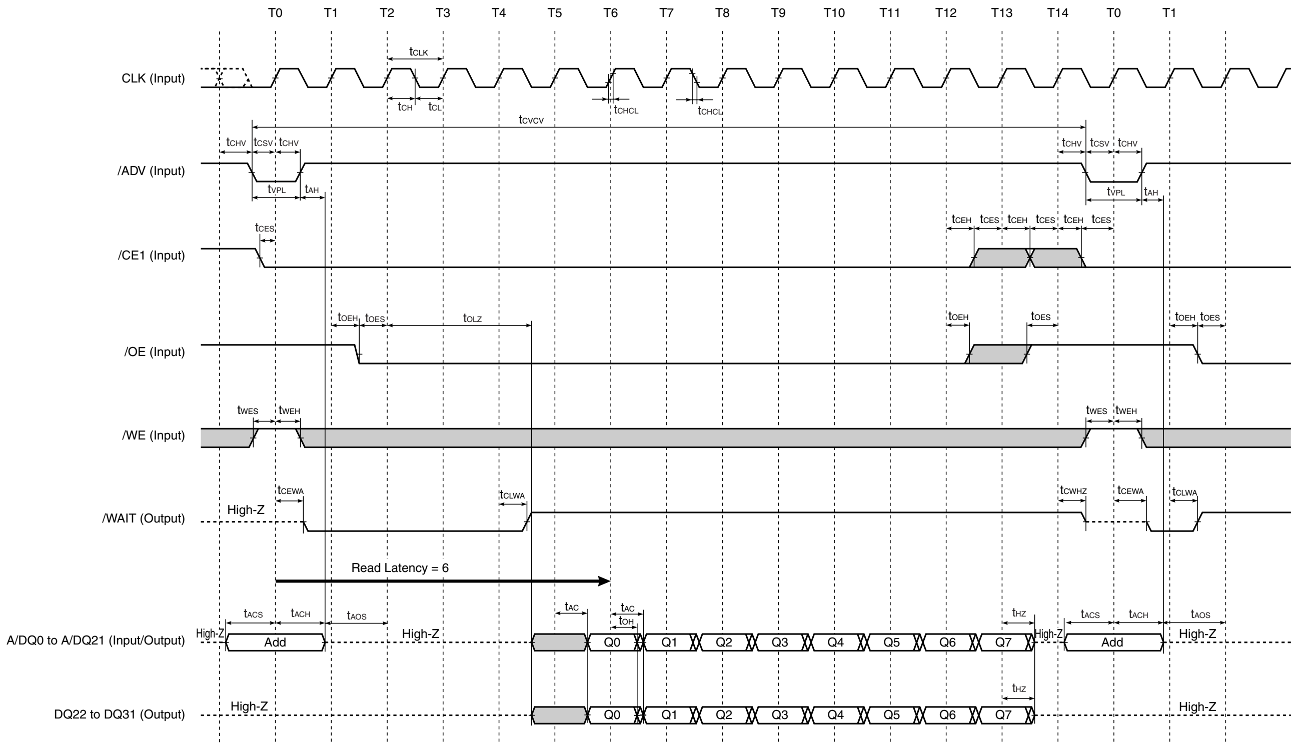
7. Timing Charts

Figure 7-1. Burst Read Cycle Timing Chart (/CE1 = LOW Consecutive Access)



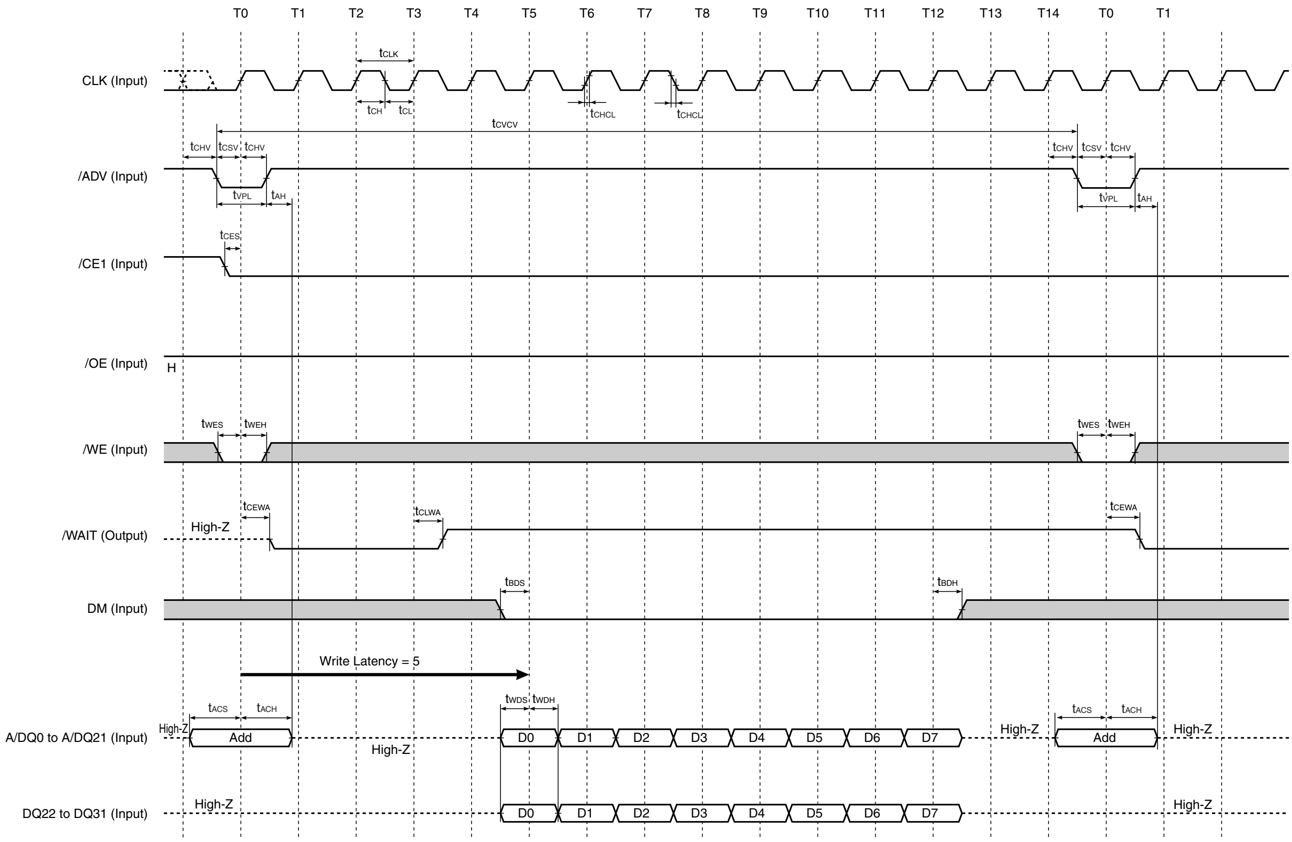
Remark The above timing chart assumes read latency is set 6.

Figure 7-2. Burst Read Cycle Timing Chart (/CE1 Toggle Access)



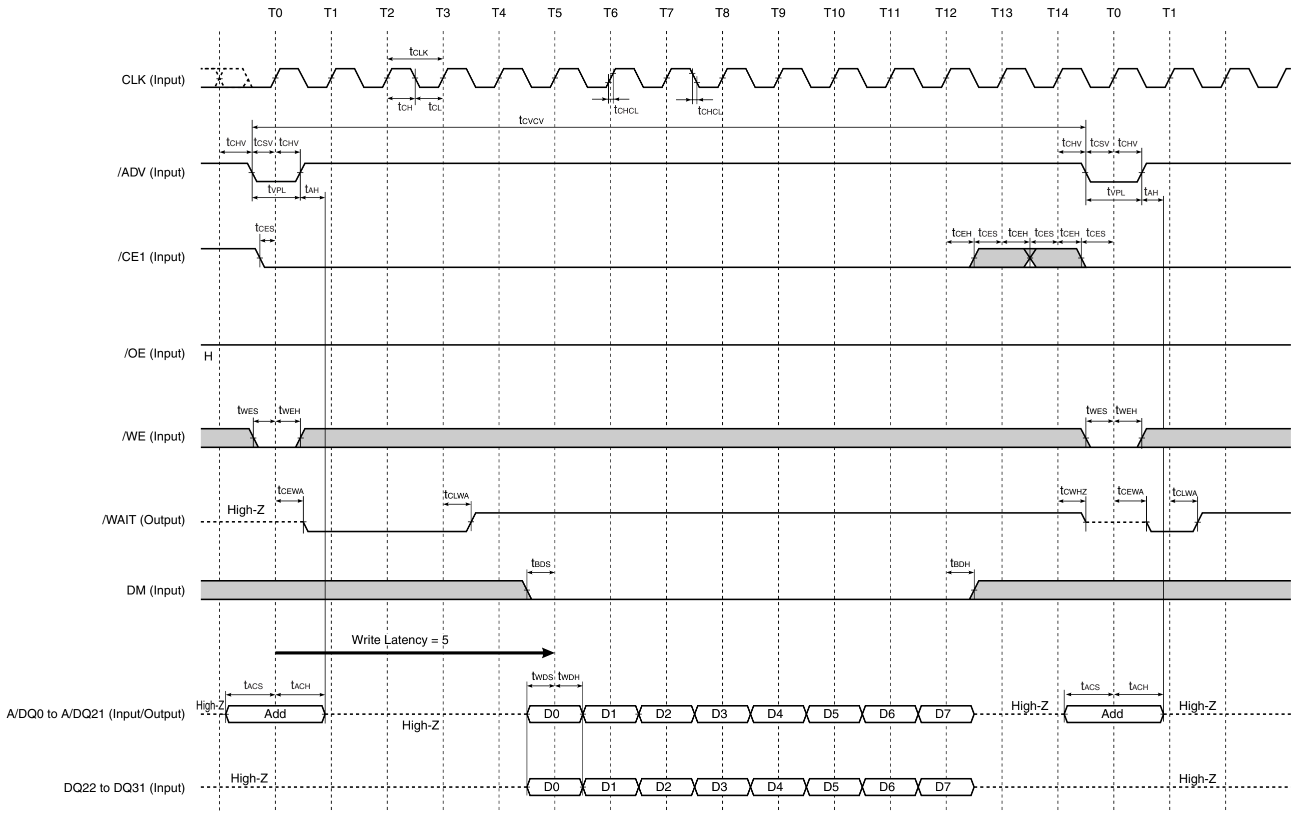
Remark The above timing chart assumes read latency is set 6.

Figure 7-3. Burst Write Cycle Timing Chart (/CE1 = LOW Consecutive Access)



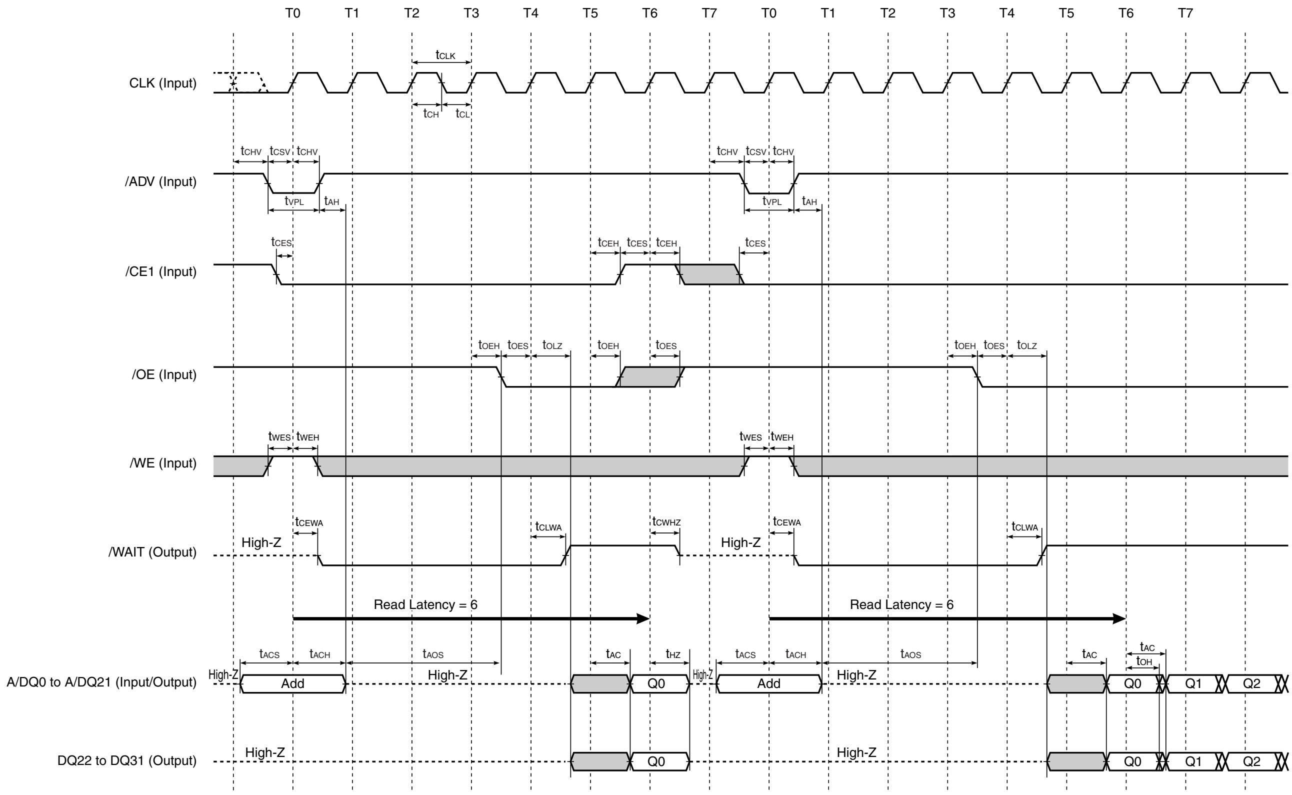
Remark The above timing chart assumes write latency is set 5.

Figure 7-4. Burst Write Cycle Timing Chart (/CE1 Toggle Access)



Remark The above timing chart assumes write latency is set 5.

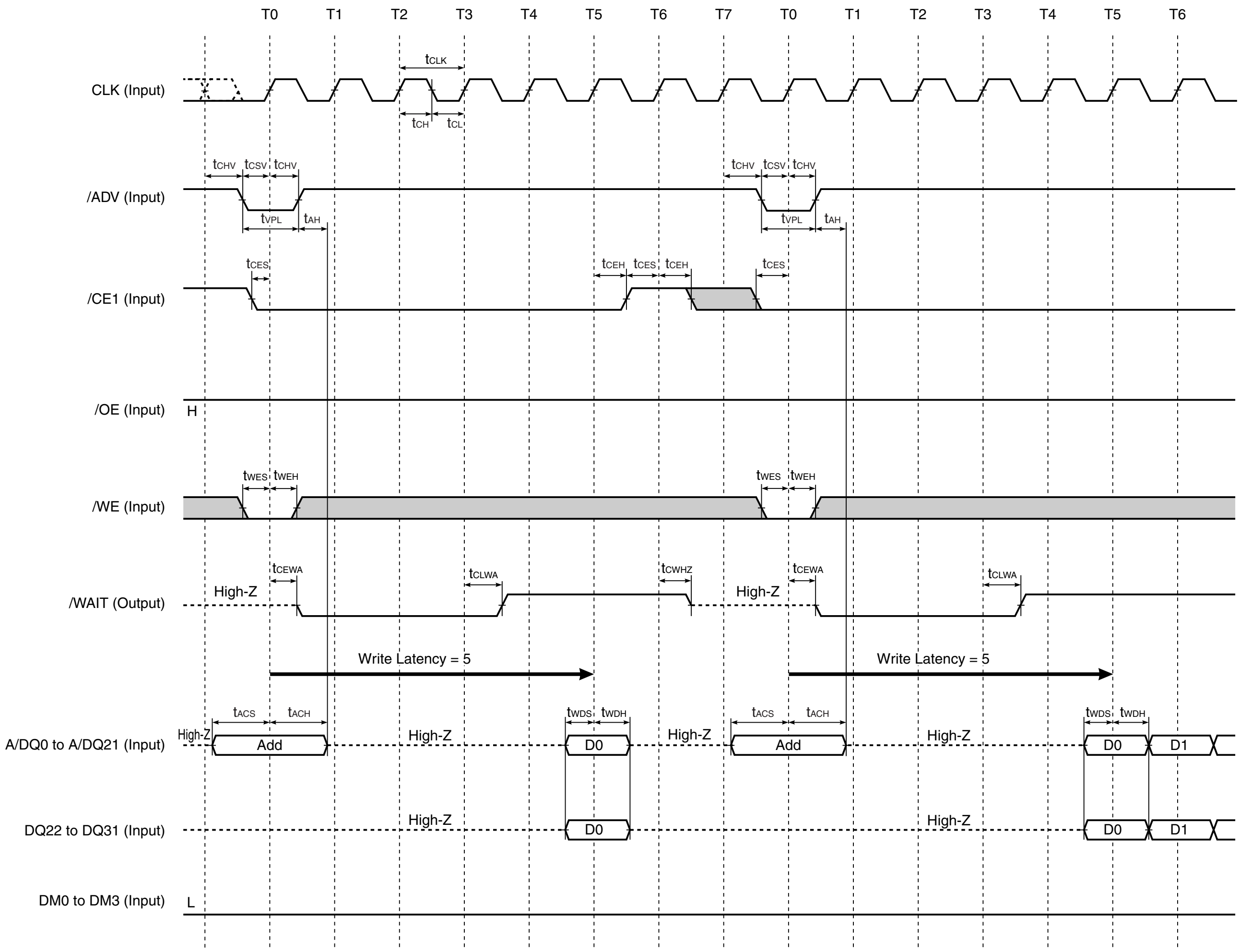
Figure 7-5. Burst Read Termination Cycle Timing Chart (/CE1 Controlled)



Note Burst Read Termination is available after the first read data output.
Figure 7-5 is the minimum cycle at Burst Read Termination to next operation.

Remark The above timing chart assumes read latency is set 6.

Figure 7-6. Burst Write Termination Cycle Timing Chart (/CE1 Controlled)

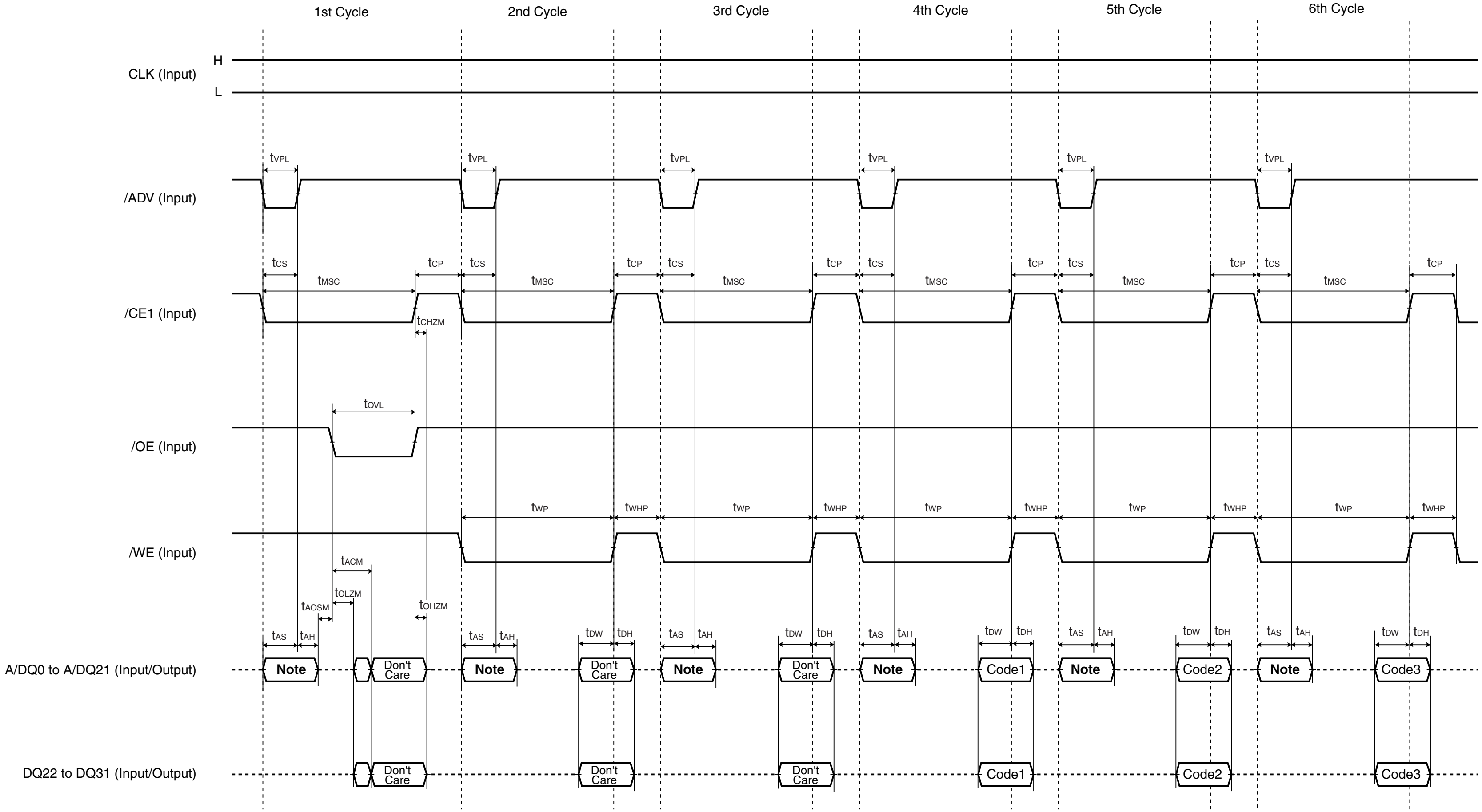


Note Burst Write Termination is available after the first write data input.
Figure 7-6 is the minimum cycle at Burst Write Termination to next operation.

Remark The above timing chart assumes write latency is set 5.

8. 1 Mode Register Setting Timing

Figure 8-1. Mode Register Setting Timing Chart

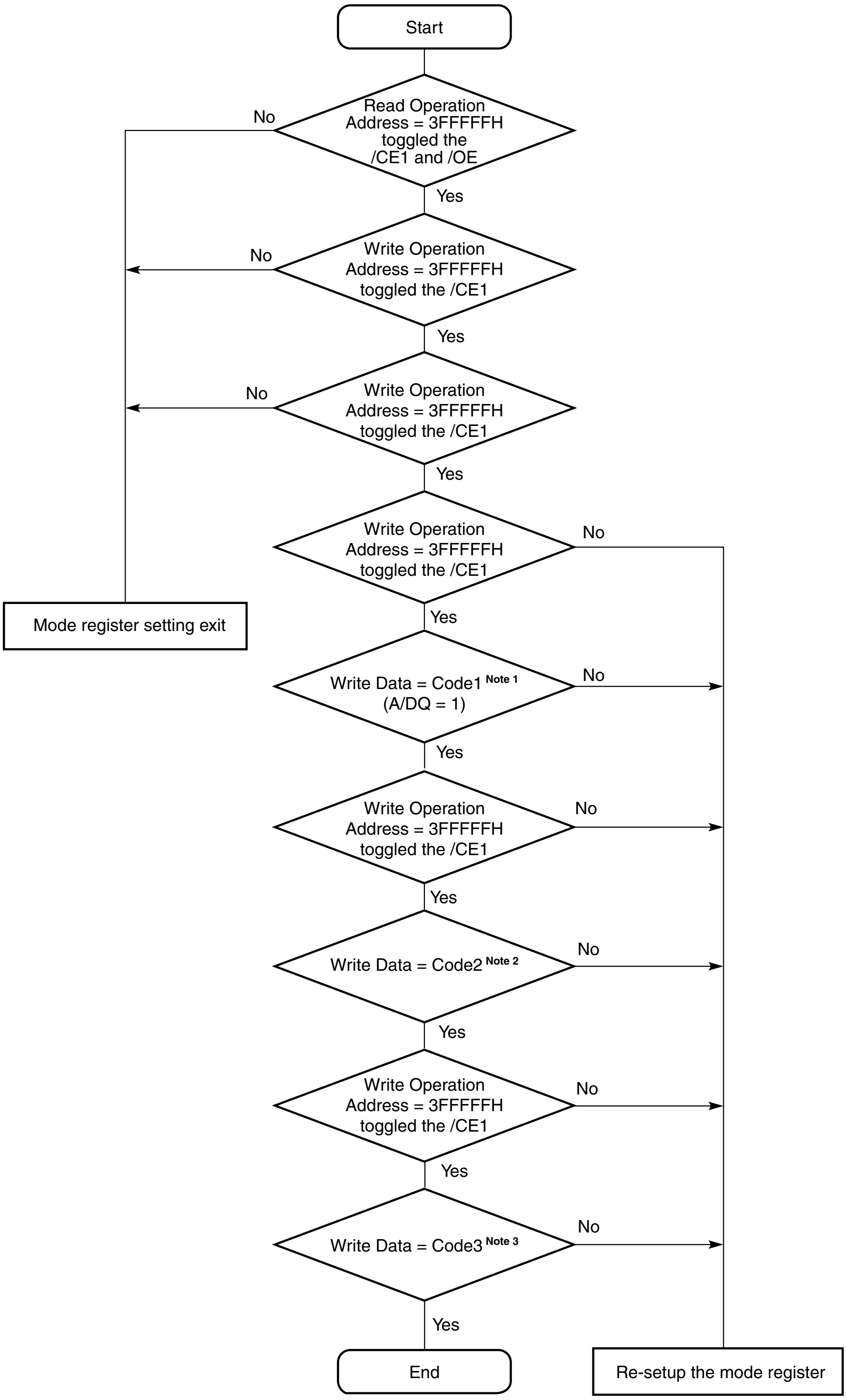


Note Address → All “1” (3FFFFFH)

Remark When setting the mode register, fix CLK to HIGH or LOW. If CLK is toggled, the mode register is not correctly set.
When the mode register is set, DM0 to DM3 are don’t care (HIGH or LOW).

8. 2 Mode Register Setting Flow Chart

Figure 8-2. Mode Register Setting Flow Chart

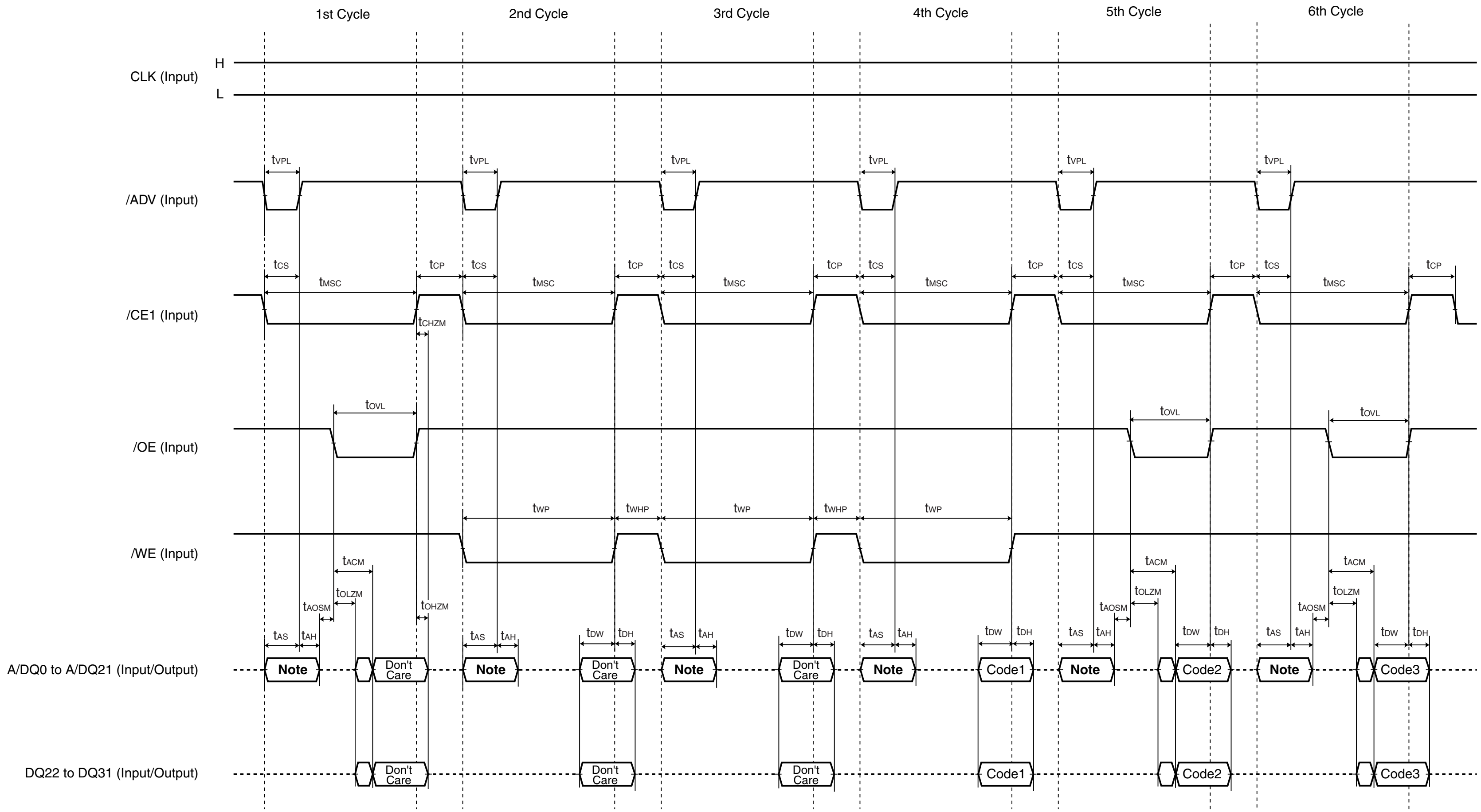


Notes 1. Refer to **Table 4-2**.

2. Refer to **Table 4-3**.

3. Refer to **Table 4-4**.

Figure 8-3. Mode Register Read Timing Chart

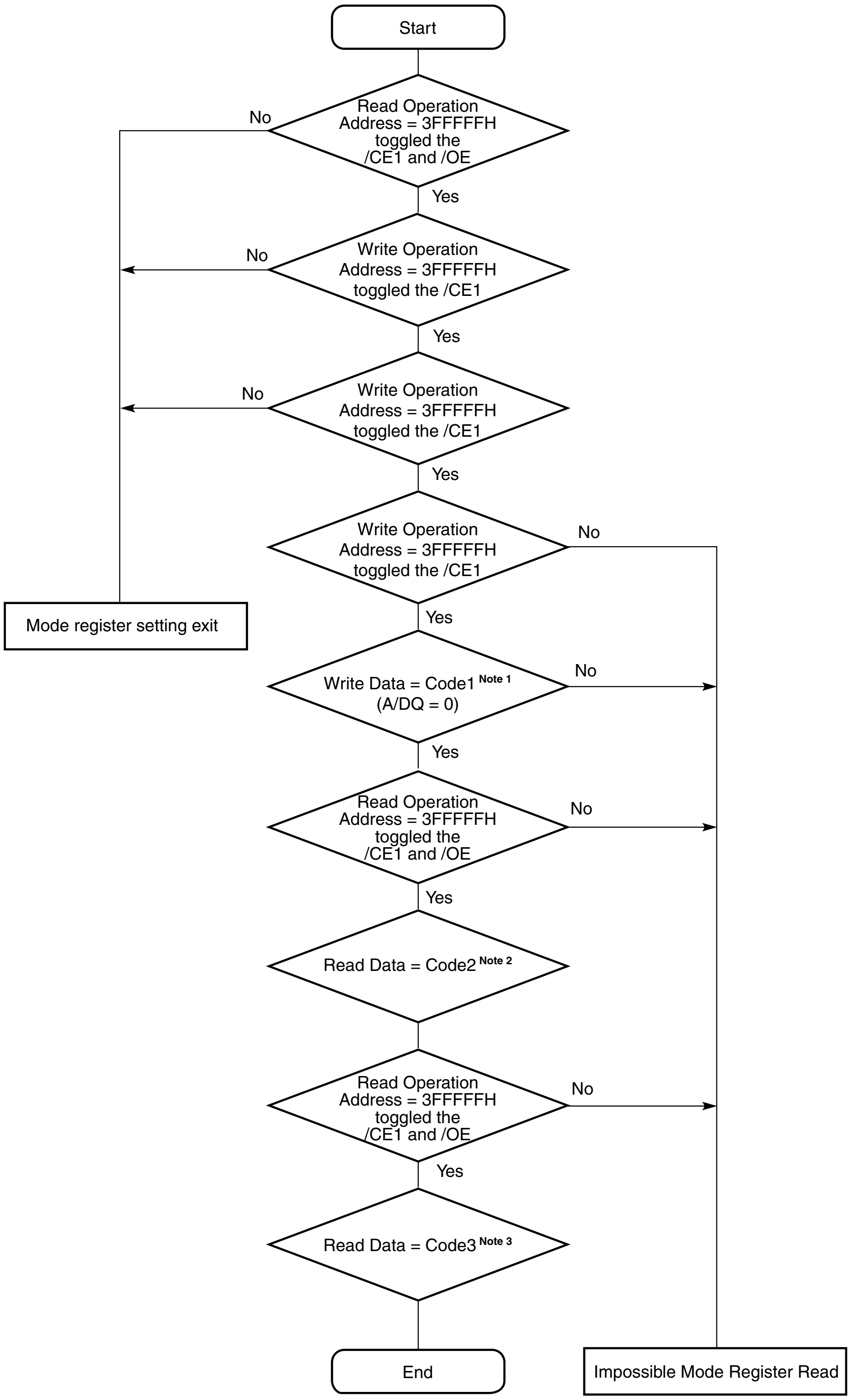


Note Address → All “1” (3FFFFFH)

Remark When setting the mode register, fix CLK to HIGH or LOW. If CLK is toggled, the mode register is not correctly set.
When the mode register is set, DM0 to DM3 are don’t care (HIGH or LOW).

8. 4 Mode Register Read Flow Chart

Figure 8-4. Mode Register Read Flow Chart



Notes 1. Refer to **Table 4-2**.

2. Refer to **Table 4-3**.

3. Refer to **Table 4-4**.

9. Standby Mode Timing Charts

Figure 9-1. Standby Mode 2 (data hold: 64M bits / 32M bits / 16M bits) Entry / Exit Timing Chart

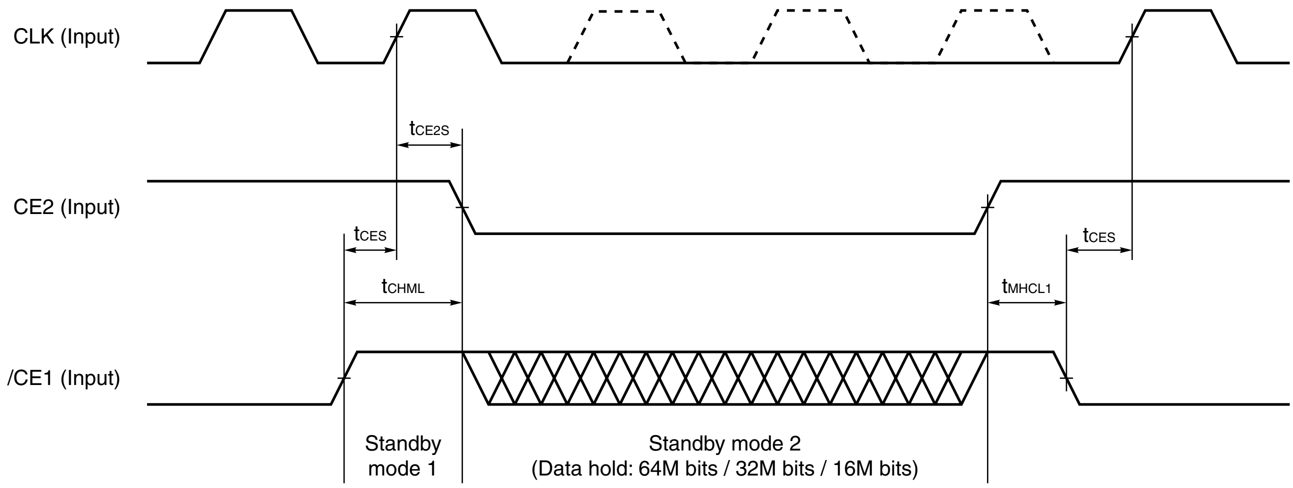
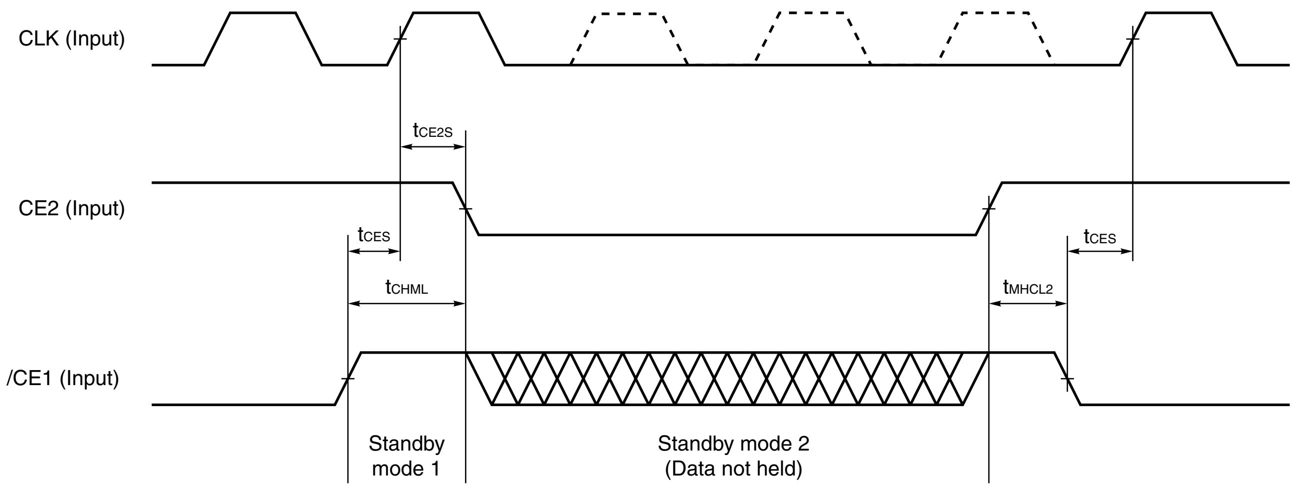


Figure 9-2. Standby Mode 2 (data not held) Entry / Exit Timing Chart



Standby Mode 2 Entry / Exit Timing

Parameter	Symbol	MIN.	MAX.	Unit	Note
Standby mode 2 entry /CE1 HIGH to CE2 LOW	t_{CHML}	0		ns	
Standby mode 2 exit to normal operation CE2 HIGH to /CE1 LOW	t_{MHCL1}	30		ns	1
Standby mode 2 exit to normal operation CE2 HIGH to /CE1 LOW	t_{MHCL2}	300		μs	2
/CE1 setup time to CLK	t_{CES}	5		ns	
CE2 hold time to CLK	t_{CE2S}	1		ns	

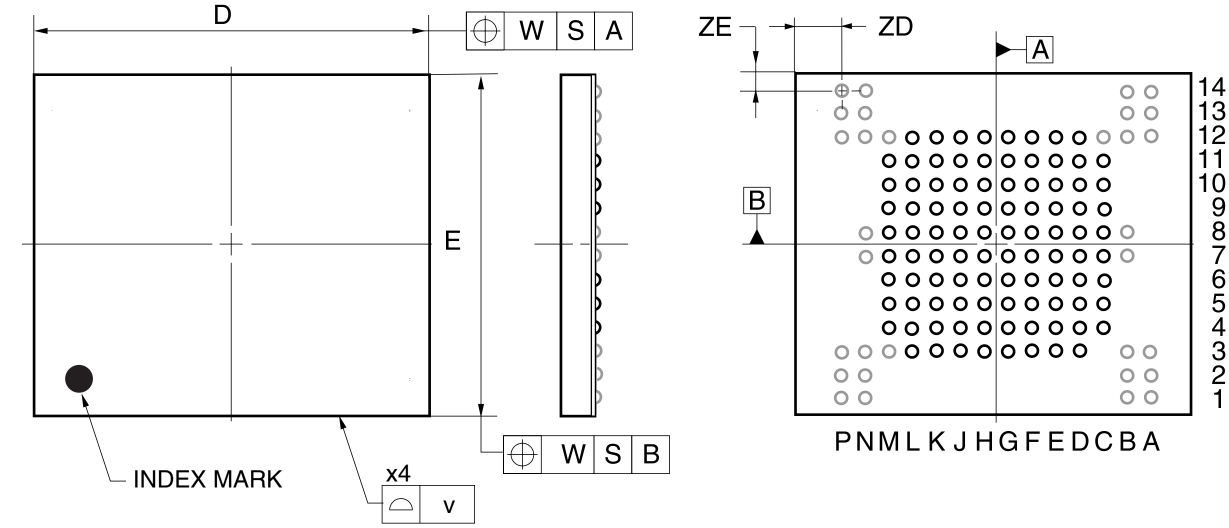
Notes 1. This is the time it takes to return to normal operation from Standby Mode 2 (data hold: 64M bits / 32M bits / 16M bits).

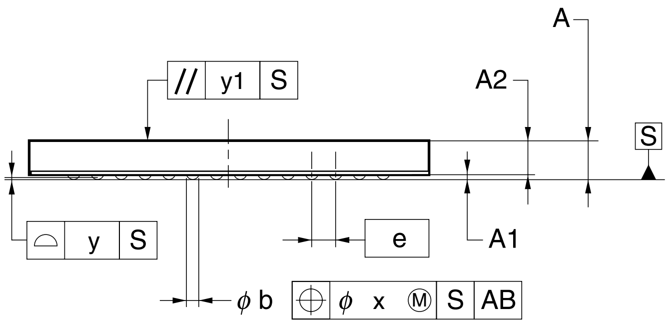
2. This is the time it takes to return to normal operation from Standby Mode 2 (data not held).

10. Package Drawing

The following is a package drawing of package sample.

127-PIN PLASTIC FBGA (13.0x11.5)





This package drawing is a preliminary version. It may be changed in the future.

(UNIT :mm)

ITEM	MILLIMETERS
D	13.00
E	11.50
v	0.15
w	0.20
e	0.80
A	1.50
A1	0.22
A2	1.28
b	0.40
x	0.08
y	0.10
y1	0.20
ZD	1.30
ZE	0.55

11. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD46128953-X.

Type of Surface Mount Device

μPD46128953F1-EB1: 127-pin PLASTIC FBGA (13.0 x 11.5)

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.