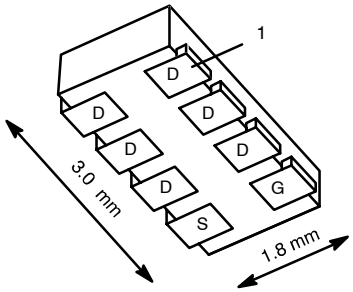
P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.037 @ V_{GS} = -4.5 V	-7.0
	0.048 @ V_{GS} = -2.5 V	-6.1
	0.065 @ V_{GS} = -1.8 V	-5.2

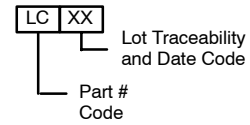
ESD Protected[b]
5000 V

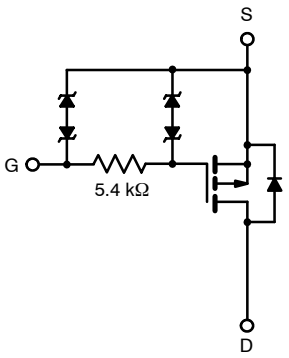
1206-8 ChipFET™



Bottom View

Marking Code





P-Channel MOSFET

Ordering Information: Si5465EDC-T1

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-12		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	-7.0	-5.0	A
	T_A = 85°C		-5.0	-3.6	
Pulsed Drain Current		I_{DM}	-20		
Continuous Source Current[a]		I_S	-2.1	-1.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	1.3	W
	T_A = 85°C		1.3	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature)[c, d]			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	40	50	°C/W
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	20	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. When using HBM. The MM rating is 300 V.
c. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

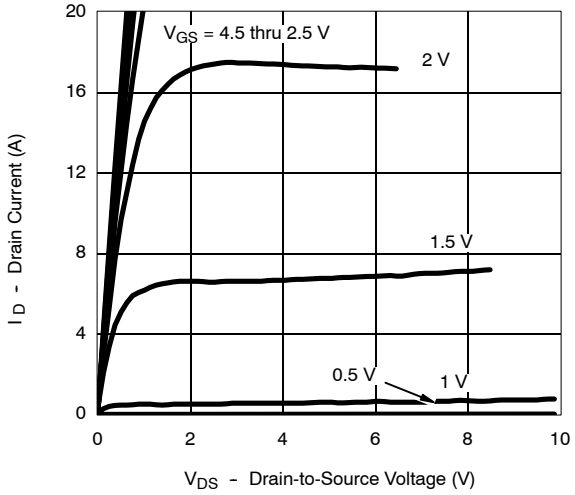
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±1.5	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −9.6 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −9.6 V, V_{GS} = 0 V, T_J = 85°C			−5	μA
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −5.0 A		0.030	0.037	Ω
		V_{GS} = −2.5 V, I_D = −4.5 A		0.040	0.048	Ω
		V_{GS} = −1.8 V, I_D = −2 A		0.052	0.065	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = −5 V, I_D = −5.0 A		15		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.1 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −5.0 A		13.5	20	nC
Gate-Source Charge	Q_{gs}			2.8		nC
Gate-Drain Charge	Q_{gd}			4.5		nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −6 V, R_L = 6 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω		2.5	3.5	μS
Rise Time	t_r			5.7	8.0	μS
Turn-Off Delay Time	$t_{d(off)}$			30	40	μS
Fall Time	t_f			21.5	30	μS

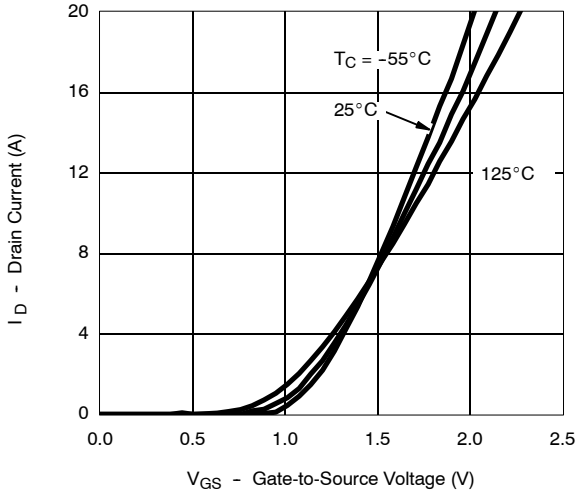
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.μ
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics



Transfer Characteristics



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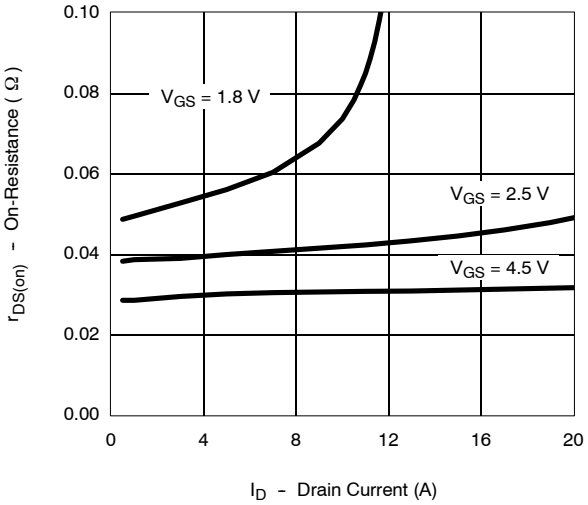
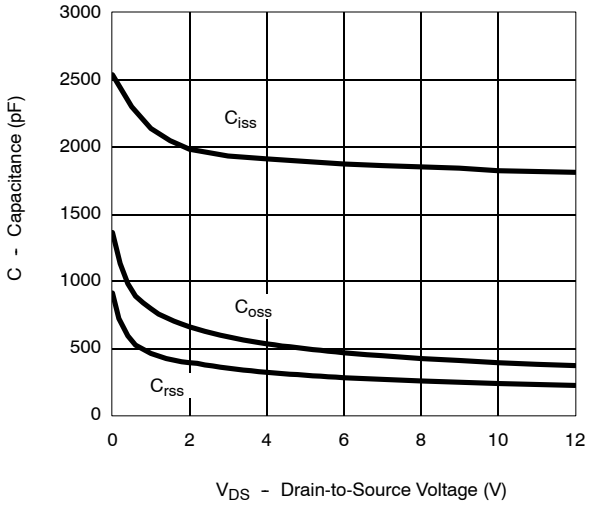
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

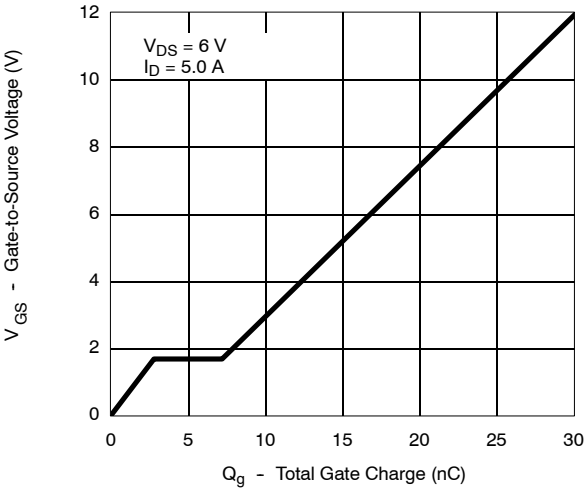
On-Resistance vs. Drain Current



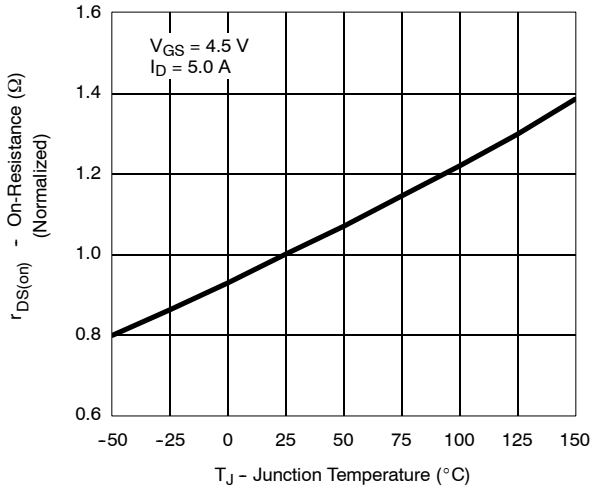
Capacitance



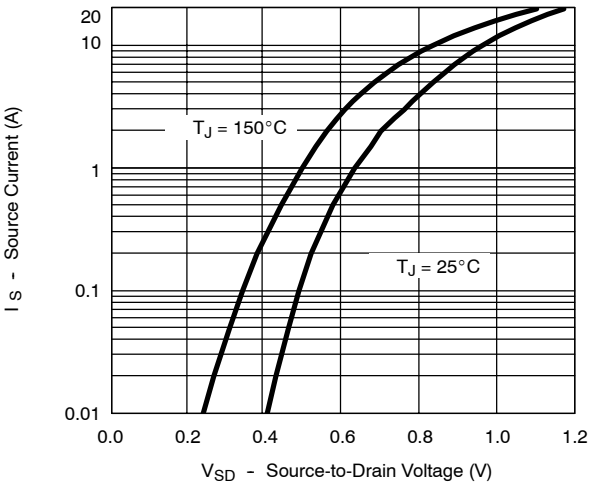
Gate Charge



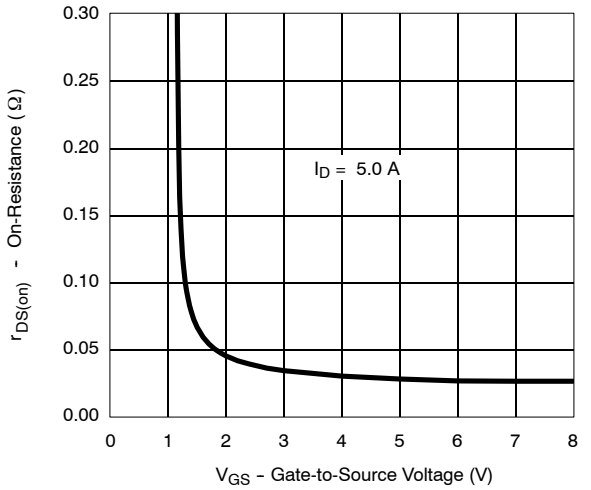
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

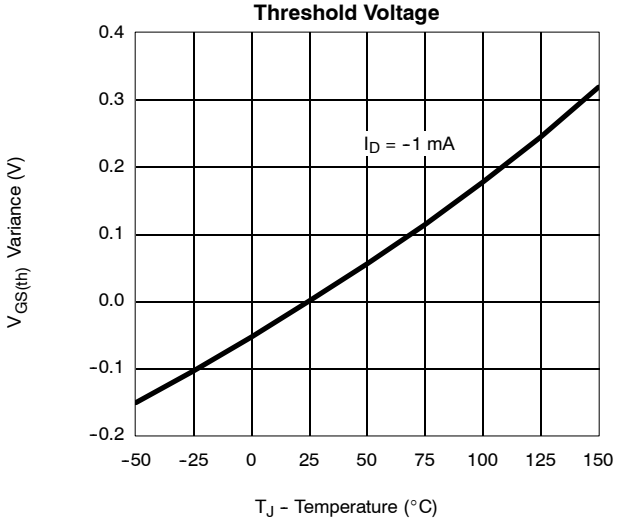


On-Resistance vs. Gate-to-Source Voltage

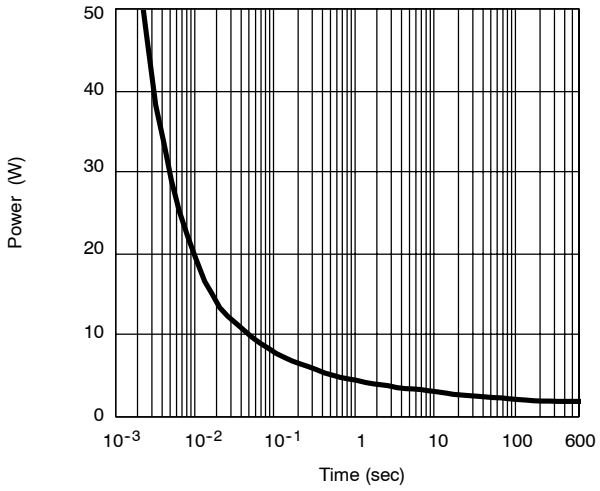


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

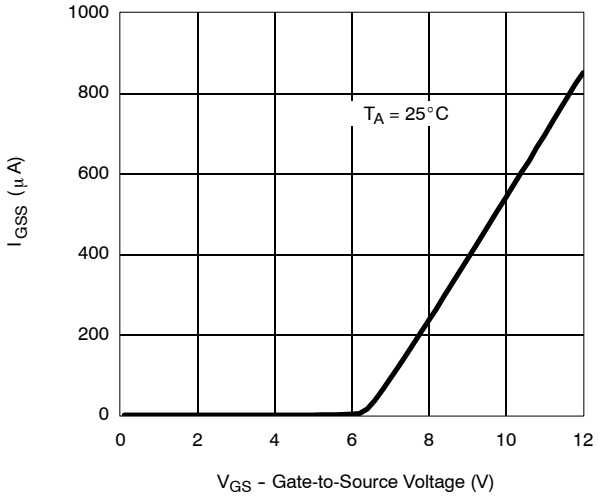
Threshold Voltage



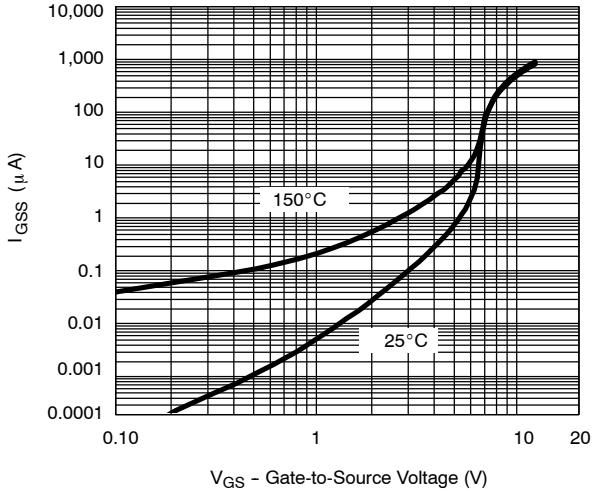
Single Pulse Power



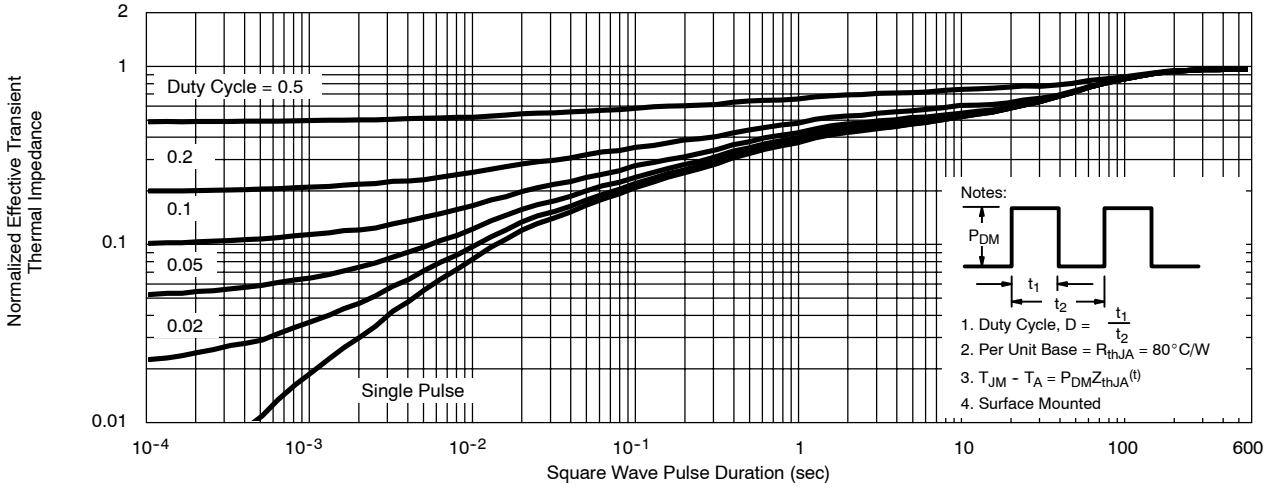
Gate-Source Voltage vs. Gate Current



Gate-Source Voltage vs. Gate Current



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Foot