Preliminary

OKI semiconductor

MSM16851

1,024-Bit SERIAL E²PROM

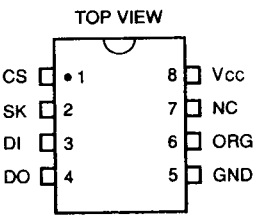
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 × 16 or 128 × 8 user selectable serial memory
- Compatible with CATALYST CAT93C46
- Self-timed programming cycle with Auto-erase
- Word and chip erasable
- Operating range 0°C to 70°C
- 10,000 erase/write cycles for each address
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

8 Pin Dial-In-Line
8 Pin S.O. Package

TOP VIEW

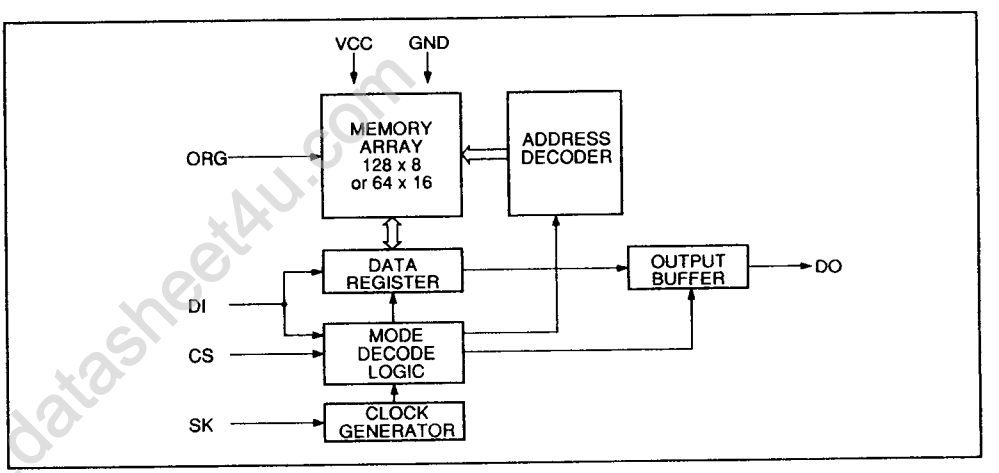


PIN FUNCTIONS

CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
Vcc	+5 V Power Supply
NC	No Connection
GND	Ground

ORG Memory Array Organization Selection Input. When the ORG pin is connected to V_{cc} the 64 × 16 organization is selected. When it is connected to ground the 128 × 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 × 16 organization.

BLOCK DIAGRAM



INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data	
			128 x 8	64 x 16	128 x 8	64 x16
READ	1	1 0	A_6–A_0	A_5–A_0		
ERASE	1	1 1	A_6–A_0	A_5–A_0		
WRITE	1	0 1	A_6–A_0	A_5–A_0	D_7–D_0	D_{15}–D_0
EWEN	1	0 0	11xxxxx	11xxxx		
EWDS	1	0 0	00xxxxx	00xxxx		
ERAL	1	0 0	10xxxxx	10xxxx		
WRAL	1	0 0	01xxxxx	01xxxx	D_7–D_0	D_{15}–D_0

Power-On Data Protection Circuitry: During power-up, all modes of operation except READ mode are inhibited until Vcc reaches a level of approximately 3.5 V. During power-down, the source data protection circuitry inhibits all modes except READ mode when Vcc falls below the voltage range of approximately 3.5 V.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ Vcc + 0.3	V
Output Voltage	V_O		−0.3 ~ Vcc + 0.3	V
Storage Temperature	T_{STG}		−55 ~+150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10%	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

(Vcc = 4.5V to 5.5V, Ta = 0°C ~ 70°C, unless otherwise specified.)

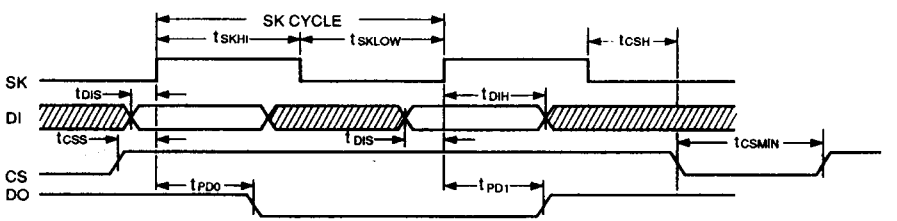
Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	Vcc = 5.0V CS = 5.0V DI = SK = 0.0V or Vcc DO = OPEN		3	mA
	I_{CC2}	Vcc = 5.5 V CS = 0 DO = ORG = OPEN DI = 0 SK = 0		100	µA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	Vcc+1	V
"L" Output Voltage	V_{OL}	I_{OL} = 2.1mA		0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −400µA	2.4		V
Input Leakage Current	I_{LI}	V_{in} = Vcc +0.1V		10	µA
Output Leakage Current	I_{LO}	V_{out} = Vcc CS = 0		10	µA

AC CHARACTERISTICS

(V_{CC} = 4.5V ~ 5.5V, Ta = 0°C ~ 70°C)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
t_{CSS}	CS Set up Time		50			ns
t_{CSH}	CS Hold Time		0			ns
t_{DIS}	DI Setup Time		100			ns
t_{DIH}	DI Hold Time		100			ns
t_{PD1}	Output Delay to 1	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V			500	ns
t_{PD0}	Output Delay to 0				500	ns
t_{HZ}	Output Delay to HiZ			100		ns
t_{EW}	Erase / Write Pulse Width				10	ms
t_{CSMIN}	Min CS Low Time		250			ns
t_{SKHI}	Min SK High Time		250			ns
t_{SKLOW}	Min SK Low Time		250			ns
t_{SV}	Output Delay to Status Valid	C_L = 100 pF				ns
SK_{MAX}	Maximum Frequency		DC		700	kHz

Synchronous Timing



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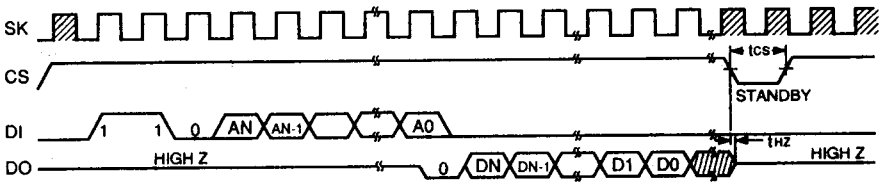
DEVICE OPERATION

The MSM16851 has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical 1, an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).
The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.
During power-up, all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction must be issued before starting to program.
At power-down, when Vcc falls below a level of approximately 3.5 V, the data protection circuitry inhibits operation, except READ mode, and an EWDS instruction is executed internally.

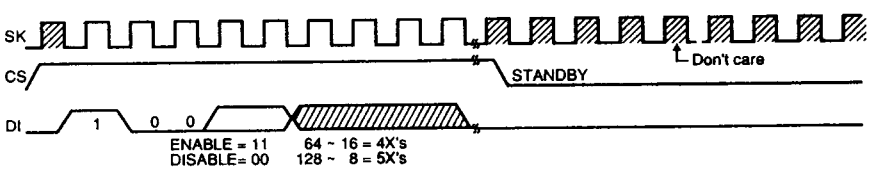
READ



Organization	A_N	D_N
128 × 8	A_6	D_7
64 × 16	A_5	D_{15}

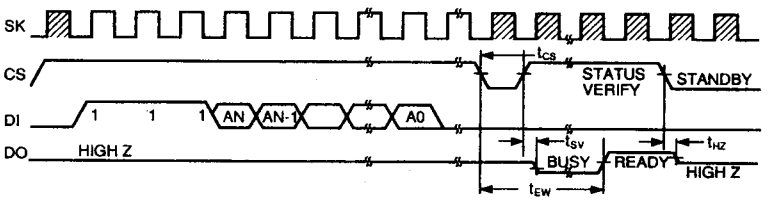
The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical 0) precedes the output data string.

EWEN/EWDS (Erase Write Enable/Erase Write Disable)



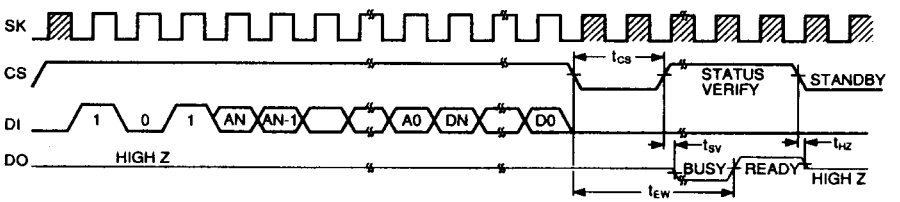
After power-up and before starting any programming instruction, the EWEN instruction must be issued. Once it is issued, it remains active until an EWDS instruction takes place. The EWDS instruction prevents accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

ERASE



After an ERASE instruction is shifted in. CS is dropped low. This sets the beginning of the self timed erase sequence. If CS is then brought high (after observing t_{CS} spec) the DO pin acts as a status indicator. It remains low so long as the chip is programming. It goes high after all the bits of the addressed register are set to a logical 1.

WRITE



After a WRITE instruction is shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This sets the beginning of the self timed programming sequence. If CS is brought high during the programming time (after observing the tcs specification), the DO pin acts as a status indicator – it remains low so long as the chip is programming. It goes high after all the bits of the addressed register are set to their proper values. With the MSM16851 it is not necessary to erase a memory location before the WRITE instruction.

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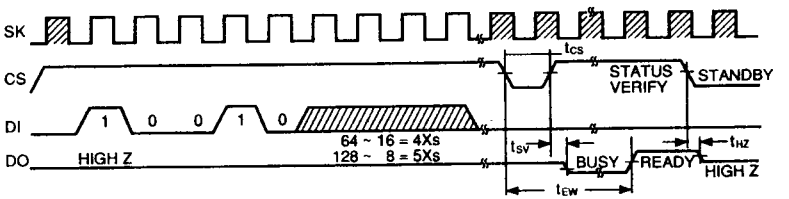
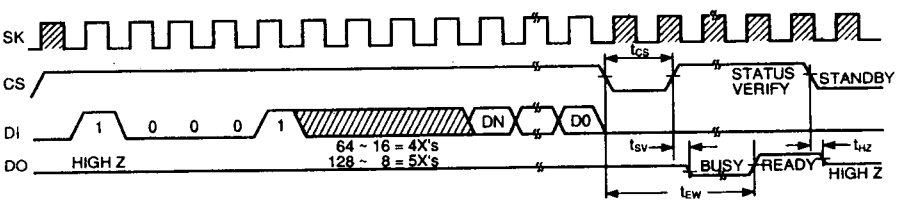
Organization	AN	DN
128 × 8	A6	D7
64 × 16	A5	D15

ERAL (Erase All)



The ERAL instruction erases the whole chip. Except for its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRAL (Write All)



The WRAL instruction writes to all the registers simultaneously. All the registers must be erased before a WRAL operation. Except for its different opcode, the WRAL instruction is identical to the WRITE instruction.