VISHAY

N- and P-Channel Dual Enhancement-Mode MOSFET

CHARACTERISTICS

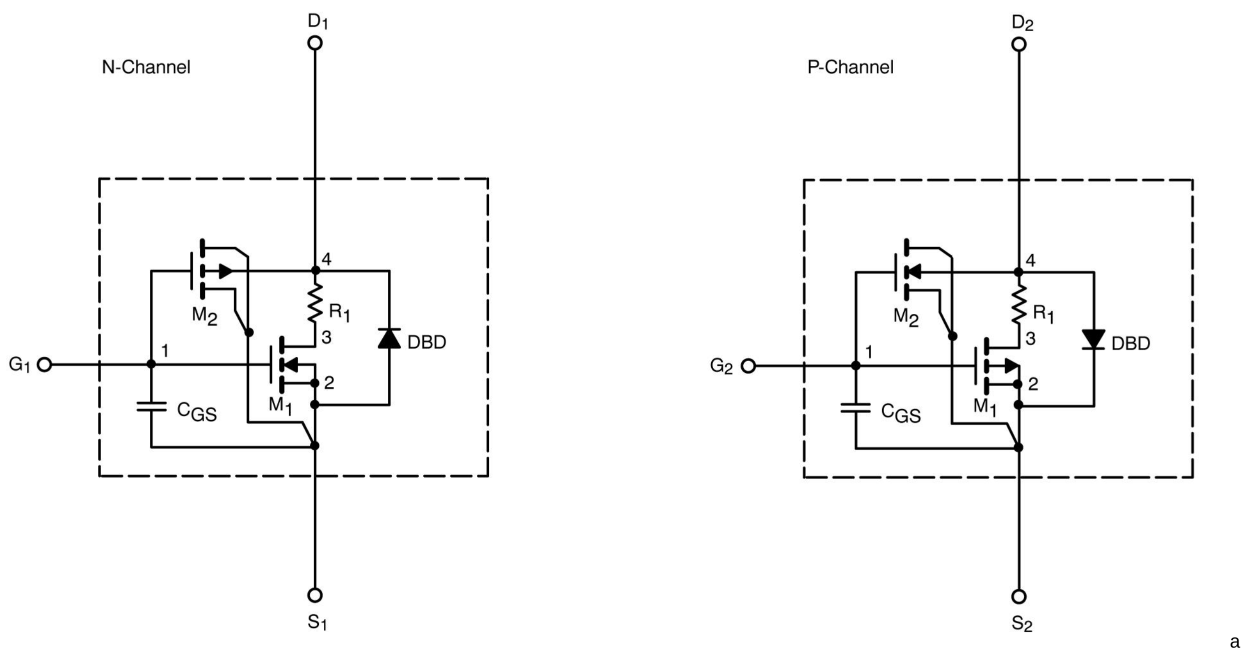
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The model subcircuit is extracted and optimized over the –55 to 125°C temperature ranges under the pulsed 0 to 5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



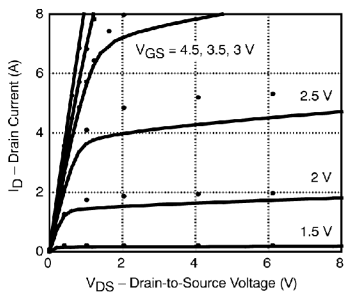
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

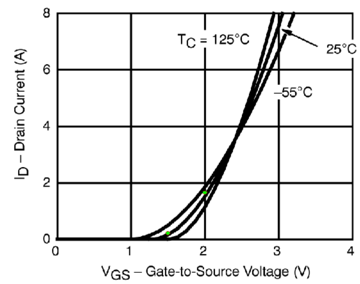
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Conditions**		**Typical**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V, V_{GS}, I_D = 250 µA	N-Ch	1.02	V
		V_{DS} = V, V_{GS}, I_D = –250 µA	P-Ch	1.15	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} 5 V, V_{GS} = 4.5 V	N-Ch	23	A
		V_{DS} = –5 V, V_{GS} = –4.5 V	P-Ch	18	
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1.9 A	N-Ch	0.112	Ω
		V_{GS} = –4.5 V, I_D = –1.7 A	P-Ch	0.154	
		V_{GS} = 3 V, I_D = 1.5 A	N-Ch	0.149	
		V_{GS} = –3 V, I_D = –1.3 A	P-Ch	0.217	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 1.9 A	N-Ch	5	S
		V_{DS} = –15 V, I_D = –1.7 A	P-Ch	4.1	
Diode Forward Voltage[a]	V_{SD}	I_S = 1 A, V_{GS} = 0 V	N-Ch	0.77	V
		I_S = –1 V, V_{GS} = 0 V	P-Ch	–0.77	
Dynamic[b]					
Total Gate Charge	Q_g	N-Channel V_{DS} = 3.5 V, V_{GS} = 4.5 V, I_D = 0.3 A P-Channel V_{DS} = –3.5 V, V_{GS} = –4.5 V, I_D = –0.3 A	N-Ch	1.6	nC
			P-Ch	3	
Gate-Source Charge	Q_{gs}		N-Ch	0.41	
			P-Ch	0.76	
Gate-Drain Charge	Q_{gd}		N-Ch	0.26	
			P-Ch	0.70	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 3.5 V, R_L = 11.5 Ω $I_D \cong$ 0.3 A, V_{GEN} = 4.5 V, R_G = 6 Ω P-Channel V_{DD} = –3.5 V, R_L = 11.5 Ω $I_D \cong$ –0.3 A, V_{GEN} = –4.5 V, R_G = 6 Ω	N-Ch	5.2	ns
			P-Ch	6	
Rise Time	t_r		N-Ch	6.2	
			P-Ch	10	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch	9	
			P-Ch	11	
Fall Time	t_f		N-Ch	15	
			P-Ch	22	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1 A, di/dt = 100 A/µs	N-Ch	31	
		I_F = –1 A, di/dt = 100 A/µs	P-Ch	30	

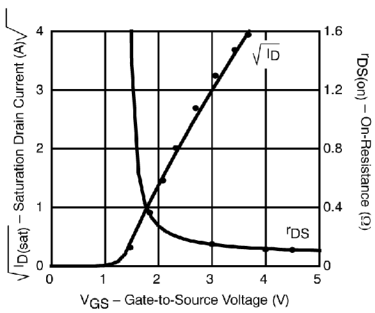
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

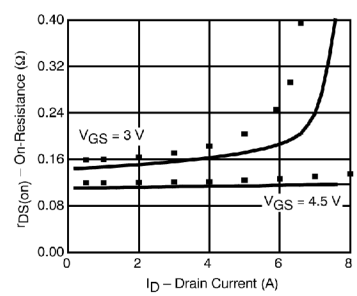
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

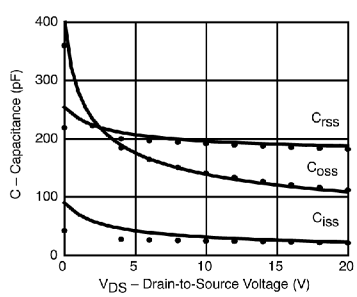
N-CHANNEL MOSFET

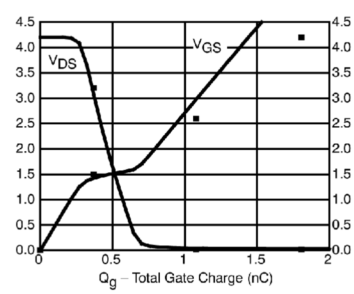












Note: Dots and squares represent measured data.

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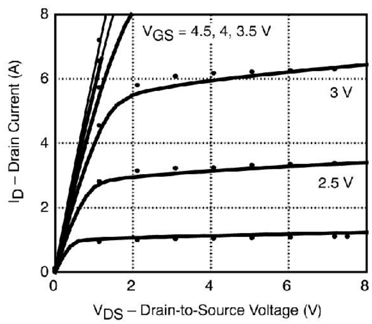
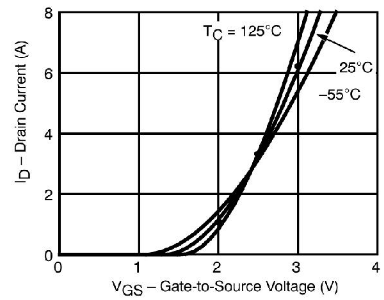
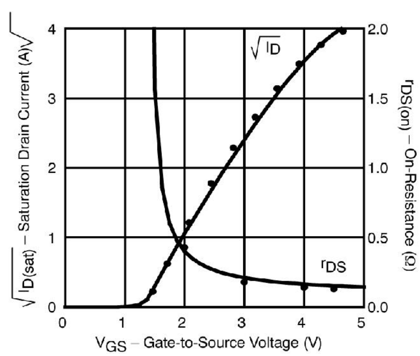
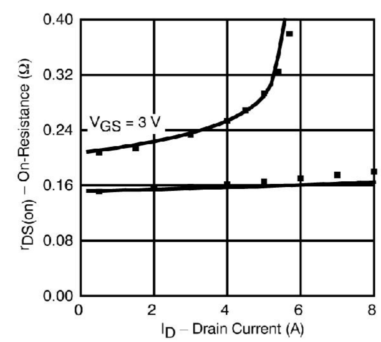
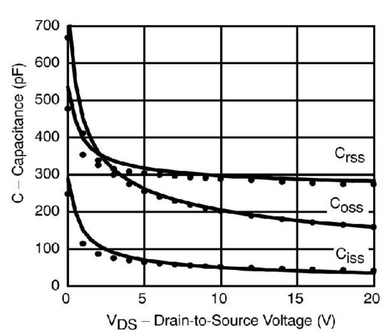
P-CHANNEL MOSFET

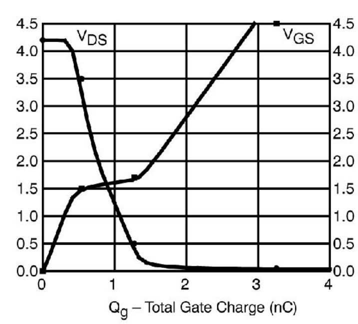












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