TE3-FALC

T3/E3 Framer & Line Interface for ATM, Frame Relay & PPP/IP

PEF 3460 E, Version 1.2

Wired Communications

Infineon technologies

Never stop thinking.

Product Overview

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Page	**Subjects (major changes since last revision)**

The information in this document is subject to change without notice.

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1 Overview

This Product Overview provides an overview about the functionality of the "T3/E3 Framer & Line Interface for ATM, Frame Relay & PPP/IP" TE3-FALC (PEF 3460 E).

Note: Some features mentioned in this document are options for future firmware enhancements and not supported with the current release of firmware. These options are marked with a preceding "✧" symbol.

The TE3-FALC is a complete solution for a T3/E3 broadband interface. It includes DS3/E3 framing, analog line interface, two jitter attenuators and the mapping of ATM or HDLC-framed PPP. The TE3-FALC also integrates a microcontroller which handles the device configuration, processes alarms and gathers statistics in accordance with the relevant managed MIB objects. A firmware image needs to be uploaded as part of the initialization of the device.

On line side the TE3-FALC interfaces to a 75 ohm co-axial cable via transformers. Highly accurate analog pulse shaping removes the need to measure cable length and set the Line Build Out.

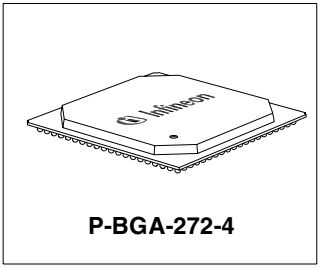
On the system side, industry standard UTOPIA and POS-PHY interface as well as UTOPIA-L2X and serial clock/data port are provided. This allows the TE3-FALC to be connected to a wide array of Layer 2/3 & 4 network processors.

TE3-FALC **PEF 3460 E**

T3/E3 Framer & Line Interface for ATM, Frame Relay & PPP/IP

Version 1.2

1.1 Features



P-BGA-272-4

General Features

- Integrated T3/E3 LIU for recovery of analog signals from the line and the transmission of signals onto the line via a transformer.
- Flexible main clock input accepting any frequency between 4 and 52 MHz.
- Integrated transmit and receive jitter attenuators
- Integrated transmit clock multiplier to enable a wide number of transmit reference clocks (optional) to be used from 8 kHz to 52 MHz
- Integrated receive clock multiplier to enable a wide number of receive reference clocks (optional) to be used from 8 kHz to 52 MHz
- Integrated receive reference clock multiplier
- DS3 M23 and C-Bit Parity framer with overhead bit processing.
- E3 G.832 framer with overhead byte processing.
- E3 G.751 framer with overhead bit processing.
- Integrated Bit Error Rate Tester (BERT)
- ATM TC layer allowing the direct mapping/extraction of ATM cells into/from the DS3 or E3 frame.
- ATM DS3/E3 G.751 PLCP function allowing the mapping of ATM cells into the DS3/ E3 G.751 frame using the PLCP sub-frame.
- Single channel HDLC controller allowing the mapping/extraction of bit or byte mapped HDLC encapsulated packet from either the DS3 or E3 frame
- Flexible 16/8-bit Packet Stream Interface (PSI) allowing connection to industry standard UTOPIA and POS-PHY as well as UTOPIA-L2X interfaces.
- Integrated micro-controller with associated code/data RAM to allow communication with the device to be achieved by 'high level' commands and status information, hence significantly reducing the software required to control the device.
- Integrates a 16/8-bit switchable Intel or Motorola style microprocessor interface.
- JTAG boundary scan according to IEEE 1149.1 (5 pins).

Type	Package
PEF 3460 E	P-BGA-272-4

- 0.18 µm, 1.8 V low power core technology
- I/Os are 3.3 V tolerant and have 3.3 V driving capability
- Package P-BGA-272-4 (27 mm x 27 mm; pitch 1.27 mm)
- Full scan path and BIST of on-chip RAMs for production test
- Power consumption: ~ 900 mW (typ.)

Analog Interface

- Supports clock recovery on B3ZS and HDB3 line coding.
- Meets jitter input tolerance according to GR-499-CORE (Cat. 1 & 2), ITU-T G.823, G.824 and ETSI TBR24.
- Meets jitter output requirements according to GR-499-CORE and ETSI TBR24.
- Performs jitter attenuation of receive clock when in loop timed mode for terminal applications in compliance to GR-499-CORE and TBR24.
- Pulse shaper meets templates according to ANSI T1.102 & 404, GR-499-CORE, ITU-T G.703.
- Maximum line length up to 1100 ft. (using standard coaxial cable, for example AT&T 728A, 734A or 734D)
- Single RC interface to transformer for both T3 and E3.
- External line length selection (LBO) is not required
- Provides PLL for transmit clock duty cycle correction.
- Provides LOS detection for both T3 (ANSI T1.231) and E3 (G.775)
- Identical performance to Infineon's PEF 3452 TE3-LIU.

DS3/E3 Framer

- DS3 M23 framer in accordance with ANSI T1.107 and T1.404.
- E3 framer in accordance with G.832 and G.751.
- DS3 support for C-Bit Parity operation and clear channel mode.
- Detection of OOF, LOF, AIS, RDI/FERF alarms. Counting of OOF events, parity errors and far end errors as required in ATMF and IETF MIB.
- Automatic insertion of RDI/FERF on correct received alarm status. Generation and insertion of FEBE on received parity errors.
- DS3 C-Bit Parity detection by AIC monitoring; counting and processing of the FEAC and maintenance data link channel.
- E3 G.832 TR byte (16 byte Trail Trace) processing and generation. MA byte multi-frame synchronization, synchronization status nibble extraction and insertion.
- Gathers statistics in accordance with RFC 2496 'Managed Objects for DS3/E3 Interface Type'.
- Bypass modes supported to bypass both Framer and Cell/Packet processor.

ATM/PPP Protocol Processor

- Transmit Cell Processing:
  - Supports ATM cell payload scrambling, header check sequence generation, idle cell generation as per ITU-T I.432.
  - Mapping of ATM cells into E3 and DS3 frame as per G.804.
  - Generation of DS3/E3 G.751 PLCP frame and mapping of ATM cell stream into PLCP frame as per ATMF UNI 3.1.
  - ✧Extraction of ATM cells on pre-set VPI/VCI[1)].
  - ✧Optional on-the-fly checking of CRC-10 or AAL5 CRC-32 and length fields for extracted cells[1)].

- Receive Cell Processing:
  - Optional termination of PLCP frame for DS3/E3 G.751, extraction of ATM cell stream from PLCP frame or directly from DS3 or E3 frame.
  - Supports cell payload de-scrambling, header check sequence verification, idle cell filtering and performance monitoring.
  - ✧Insertion of ATM cells in the direction of the UTOPIA port[1)].
  - ✧Optional generation of CRC-10 or AAL5 CRC-32 field for inserted cells[1)].

- Transmit Packet Processing:
  - Supports HDLC Flag, CRC-16/32 and idle sequence generation. Abort generation for under-run conditions.
  - Mapping of HDLC data stream directly into DS3 or E3 frame.
  - ✧Extraction of in-band messaging packets on packet header[1)].
  - ✧On-the-fly checking of CRC and length fields for extracted packets[1)].
  - ✧Insertion of PPP packets into data stream[1)].

- Receive Packet Processing:
  - Extraction of HDLC data stream from DS3 or E3 frame.
  - Detection and removal of HDLC flags, checks for Abort sequence and optional checking of length and CRC-16/32 field.
  - Optional PPP Address-and-Control-Field filtering supported.
  - ✧Insertion of in-band messaging packets in the direction of the POS-PHY/ UTOPIA-L2X port[1)].

1) This is an option which is not available with the current firmware release.

System Interface

- UTOPIA Interface
  - 8/16-bit interface running up to 50 MHz.
  - Compliant to ATMF Utopia Level 2.
  - 16 Cell FIFO in both transmit and receive directions, programmable FIFO depth.
- POS-PHY Interface
  - Dual mode 8/16-bit interface running up to 50 MHz.
  - Compliant to POS-PHY Level 2.
  - Programmable burst size up to 64 bytes.
  - 896 byte FIFO in both transmit and receive directions, programmable FIFO depth.
- UTOPIA-L2X Interface
  - 8/16-bit interface running up to 50 MHz.
  - Based on UTOPIA Level 2 interface, extended for packet transfer capability.
  - Programmable chunk size of 16 ... 64 bytes.
  - 896 byte FIFO in both transmit and receive directions, programmable FIFO depth.
- Serial Bitstream Interface
  - Serial clock master and data interface for access to the DS3/E3 framer.
  - Serial clock slave and data interface for access to the cell/packet processor.

Microprocessor Interface

- 8/16-bit microprocessor slave interface - allows communication with the Device Control Interface (DCI). The DCI is an on-chip dual-ported Memory and Register Area. All communication with the TE3-FALC is achieved by writing high level commands, and reading high level status information, to and from the DCI.
- Multi-master access to external FLASH/EPROM when device is configured to boot independently.
- Eight configurable I/O ports that can be used to control LED's, provide boot up information or control external circuitry.

General

- JTAG enables Boundary Scan Test Support (IEEE 1149.1) for low-cost product development.

Applications

- 3rd Generation Mobile Basestations etc.
- DSLAMs
- Multiservice Access Switches
- Edge Routers

1.2 Logic Symbol

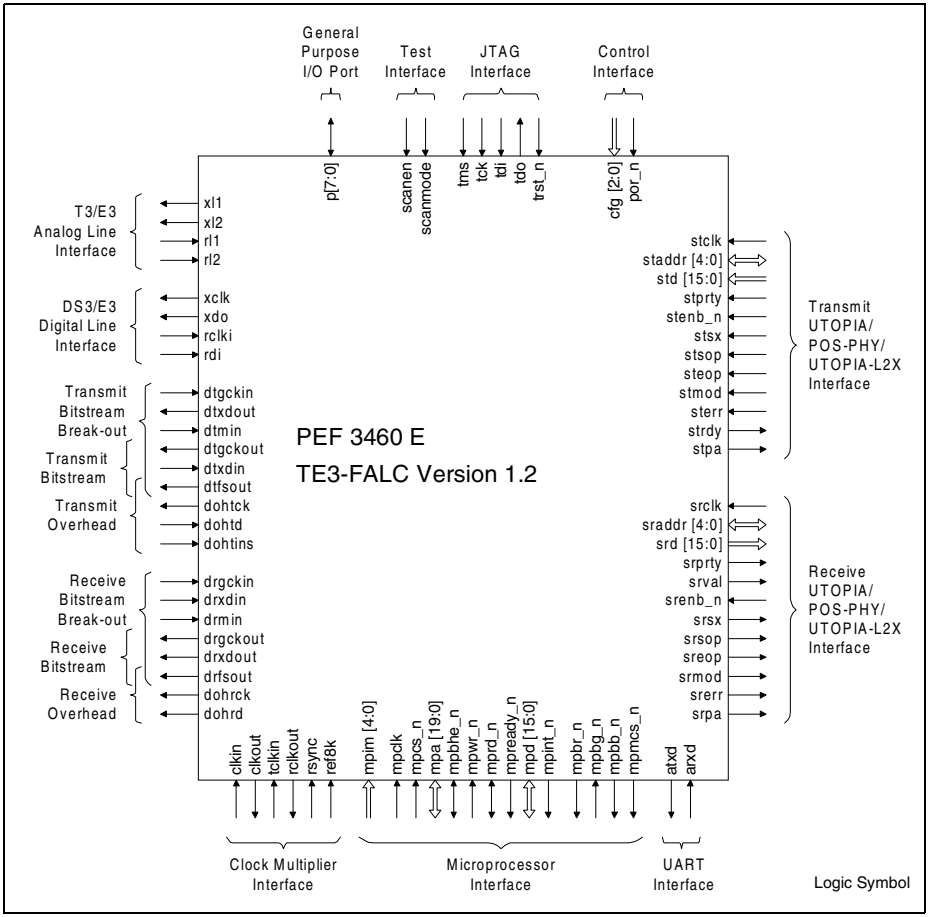
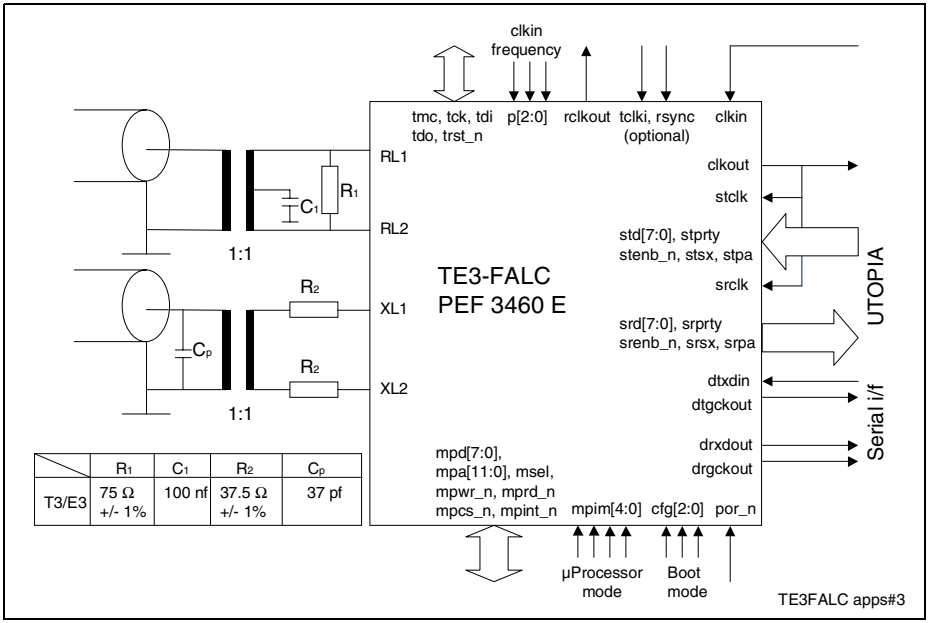


Figure 1 Logic Symbol

1.3 Minimum System



	R1	C1	R2	Cp
T3/E3	75 Ω +/- 1%	100 nf	37.5 Ω +/- 1%	37 pf

Figure 2 TE3-FALC Minimum System (UTOPIA or Serial Interface)

The above diagram shows the minimum system connectivity for the TE3-FALC showing all required signals to operate the device either with an UTOPIA interface or a serial interface. The TE3-FALC can operate from a single reference clock, CLKIN, and support software switching between T3 and E3 without any hardware change. When using a POS-PHY or UTOPIA-L2X interface the TE3-FALC is also able to switch between mapping ATM cells to PPP packets without any hardware change. Unused pins should be either left unconnected or tied to their inactive state as recommended in the pin description tables.

There are three hardware configuration selection pin groups. The first is P[2:0] which select the frequency range of CLKIN. The second is MPIM[4:0] which selects the type of microprocessor mode being used and the third, CFG[2:0], selecting the start up boot mode.

1.4 Typical Applications

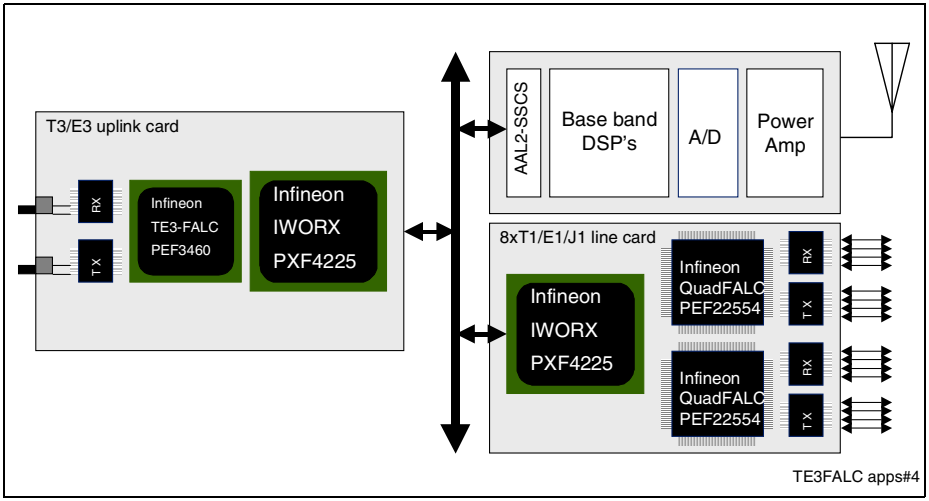


Figure 3 3G Mobile Base Station (AAL1/AAL2/AAL5)

The above diagram shows an application where the TE3-FALC provides the T3/E3 high speed WAN connection of a 3G Base stations, via point-point micro-wave equipment or SDH/SONET Optical transmission. Along with the very high integration (LIU, DJAT, Framer) the ability of the TE3-FALC to support both ATM and PPP/IP enables a single network interface to be designed that support today's ATM based networks and future proposed IP based networks.

The TE3-FALC compliments Infineon's IWORX device and QuadFALC. The IWORX provides a complete solution for AAL2 CPS, Traffic Management (CBR, VBR-rt etc.), I.610 OAM, Address Translation and IMA which is required for E1/T1 ATM based 3G Network interfaces. The IWORX also supports AAL1 allowing 2G equipment with TDM interfaces (Abis) to be connected to a 3G core network. The IWORX can also connect to other PHY devices like TE3-FALC via a second UTOPIA port. The QuadFALC framer and line interface component fulfills all required interfacing for four analog E1/T1/J1 lines. The powerful clocking options of QuadFALC have been included in TE3-FALC as well.

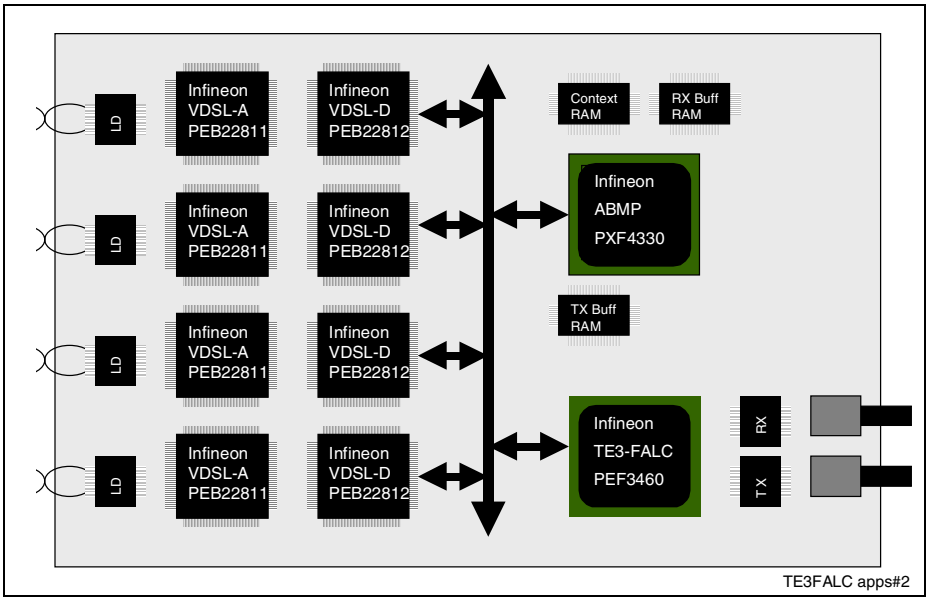


Figure 4 Customer Based MDU with T3/E3 Uplink

The above diagram shows an example of a four port Multi Dwelling Unit (MDU). The TE3-FALC provides the high speed connection to the core via SDH/SONET transmission equipment, the ABMP provides both traffic management and switching functionality.

The TE3-FALC supports not only ATM but also Frame Relay and PPP/IP which are popular alternatives for high speed links especially for equipment delivering Frame Relay over DSL or 10BaseS Ethernet. Integrated digital jitter attenuators enable the equipment to be in loop-timed mode and the integrated LIU supports plug and play installation for T3 (no requirement to measure cable length and set Line Build Out on the transmit pulse)

The ABMP provides full traffic management and switching for up to 31 UTOPIA L2 ports, it provides CBR, VBR-rt, VBR-nrt, ABR and UBR classes and supports IP Diffserv over ATM. Support of MPLS Label Switch Router (LSR) functionality is enabled with the support of VC-merging. Additional Infineon devices can be used along side the ABMP to add I.610 OAM (PXB 4340 AOP) and I.371 Policing and Address Translation (PXB 4350 ALP)

The VDSL transceivers solution from Infineon (PEB 22811 & PEB 22812) connect to the ABMP via a UTOPIA L2 interface. These interfaces can be exchanged for ADSL or G.SHDSL interfaces also available from Infineon.

2 Pin Descriptions

Table 1 gives an overview about the pin utilization per interface. Beyond the signal count of these interfaces there is a variety of test signals, which is made available either directly (using dedicated pins) or multiplexed with existing signal I/O pins. These test signals are not shown in Table 1. For complete pinning information, including multiplexed signals, driver strengths, pull-ups/pull-downs, refer to the data sheet, which cover all pins.

Table 1 External Interfaces

Interface	Function	Signal Count
T3/E3 Analog Line Interface	Transmit tip/ring, receive tip/ring	4
DS3/E3 Digital Line Interface	Transmit and receive clock/data	4
DS3/E3 Bitstream and Overhead Access Interface	Optional access to DS3/E3 overhead and/or payload data (9 transmit, 8 receive pins)	17
Clcok Multiplier Interface	Clock supplies and clock outputs	6
System Interface (UTOPIA / POS-PHY / UTOPIA-L2X)	Cell and packet based streaming interface. 16-bit data, 5-bit address per direction	62
Microprocessor Interface	Microprocessor interface in Intel/ Motorola format. 16-bit data, 20-bit address	52
JTAG Interface	Provides access to boundary scan	5
Control Interface	Reset, boot configuration	6
General Purpose I/O Port	General purpose I/O pins	8
UART Interface	Asynchronous TX and RX line	2
Test Interface	Test pins for manufacturer use only	2
Debug Interface (Reserved)		19

2.1 Pin Diagram

(top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VDD	clkout	VDDPLL	mpim1	mpim4	mpready_n	mpwr_n	mpmcs_n	mpa16	mpa15	mpa12	mpa8	mpa5	VDD	mpd15	mpd12	mpd11	mpd6	mpd5
B	RSVD	ref8k	rsync	clkin	mpint_n	mpim0	mpbhe_n	VDD	mpbr_n	mpa17	mpa13	mpa11	mpa7	mpa4	mpa2	mpd14	mpd8	mpd7	mpd4	mpd2
C	N.C.	RSVD	N.C.	rclkout	core_ratio	mpim3	mpcs_n	mprd_n	mpbg_n	mpa18	mpa14	mpa10	mpa6	mpa3	mpa0	mpd13	mpd9	mpd3	mpd1	sterr
D	N.C.	RSVD	RSVD	VSS	tclkin	VDDP	mpim2	VSS	mpbb_n	mpa19	VDDP	mpa9	VSS	mpa1	VDDP	mpd10	VSS	mpd0	VDD	steop
E	N.C.	N.C.	N.C.	RSVD	*Clock Multiplier Interface*				*Microprocessor Interface*								mpclk	stmod	strdy	stenb_n
F	RSVD	RSVD	RSVD	VDDP													VDDP	stsop	RSVD	stpa
G	VDD	rdi	rclki	RSVD													stsx	RSVD	staddr0	staddr1
H	VDDA	xclk	xdo	VSS	*T3/E3 Line Interface*												VSS	staddr2	staddr3	VDD
J	xl1	VDDA	RSVD	RSVD					VSS	VSS	VSS	VSS		*Streaming Interface*			staddr4	RSVD	stprty	std0
K	rl1	xl2	N.C.	VDDP					VSS	VSS	VSS	VSS					std1	std2	std3	std4
L	rl2	VDDA	VDDA	VDD					VSS	VSS	VSS	VSS		*(UTOPIA / POS-PHY / UTOPIA-L2X)*			VDDP	std6	std7	std5
M	VDD	N.C.	dtgckin	dtxdout	*Bitstream and Overhead Access*				VSS	VSS	VSS	VSS					std11	std10	std9	std8
N	VDD	dtxdin	dtfsout	VSS													VSS	std13	VDD	std12
P	dtmin	dtgckout	dohtd	drxdout													srd14	stclk	std15	std14
R	dohtck	dohtins	drxdin	VDDP			*Config & Misc*										VDDP	srd13	srd15	srclk
T	drgckin	drfsout	drgckout	scanmode	*Test Pins*				*Debug Pins (reserved)*								srd7	srd10	srd11	srd12
U	drmin	dohrck	scanen	VSS	arxd	VDDP	p6	VSS	RSVD	VDDP	RSVD	RSVD	VSS	srenb_n	VDDP	sraddr4	VSS	srd6	VDD	srd9
V	dohrd	tdo	tck	atxd	p2	p5	cfg1	RSVD	RSVD	RSVD	RSVD	RSVD	srerr	srsop	RSVD	sraddr1	RSVD	srd1	srd5	srd8
W	tdi	tms	VDD	RSVD	p3	p7	cfg2	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	sreop	srsx	srpa	sraddr2	srprty	srd2	srd4
Y	trst_n	por_n	p0	p1	p4	cfg0	RSVD	RSVD	VDD	RSVD	RSVD	RSVD	RSVD	srmod	srval	VDD	sraddr0	sraddr3	srd0	srd3

(table)

Figure 5 Pin Configuration P-BGA-272-4 Package

3 Functional Description

3.1 Block Diagram

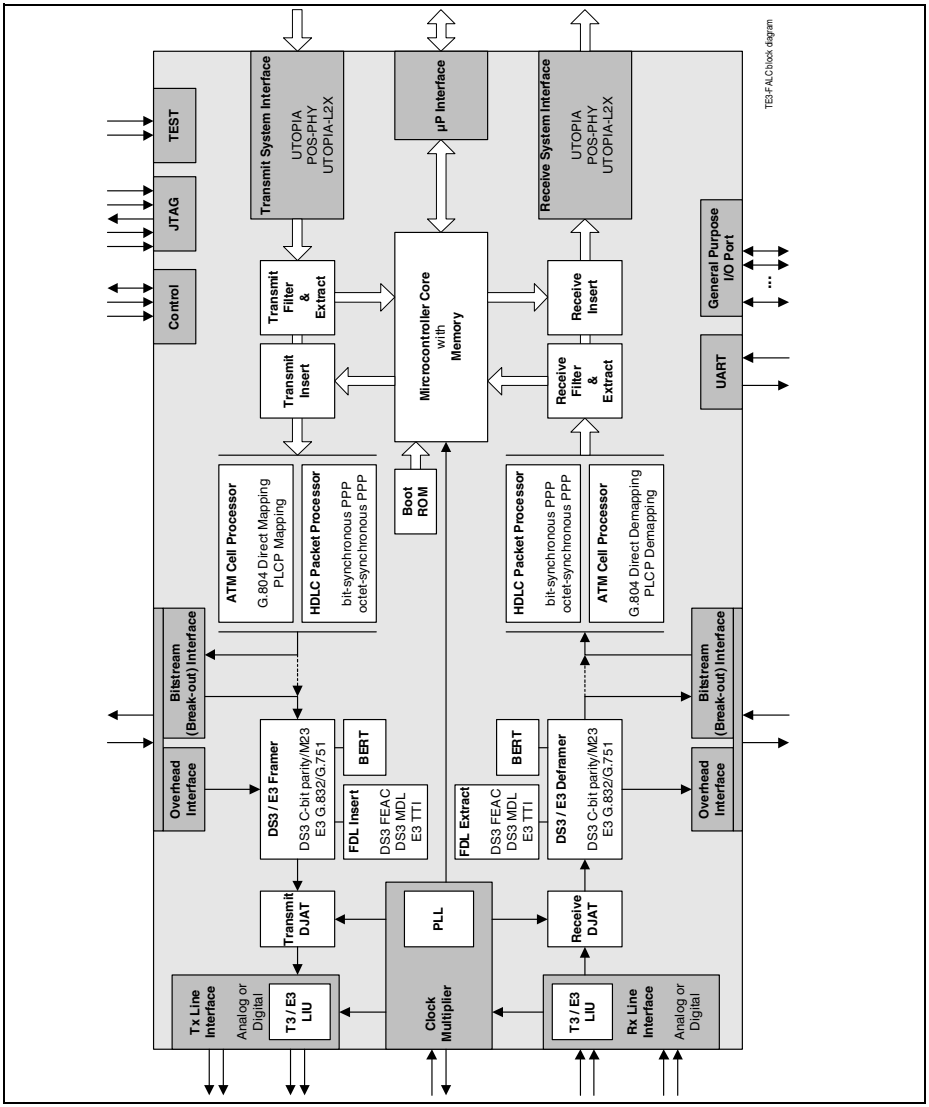


Figure 6 TE3-FALC Block Diagram

3.2 Functional Blocks

The functional blocks described in this section are shown as white boxes in the block diagram, **Figure 6**.

For a description of the external hardware interfaces shown as greyed boxes in the above block diagram refer to **“Hardware Interface Description” on Page 26**.

3.2.1 Analog T3/E3 Line Interface Unit (LIU)

This contains analog and digital functional blocks, which are configured and controlled via software.

The main interfaces are

- Receive Line Interface
- Transmit Line Interface

The main internal functional blocks are

- Analog line receiver with noise & crosstalk filter, equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper
- Central clock generation module
- Maintenance functions (e.g. loop switching local or remote)

3.2.2 Jitter Attenuator (DJAT)

3.2.2.1 Receive DJAT

The receive jitter attenuator is placed in the receive path. The working clock is an internally generated high frequency clock based on the clock provided on pin CLKIN. The jitter attenuator meets the E3 requirements of G.823 and ETSI TBR24 and DS3 requirements of GR-499-CORE. The internal PLL circuitry generates a "jitter-free" output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock. The receive jitter attenuator can be synchronized either on the extracted receive clock RCLK or on a programmable receive reference clock, between 52 MHz and 8 kHz clock, provided on pin RSYNC. The jitter attenuated clock can be output on pin RCLKOUT and optionally divided down to an 8 kHz clock. The receive jitter attenuator circuitry attenuates the incoming jittered clock starting at 20 Hz jitter frequency with 20 dB per decade fall-off. Wander with a jitter frequency below 20 Hz is passed un-attenuated. A holdover mode or a center mode is possible in case of lost reference clock. The Rx DJAT center mode clock frequency is derived from CLKIN. The intrinsic jitter in the absence of any input jitter is < 0.06 UI.

3.2.2.2 Transmit DJAT

The transmit jitter attenuator circuitry generates a "jitter-free" transmit clock and meets the following requirements for E3: ETSI TBR24 and DS3: GR-499-CORE. The Tx DJAT circuitry works internally with the same high frequency clock as the receive jitter attenuator. It synchronizes either to the transmit reference clock provided on pin TCLKIN, or the clock recovery PLL output, or to the Rx DJAT output clock (remote loop/ loop-timed). A holdover mode or a center mode is possible in case of lost reference clock. The Tx DJAT center mode clock frequency is derived from CLKIN.

The Tx DJAT attenuates the incoming clock jitter starting at 20 Hz with 20 dB per decade fall-off. Wander with a jitter frequency below 20 Hz is passed transparently.

The jitter attenuated clock is output on pin XCLK. The transmit jitter attenuator can be disabled. In that case data is read from the transmit elastic buffer with the clock sourced on pin TCLKIN (34 MHz for E3 or 45 MHz for DS3).

Intrinsic Jitter

The TE3-FALC transmit PLL generates an output jitter which fulfills the requirements as specified below:

- GR-499-CORE
- ANSI T1.404 (DS3)
- ETSI TBR24 (E3)

3.2.2.3 Center/Holdover Mode

Both Rx and Tx DJAT PLL are programmable to operate with a P characteristic or with PI characteristic.

Center Mode

When the PLL operates with P characteristic (only proportional element) and its reference clock is lost, the PLL will output the center frequency derived from main clock CLKIN.

Holdover Mode

When the PLL operates with PI characteristic (proportional and integral element) and its reference clock is lost, the PLL will hold the latest frequency. Due to the integral portion of the PLL circuit the holdover frequency gets constantly adapted. Thus there will be no slip in frequency in this case.

3.2.2.4 Rx and Tx Jitter Attenuator Buffer

The TE3-FALC has two jitter attenuator buffers, one for transmit direction and one for receive. The buffer size is 64 bit. The buffers can be used if the line clock and the framer

clock are different, e.g. in case the Rx DJAT output clock is used as receive framer clock. As the TE3-FALC is a terminating device, it is normally not necessary to use the dejittered clock for the receive framer and the Rx buffer can be bypassed.

The buffers are useful for remote loops with jitter attenuation and if the bitstream access ports should have a dejittered clock.

3.2.3 Line Coding

In E3 applications the HDB3 coding is provided for the data received from the ternary interface. In DS3 mode the B3ZS code is supported. All code violations are detected and indicated.

3.2.4 DS3 Framer

The DS3 framer can be operated in two application modes:

- C-bit parity format
- M23 multiplex format

Optionally the TE3-FALC can automatically detect the application mode by observing the Application Identification Channel (AIC bit in C-bit parity = C_{11} bit in M23 multiplex mode). In both modes, full payload rate format is supported, i.e. the data blocks [84] carry one continuous data stream.

3.2.4.1 Alarm Indication Signal (AIS), Idle Signal

Alarm Indication Signal or Idle signal is declared, when the selected signal format was received with less than 8/15 bit errors for at least one multiframe.

The alarm indication signal can be selected as:

- Unframed all '1's
- Framed '1010' sequence, starting with a binary '1' after each OH-bit. C-bits are set to '0'. X-bits are checked as '1' (✧X-bit check can be disabled[1)]).

The idle signal is a

- Framed '1100' sequence, starting with a binary '11' after each OH-bit. C-bits are set to '0' in M-subframe 3. X-bits are checked as '1' (✧X-bit check can be disabled[1)]).

3.2.4.2 Loss of Signal

Loss of signal defect is declared, when the incoming data stream contains more than 1022 consecutive '0's. Loss of signal defect is removed, when two or more ones are detected in the incoming data stream.

1) This is an option which is not available with the current firmware release.

3.2.4.3 Performance Measurement

The following conditions are counted:

- Line code violations
- Excessive zeros
- P-bit errors, CP-bit errors
- Framing bit errorsFar end block errors
- OOF defects
- LOS defects
- Remote Defect Indications (RDI)
- Errored Seconds (far-end and near-end)

3.2.5 E3 Framer

The E3 framer can be operated in two application modes:

– E3 framer according to ITU-T G.832
– E3 framer according to ITU-T G.751

3.2.5.1 Performance Measurement

The following conditions are counted:

- Line code violationsBIP-8 errors (E3 G.832 only)
- Excessive zeros
- Framing errors
- Remote error indications (REI)(E3.G832 only)
- Remote Alarm indications (RAI)(E3 G.751 only)
- OOF defects
- LOS defects
- Remote Defect Indications (RDI)(E3 G.832 only)
- Errored Seconds (far-end and near-end)

3.2.6 DS3/E3 Bit Error Rate Test (BERT) Unit

The bit error rate test unit of the TE3-FALC incorporates a test pattern generator and a test pattern synchronizer which can be assigned to the DS3 or the E3 framer. Controlled by a set of messages it can generate and synchronize to polynomial pseudorandom test patterns or repetitive fixed length test patterns.

In pseudorandom test mode the receiver tries to achieve synchronization to a test pattern which satisfies the programmed receiver polynomial. In fixed pattern mode it synchronizes to a repetitive pattern with a programmable length. An all '1' pattern or an all '0' pattern, which satisfies this condition, is flagged. Measurement intervals as well as receiver synchronization can be controlled by the user. When a test is finished an interrupt is generated and the bit count and the bit error count are readable.

Bit Error Insertion

The test unit provides the optional capability to insert bit errors in the range of 10^{-7} (1 error in 10.000.000 bits) up to 10^{-1} bit errors (1 error in 10 bits).

3.2.7 ATM Cell Processor and PLCP

The cell processor performs the mapping and de-mapping of ATM cells from the G.832/ G.751 E3 Frame, DS3 Frame and PLCP Frame (DS3 or E3 G.751). The mapping and de-mapping follows the requirements described in ITU-T G.804.

The self-synchronizing payload scrambler with the generator polynom $X^{43} + 1$ can optionally be enabled.

Transmit

In the transmit direction ATM cells from the internal FIFO are taken, a valid HEC is calculated and written into the cell header.

In order to maintain a constant flow of back-to-back cells, IDLE cells are automatically inserted when no cells are available from the internal FIFO.

ATM cells are mapped byte-synchronously into the E3 G.832/G.751 frame and the PLCP sub-frame. Nibble-aligned mapping is used for the DS3 frame option.

Receive

In receive direction the ATM cells are either extracted directly from the E3 or DS3 frame or from the PLCP frame. When extracting cells directly from the E3/DS3 frame, cell boundaries are found by using the HCS.

Single bit errors in the ATM header can be corrected using the Header Error Correction mechanism. IDLE cells are detected and discarded within the cell processor.

3.2.7.1 PLCP Mapping

The TE3-FALC supports mapping of ATM cells via PLCP layer into a DS3/ E3 G.751 envelope according to standards ATM Forum af-phy-0054.000 and ANSI T1.646-1995.The PLCP frame rate is 125 µs.

3.2.7.2 Performance Measurement

The TE3-FALC offers a set of counters

- Transmitted and received user cells
- Transmitted and received idle cells
- HEC errors
- HEC corrections
- OCD events

- PLCP BIP-8 errors
- PLCP framing errors
- PLCP far end block errors
- PLCP OOF defects
- PLCP Remote Alarm Indications (RAI)

3.2.8 HDLC Packet Processor

The HDLC packet processor implements HDLC framing and supports the Point-to-Point Protocol (PPP) with its bit-synchronous and octet-synchronous mapping options.The frame[1)] begin and frame end synchronization is performed with the flag character $7E_H$ ($0111\ 1110_2$). Shared opening and closing flag is supported in receive direction and can be programmed for transmit direction. Shared '0' bit between closing and opening flags is understood by the receiver in bit-synchronous HDLC operation.

The following CRC modes are supported:

- 16 bit CRC1+x^5+x^{12}+x^{16}
- 32 bit CRC1+x+x^2+x^4+x^5+x^7+x^8+x^{10}+x^{11}+x^{12}+x^{16}+x^{22}+x^{23}+x^{26}+x^{32}

Optionally CRC transfer and check can be disabled. The interframe-time fill pattern can be programmed to either flags ($7E_H$) or all ones indicating idle.

3.2.8.1 PPP Header Operations

TE3-FALC supports PPP in HDLC-like framing according to IETF RFC1661 and RFC1662.

In contrast to plain HDLC operation, the Address and Control fields contain the fixed hexadecimal values FF_H and 03_H respectively. An implemented filter passes only receive packets starting with the PPP header FF-03_H, unless the Address-and-Control-Field compression option from below is enabled.

Address-and-Control-Field Compression (ACFC) Option

If Address-and-Control-Field compression (RFC1661, chapter 6.6) is enabled, PPP packets on the line are transferred without the PPP Address and Control fields FF-03_H. If disabled, the transmitter prepends the fields FF-03_H for each PPP packet coming from the system side.

Compression in transmit direction is not performed for LCP packets, which are recognized by their protocol ID (PID) value C0-21_H.

On reception, the Address and Control fields are decompressed by examining the first two octets. If they contain the values FF_H and 03_H, they are assumed to be the Address

1) Both terms "frame" and "packet" are used further on. When describing HDLC framing functions, "frame" is the preferred term; a PPP datagram is referred as "packet".

and Control fields. If not, it is assumed that the fields were compressed and were not transmitted. Towards the system side, the bytes FF-03 are omitted if they were present on the line.

Protocol Field Compression (PFC) Option

If the Protocol-Field compression option (RFC 1661, chapter 6.5) is enabled, certain Protocol fields can be compressed to one octet instead of two.

In transmit direction, this compression is performed if the protocol field value is 00-FF_H or less, i.e. the most significant PID octet is zero.

In receive direction, protocol field compression is detected by evaluating the least significant bit of the first incoming PID octet: A '0' marks the most significant octet, a '1' marks the least significant octet of the protocol field. If the least significant bit of the first PID octet is '1', the received protocol field has been compressed to one octet and will now be decompressed by inserting 00_H as the most significant octet before forwarding it to the system side.

3.2.8.2 Performance Measurement

The TE3-FALC offers a set of counters:

- Transmitted and received bytes
- Transmitted and received valid and errored packets
- Underflown and overflown packets
- Too long, too short packets
- CRC errored packets
- Misaligned packets
- Bad PPP address fields and bad PPP control fields

3.2.9 Test Loops

The TE3-FALC supports a number of test loops:

- Local Line Loop
- Remote Line Loop
- Local Framer Loop
- ✧Remote Framer Loop[1)]
- Local system Interface Loop

Each of the loops can individually be enabled or disabled.

1) This is an option which is not available with the current firmware release.

3.2.10 Microcontroller Core with Memory

The TE3-FALC contains a microcontroller core which configures and controls the device. All necessary code and data RAM is on-chip. As part of the device initialization a firmware image of maximum 128 kB size must be uploaded. This firmware is essential for running the device and it is provided as a binary file. The firmware upload can be performed in two ways. The firmware image data is read autonomously by TE3-FALC (acting as bus master) out of an attached EPROM or image data can be written to the device by issuing a set of boot messages via the Device Control Interface DCI.

3.2.11 Software Handling

The firmware handles device configuration, alarm/ statistics management and the message based interface used to control the TE3-FALC. The message based interface can operate via the 8/16-bit microprocessor interface or via ✧inband messages encapsulated in ATM or PPP packets.[1)] The firmware reduces the time and effort spent of developing device specific software and also reduces time in conformance testing.

The provided interface of the TE3-FALC is called Device Control Interface (DCI) and is built to make the configuration and controlling of the device easier and more comfortable. The DCI is a dual-ported Memory- and Register-Area which is accessible for the user. This interface decouples the internal functional blocks from the external microprocessor bus. The DCI manages four message queues which are accessible from the internal and from the external bus for read and write, with the external access having the higher priority.

Communication with the TE3-FALC is done via messages. There is no need to read/ write configuration bits in registers directly. There are specific message types for different needs. The structure of the messages is common to all types, only the message identifier (MSGID) differs.

There are five general message types:

- Command (CMD)
- Progress Indication (PRG)
- Acknowledgement (ACK)
- Notification (NFC)
- Alarm (ALM)

A message consists of a 32-bit message actuator (MAT) and an optional parameter array.

The configuration process should be hierarchical. A Data Flow Configuration Function selects a specific data flow between the system side and the line side of the TE3-FALC device. According to the selected data flow all involved modules are configured by module specific configuration functions. A number of default settings are applied which can individually be changed by Module Configuration Messages. After configuration is completed, the interfaces can be enabled with a dedicated command.

This user friendly high level message based interface reduces development time and makes configuration of TE3-FALC easier.

4 Hardware Interface Description

4.1 T3/E3 Analog Line Interface

4.1.1 Receiver Application

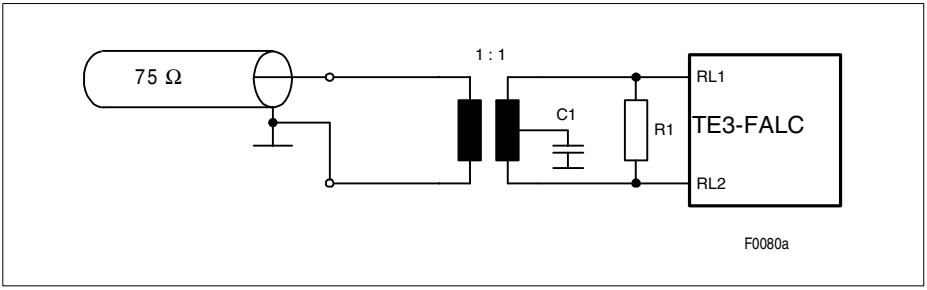


Figure 7 Standard Receiver Configuration

Table 2 External Component Values for Receiver

Parameter	Characteristic Line Impedance [Ω]	
	DS3	E3
	75	
R_1 (± 1 %) [Ω]	75	
C_1 (± 20 %) [nF]	100	
$t_2 : t_1$	1 : 1	

The external components are the same for DS3 and E3 applications. The TE3-FALC supports additional line monitoring mode.

4.1.2 Receive Line Interface

The receive line interface consists of a pre-amplifier, a noise and crosstalk filter, a variable gain amplifier (VGA) and an equalizer followed by the clock and data recovery.

The noise and crosstalk filter reduces distortions within the incoming analog signal. The VGA amplifies the analog signal and the equalizer compensates the frequency dependent line attenuation. Digital signal levels are formed within the retiming block of the clock and data recovery.

Receive return loss requirements of ITU-T G.703 are fulfilled as required for E3 operation.

The equalizer contains an additional 20 dB gain stage, which is used in line monitoring mode to amplify resistively attenuated signals.

4.1.3 Receive Clock and Data Recovery

The receive clock and data recovery extracts the route clock from the digital data stream and converts the data stream into a dual rail bit stream. The clock and data recovery needs a reference clock to keep the PLL stable during times without data signal at RL1/RL2. The receive clock is recovered of the signal provided on RL1/RL2 and has a duty cycle close to 50 %. The PLL reference clock is generated internally without the need for external components.

4.1.4 Receive Analog LOS

If the TE3-FALC is in E3 mode, the receive line interface includes the alarm detection for analog loss of signal (LOS). In T3/DS3 mode, the LOS definition is based on digital input levels. Digital LOS detection is a function of the DS3 framer.

Analog LOS is detected, if the signal level on pins RL1/2 drops below a fixed level ("B") for a certain period. Loss of signal level "B" is defined to be between 15 and 35 dB below normal signal level "A". If the signal exceeds 35 dB for 175 contiguous pulse periods (10 ≤ N ≤ 255), analog LOS defect is indicated.

Analog LOS defect is cleared, if the signal exceeds a threshold of 15 dB below nominal level for 175 contiguous pulse periods (10 ≤ N ≤ 255). See ITU-T G.775 for reference.

4.1.5 Receive Jitter Tolerance

The TE3-FALC receiver’s tolerance to input jitter complies to and exceeds the relevant international standards. Especially the requirements of Telcordia GR-499-CORE (DS3), ITU-T G.824 (DS3) and ITU-T G.823 (E3) are fulfilled and exceeded.

4.1.6 Transmitter Application

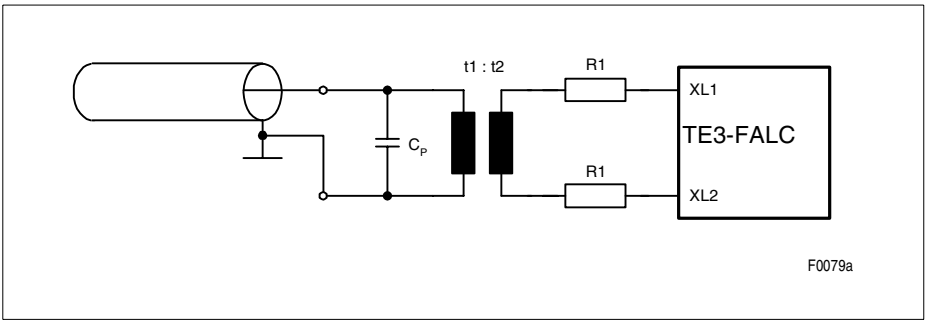


Figure 8 Transmitter Configuration

Table 3 External Component Values for Transmitter

Parameter	Characteristic Line Impedance [Ω]	
	DS3	E3
	75	
R_1 (± 1 %) [Ω]	37.5[1)]	
C_p [pF]	37[2)]	
$t_2 : t_1$	1 : 1	

1) This value refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value for the output serial resistors.

2) This value includes all parisitic capacitances on the secondary side of the transformer.

The external components are the same for DS3 and E3 applications. Transmit return loss requirements for E3 defined in ETS 300 166 are fulfilled. Pulse mask requirements according to ANSI T1.102 (at cross connect point, up to 450 ft.) are fulfilled.

Note: An additional capacitor on the primary or secondary side of the transformer may be required in some DS3 applications to improve the pulse mask, if the parasitic capacitances of the PCB are very small.

4.1.7 Transmit Pulse Shaper

The internal pulse shaper generates the required pulse shapes for E3 and DS3 signals according to ANSI T1.102, T1.404, Telcordia GR-499-CORE and ITU-T G.703).

The specific pulse mask is fulfilled at the crossconnect point at a distance of 0 to 450 ft. to the transmitter (DS3 requirement). There is no need to do additional configuration.

The maximum line length between a TE3-FALC transmitter and TE3-FALC receiver is 1100 ft. for a coaxial cable of AT&T type 728A, 734A or 734D.

4.2 DS3/E3 Digital Line Interface

The T3/E3 LIU can be bypassed and a digital clock and data interface can be provided via pins RDI, RCLKI, XCLK and XDO. This interface enables TE3-FALC to be connected to an external clock recovery circuit used for transmitting DS3/E3 over fiber or for connection to a DS3/E3 mapping device.

4.3 DS3/E3 Overhead, Bitstream and Payload Access Interface

The TE3-FALC provides serial access to the DS3/E3 frame overhead which enables proprietary framing formats or insertion/extraction of reserved overhead bits (named "Overhead Interface"). Once this interface is enabled, DS3/E3 frame overhead data can be extracted on the receive side at all times. Transmit overhead bits get overwritten whenever the DOHTINS signal is active (high) at the corresponding bit position. The first overhead bit is marked with the frame sync marker.

The TE3-FALC supports two serial payload interfaces, the first allows the TE3-FALC to act as a pure framer and provides clock, frame pulse and data signals for an external controller to map protocols, such as HDLC, into the frame (named "Bitstream Interface"). The second serial payload interface allows the data to and from the ATM cell processor or HDLC controller of the TE3-FALC to be accessed externally.

The latter two interfaces can be used together to provide a break in the TE3-FALC datapath (named "Bitstream Break-out") to allow for external proprietary sub-rate framing to performed, such as those used for Subrate T3.

Both overhead and bitstream interface share common frame sync markers.

4.4 Clock Multiplier Interface

The TE3-FALC integrates PLL's to enable the generation of T3/E3 line rate clocks for use in both transmit and receive directions. The TE3-FALC requires only a single clock, CLKIN, which can vary between 4 MHz to 52 MHz, the frequency range is selected by setting pins P0, P1 and P2 (1st stage PLL programming) with fine tuning via internal registers (2nd stage PLL programming).

All required clocks can be generated via CLKIN, this includes transmit line clock, receive reference clock, high speed clocks for the Tx and Rx DJAT's, internal logic and also a programmable output clock CLKOUT which can be used by the system (e.g. for UTOPIA clock).

TCLKIN is the optional transmit reference clock, this clock can be the reference for the Tx DJAT PLL or be used as the exact transmit clock (bypass the Tx DJAT PLL). The reference clock for the Tx DJAT PLL can vary between 8 kHz and 52 MHz.

RSYNC is the optional receive reference clock, the TE3-FALC can use this clock during LOS conditions for a reference to the Rx DJAT PLL. The reference clock for the Rx DJAT PLL can vary between 8 kHz and 52 MHz. The clock recovery PLL uses a reference clock derived from CLKIN in case of LOS conditions.

✧REF8K is an optional 8 kHz input used to synchronize the PLCP sub-frame inside a DS3/E3 G.751 frame; it does not need to be synchronous with TCLKIN[1)].

The TE3-FALC monitors clock activity on TCLKIN and RSYNC and can switch back to internally generated clocks, this provides the ability for the TE3-FALC to continue operating (e.g. to enable AIS transmission) when the central clock unit of a system fails or is removed.

Two clock outputs are provided: CLKOUT and RCLKOUT.

CLKOUT is a programmable general purpose clock (between 15 and 52 MHz), e.g. for UTOPIA clock.

RCLKOUT is the recovered line clock, this clock can be taken directly from the clock recovery unit and in this case is the line rate clock (34 or 45 MHz) with jitter. Optionally the RCLKOUT can pass through the Rx DJAT PLL and provide a smooth reference clock in the range 8 kHz to 52 MHz (e.g to give an 19.44 MHz, 2.048 MHz or 8 kHz reference). The Rx DJAT also provide optional holdover for RCLKOUT during LOS rather than switching back to the receive reference clock.

4.5 System Interface (UTOPIA / POS-PHY / UTOPIA-L2X)

The system side of the TE3-FALC implements a streaming interface which represents a superset of the industry standard interfaces:

- UTOPIA
- POS-PHY
- UTOPIA-L2X

The TE3-FALC acts as slave on these interfaces.

UTOPIA-L2X ("UTOPIA Level 2 with packet eXtension") interface supports the transfer of variable size packets in form of segments (chunks). POS-PHY interface also supports the transfer of variable size packets and mainly differs in the signalling.

Standard UTOPIA is considered a sub-mode of the packet oriented modes, with the assumption that an ATM cell is a fixed size packet with a length of 53 bytes (8-bit UTOPIA interface) or 27 words (16-bit UTOPIA interface).

The data bus can be configured to be 8-bit or 16-bit wide in all interface modes (although 8-bit bus width is not standardised in POS-PHY Level 2). The data format is big endian

1) Firmware option. TE3-FALC uses by default a fixed PLCP stuffing sequence which results in a nominal frame rate of 7.999848 kHz in DS3 master timed mode and 8.0 kHz in E3 G.751 master timed mode. In loop-timed mode, the recovered 8 kHz from the receiver is used as PLCP transmit reference.

and the parity calculated over the data bus lines is odd. The size of the chunks is programmable.

4.5.1 UTOPIA Interface Option

For a description of the UTOPIA Level 2 interface protocol refer to ATM-Forum specification af-phy-0039.000. Regarding the TE3-FALC interface signals consider the following:

- Packet signals SOP, EOP, ERR and MOD are not used. The corresponding transmit inputs must be pulled down to V_{SS} level, corresponding receive outputs can be left unconnected.
- SRSX/STSX are equivalent to the UTOPIA start of cell signals RxSoc/TxSoc.
- SRPA/STPA are equivalent to the UTOPIA cell-available signals RxClav/TxClav.

Optional UTOPIA Settings

- Bus Width
  - 8 bit
  - 16 bit
- Handshake
  - Cell-level handshake
  - Octet-level handshake
- Status Indication
  - MPHY polling mode
  - Direct status indication
- Bus Configuration
  - Multiple PHY devices (tri-state bus)
  - Single PHY, point-to-point connection (outputs do not tri-state)
- Parity Check
  - Parity check enabled.
    Parity-errored cells are discarded within transmit buffer.
  - Parity check disabled

4.5.2 POS-PHY Interface Option

The POS-PHY Level 2 interface has been defined by the SATURN group. For a description of the interface protocol refer to the POS-PHY Level 2 specification. The TE3-FALC signals SRSX/STSX are unused; the transmit input STSX must be pulled down to V_{SS} level, SRSX can be left unconnected.

Optional POS-PHY Settings

- Bus Width
  - 8 bit (although not standardized)

  - 16 bit
- Status Indication
  - Packet level mode
  - Byte level mode
- Bus Configuration
  - Multiple PHY devices (tri-state bus)
  - Single PHY, point-to-point connection (outputs do not tri-state)
- Parity Calculation
  - Odd or Even parity generation/check
    Short parity-errored packets are discarded within transmit buffer.
    Long parity-errored packets are aborted on the line.
  - Parity check disabled

4.5.3 UTOPIA-L2X Interface Option

UTOPIA-L2X ("UTOPIA Level 2 with packet eXtension") interface supports the transfer of variable size packets in form of segments (chunks).

Optional UTOPIA-L2X Settings

- Bus Width
  - 8 bit
  - 16 bit
- Chunk Size
  - Programmable to 16 .. 64 bytes (multiple of 4 bytes)
- Status Indication
  - MPHY polling mode
  - Direct status indication
- Bus Configuration
  - Multiple PHY devices (tri-state bus)
  - Single PHY, point-to-point connection (outputs do not tri-state)
- Parity Check
  - Parity check enabled.
    Short-parity errored packets are discarded within transmit buffer.
    Long-parity errored packets are aborted on the line.
  - Parity check disabled

4.6 Microprocessor Interface

The microprocessor interface (MPI) can be configured to asynchronous Intel or Motorola like handshake, the Motorola mode offers additionally a synchronous interface option with MPC860 compatible handshake. The addressing scheme (Big/Little Endian) can be programmed independent from the selected interface style (Motorola/Intel) via mode pin MPIM4.

4.6.1 Slave Accesses (Device Configuration/Control)

Communication with the TE3-FALC is done via MPI slave accesses according to the message based Device Control Interface (DCI). Internal data structures are 32-bit wide, and in general 32-bit words (DWORD) have to "tunnel" through the low pin-count MPI with 16- or 8-bit data bus width.

4.6.2 Master Accesses (8-Bit EPROM Load Function)

TE3-FALC performs master read accesses to an external EPROM/EEPROM/Flash during the boot process if an appropriate boot configuration is selected via pins CFG[2:0]. The addressable range is 128 kB using address lines A[16:0].

Prior to a read access the TE3-FALC arbitrates for bus mastership. Both Intel and Motorola arbitration mechanisms are implemented.

4.7 JTAG Interface

A Test Access Port (TAP) with boundary scan operation is implemented according to IEEE 1149.1.

4.8 Control Interface

Power-On Reset

Setting the external input pin $\overline{\text{POR}}$ to 0 resets the complete chip with new image download. This is an asynchronous reset.

Boot Mode Configuration

The 3 pins CFG[2:0] exist for configuration of the boot mode.

For boot operation via the message based Device Control Interface (DCI), pins (CFG2, CFG1, CFG0) should be set to (0, 0, 1).

To boot from an external EPROM, pins (CFG2, CFG1, CFG0) should be set to (0, 1, 1).

Any other settings are for debug purpose or future use.

4.9 General Purpose I/O Port

The general purpose I/O port comprises two functions:

PLL Frequency Programming

At the beginning of the boot process, right after reset, the input levels on pins P2, P1 and P0 are used to roughly program the on-chip PLL such that it generates a system clock of 25 to 50 MHz derived from the provided clock CLKIN.

Note: Wrong PLL frequency programming might lead to internal overclocking and can thus influence the reliablitiy of the device's operation!

General Purpose Input/Output Function

During operation, pins P0 to P7 are used as general purpose inputs and outputs. Optionally an internal pull-up or pull-down transistor can be enabled which eliminates the need for an external resistor.

4.10 UART Interface

✧The UART interface is available for potential debug purposes.[1)] It might be a good practice to provide soldering pads for the UART receive and transmit signals.

The output can be monitored via a terminal with following settings:

- 9600 bit/s
- 1 Start bit
- 8 Data bits
- No Parity
- 1 Stop bit

4.11 OCDS and TEST Interface

The OCDS (debug interface) and the TEST interface are for manufacturer use only. OCDS pins can be left unconnected while the TEST interface pins should be connected to V_{SS}.

1) This is an option which is not available with the current firmware release.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-40 to +85	°C
Storage temperature	T_{stg}	-65 to +125	°C
Core supply voltage	V_{DD}	-0.4 to 1.89	V
I/O supply voltage Analog PLL supply voltage Analog LIU supply voltage	V_{DDP} V_{DDPLL} V_{DDA}	-0.4 to 3.6	V
Voltage on any pin with respect to ground	V_S	-0.4 to 3.6	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	1500	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

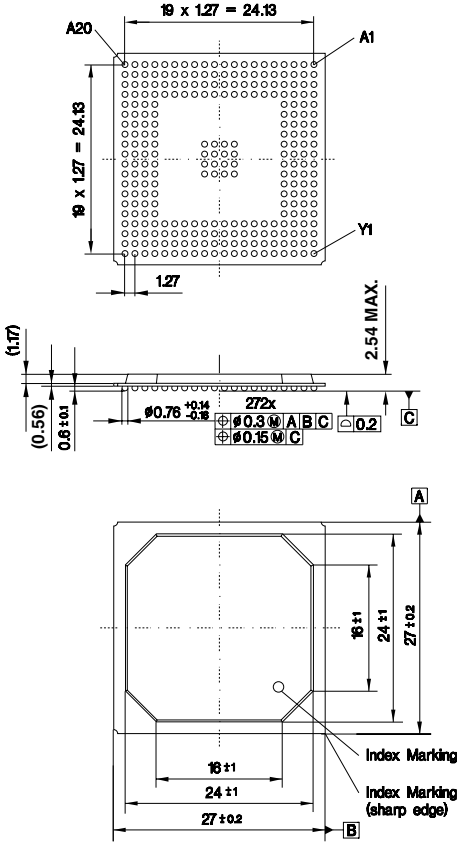
5.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Core supply voltage	V_{DD}	1.71	1.89	V	1.8 V ± 5%
I/O supply voltage Analog PLL supply voltage Analog LIU supply voltage	V_{DDP} V_{DDPLL} V_{DDA}	3.14	3.46	V	3.3 V ± 5%

Note: In the operating range, the functions given in the circuit description are fulfilled.

6 Package Outlines

P-BGA-272-4
(Plastic Ball Grid Array)



You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

7 Appendix

TE3-FALC comes along with a comprehensive support package available on the Infineon Technologies web site at http://www.infineon.com/t3.

7.1 Documentation

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the Internet page:

http://www.infineon.com/t3

On the same page you find as well the

- Boundary Scan file for TE3-FALC Version 1.2 (BSDL File)
- TE3-FALC Firmware Image
- IBIS Model for TE3-FALC Version 1.2

7.2 Tools and Software Support

The following software package is provided together with the TE3-FALC Evaluation Board EASY 3460:

- Schematics, Layout, Gerber Files, Bill of Material of the EASY 3460 Board
- "TE3-FALC Configuration Assistant"
- Reference Source Code Driver for TE3-FALC API Message Interface with documentation; easy re-use in customer system software

TE3-FALC Configuration Assistant

To make system design easier, the "TE3-FALC Configuration Assistant" is available. This tool runs under Win 9x/ME/NT/2000/XP environment.

The Configuration Assistant is a Windows Application which helps the user to get a quick overview over the chip and to configure it with only a few mouse clicks.

Starting from the archived application, data flow and operational modes of this application translates the setup into configuration messages which need to be given to the device.

- Configuration of the data flow and main operational modes
- Detailed block configurations (Optional)
- Check for potential misconfiguration
- Online configuration by message transfer to the device
- Online status evaluation, performance and alarm monitoring
- Offline Mode: Output of the minimum configuration message set to ASCII file or printer. This output can be used as base for development of custom software configuration set

Screenshots of the program are shown in **Figure 9** and **Figure 10** below:

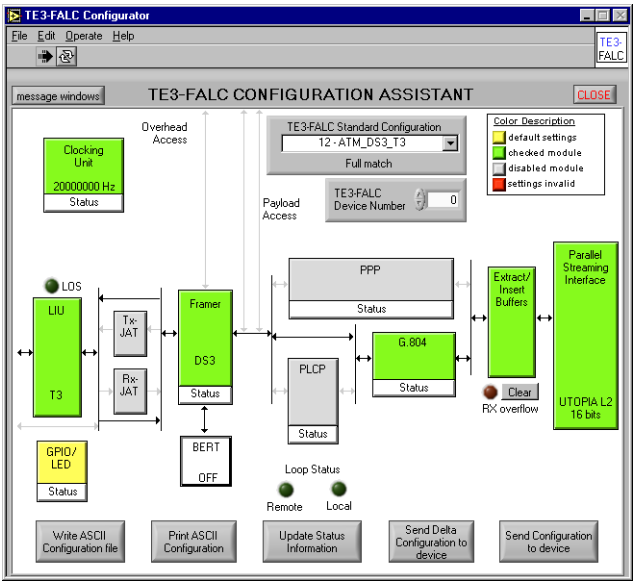


Figure 9 TE3-FALC Configuration Assistant Main Window

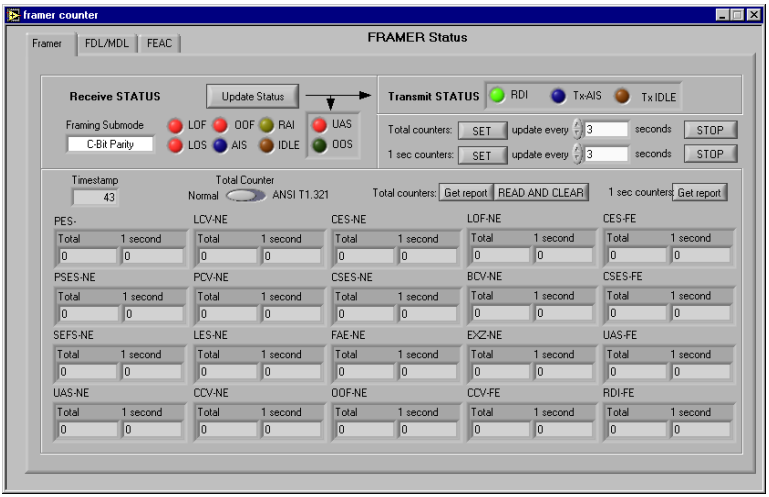


Figure 10 Configuration Assistant Framer Status and Performance Counters

http://www.infineon.com

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