

Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage, V _G	-15V to +0.3V
All Input Voltages	-15V to +0.3V
All Output Voltages	-15V to +0.3V
Output Current (total, all ports)	-4 mA

ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{GG} = -10V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V _{IH}	0		-2.0	V	Ports A to D, I _{7,0} BREAK, STEP, INT, RESET, and ACC/PC
Input Low Voltage	V _{IL}	-4.3		V _{GG}	V	Ports A to D, I _{7,0} BREAK, STEP, INT, RESET, and ACC/PC
Clock High Voltage	V _{CH}	0		-0.8	V	CL ₀ Input, External Clock
Clock Low Voltage	V _{CL}	-6.0		V _{GG}	V	CL ₀ Input, External Clock
Input Leakage Current High	I _{LIH}			+10	μA	Ports A and B, I _{7,0} INT, RESET, BREAK, STEP, ACC/PC, V _I = -1V
				+10	μA	Ports C and D, V _I = -1V
Input Leakage Current Low	I _{LIL}			-10	μA	Ports A and B, I _{7,0} INT, RESET, BREAK, STEP, ACC/PC, V _I = -11V
				-10	μA	Ports C and D, V _I = -11V
Clock Input Leakage High	I _{LCH}			+200	μA	CL ₀ Input, External Clock, V _{CH} = 0V
Clock Input Leakage Low	I _{LCL}			-200	μA	CL ₀ Input, External Clock, V _{CL} = -11V
Output High Voltage	VOH1			-1.0	V	Ports C to I, P _{10,0} I _{OH} = -1.0 mA
	VOH2			-2.3	V	Ports C to I, P _{10,0} I _{OH} = -3.3 mA
Output Leakage Current Low	I _{LOL}			-30	μA	Ports C to I, P _{10,0} V _O = -11V
Supply Current	I _{GG}		-30	-50	mA	

AC CHARACTERISTICS

T_a = -10°C to +70°C, V_{GG} = -10V ± 10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Frequency	f ₀	150		440	KHz	
Clock Rise and Fall Times	t _r , t _f	0		0.3	μs	
Clock Pulse Width High	t _{0WH}	0.5		5.6	μs	
Clock Pulse Width Low	t _{0WL}	0.5		5.6	μs	
Input Setup Time	t _{IS}			5	μs	
Input Hold Time	t _{IH}	0			μs	
BREAK to STEP Interval	t _{BS}	200			μs	f = 400 KHz, "1" Written
STEP to RUN Interval	t _{SB}	200			μs	f = 400 KHz, "1" Written
STEP Pulse Width	t _{WS}	30			μs	f = 400 KHz, "1" Written
BREAK to ACC Interval	t _{BA}	200			μs	f = 400 KHz, "1" Written
ACC/PC Pulse Width	t _{WA}	30			μs	f = 400 KHz, "1" Written
STEP to ACC Interval	t _{SA1}	200			μs	f = 400 KHz, "1" Written
PC to STEP Overlap	t _{SA2}			5	μs	f = 400 KHz, "1" Written
PC to RUN Interval	t _{AB}	0			μs	f = 400 KHz, "1" Written
ACC/PC - P _{10,0} Delay	t _{DAP1}			15	μs	f = 400 KHz, "1" Written
	t _{DAP2}			15	μs	f = 400 KHz, "1" Written

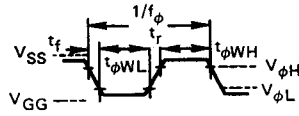
CAPACITANCE

T_a = 25°C

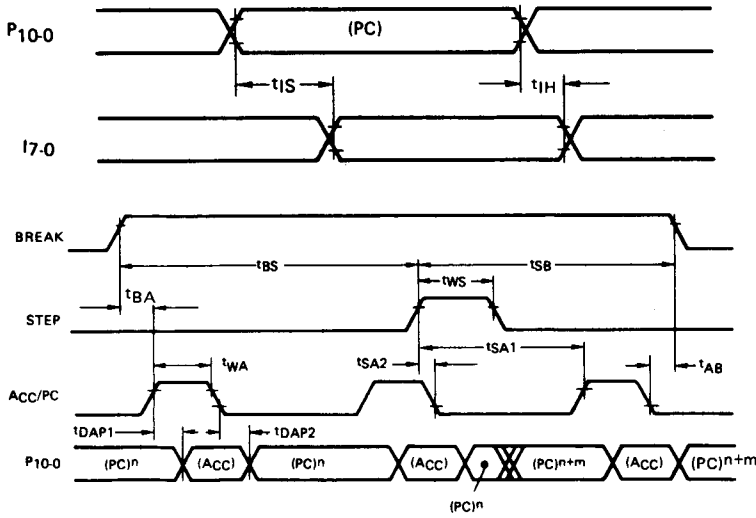
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C _I			15	pf	f = 1 MHz
Output Capacitance	C _O			15	pf	
Input/Output Capacitance	C _{IO}			15	pf	

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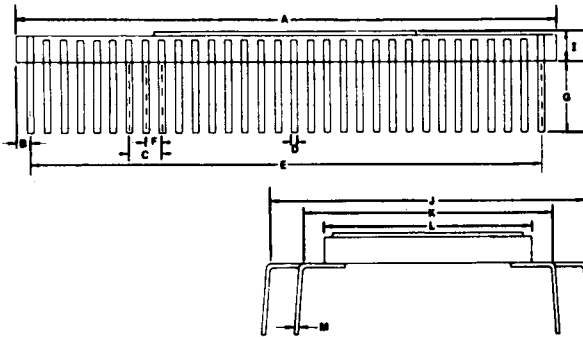
CLOCK WAVEFORM



TIMING WAVEFORMS



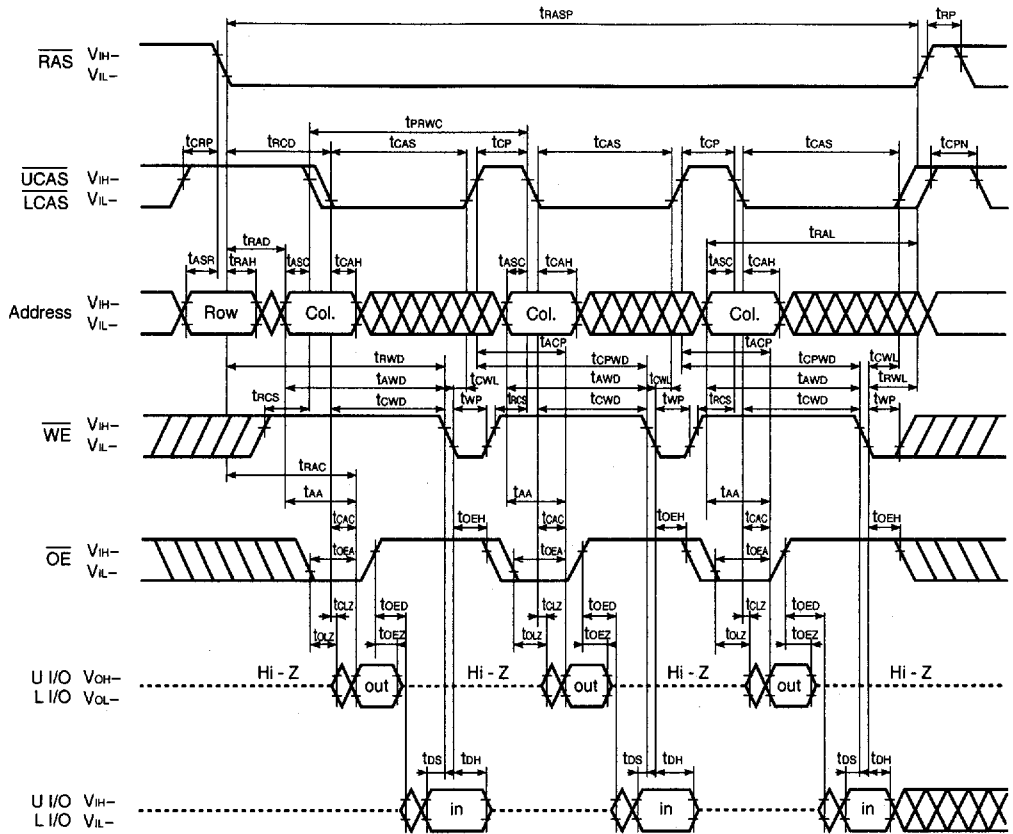
PACKAGE OUTLINE
μPD556B



CERAMIC

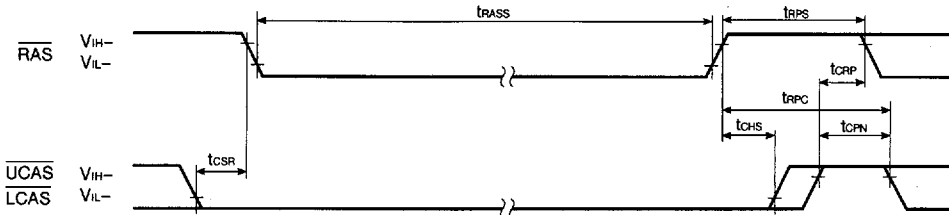
ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

CAS Before RAS Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

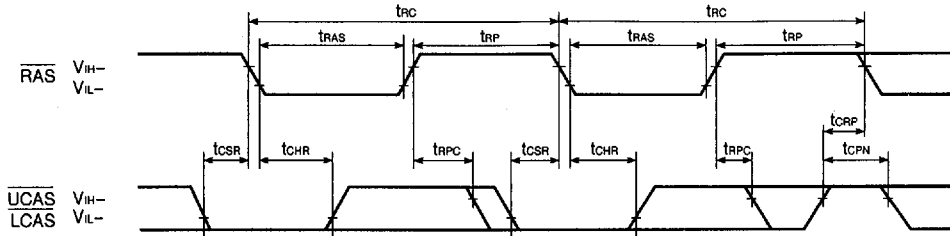
(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied. And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

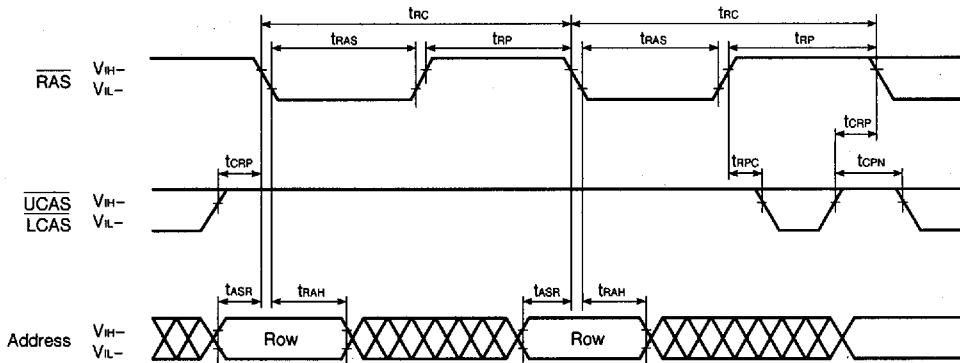
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



Remark \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)

