FUJITSU

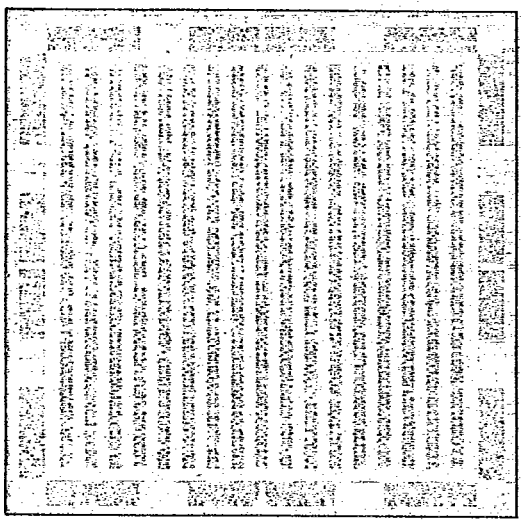
Bipolar Gate Array

GENERAL INFORMATION

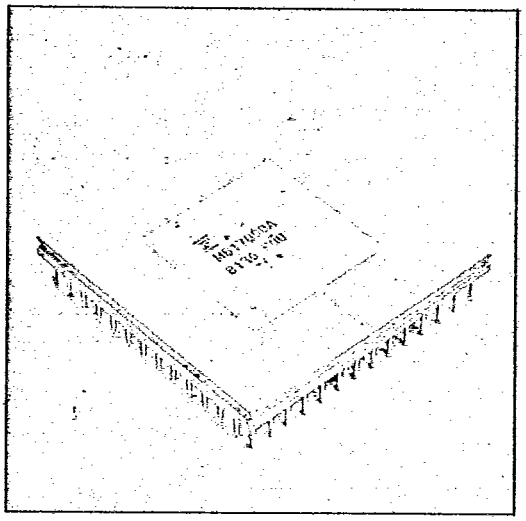
The Fujitsu bipolar gate array family consists of five device types fabricated with low-power Schottky TTL (Transistor-Transistor-Logic) technology. The arrays contain from 240 to 2108 internal 3-input NAND gates and Input/Output buffers. With the application of a customized double-layer metal mask, the gates and buffers may be interconnected to form a wide variety of high density and high performance random logic configurations.

To reduce the design task of the customer, the functions of standard SSI's and MSI's such as 74LS series are prepared as macros called "F-MACRO" in the library.

To assure quick, simple and error-free implementation of the metal interconnection routing, Fujitsu utilizes a unique Computer Aided Design (CAD) system to interface customer specification with the manufacturing function. This CAD software provides the physical layout of the array, line routing, mask pattern data generation and test programs, as well as computer simulation of the final circuit.

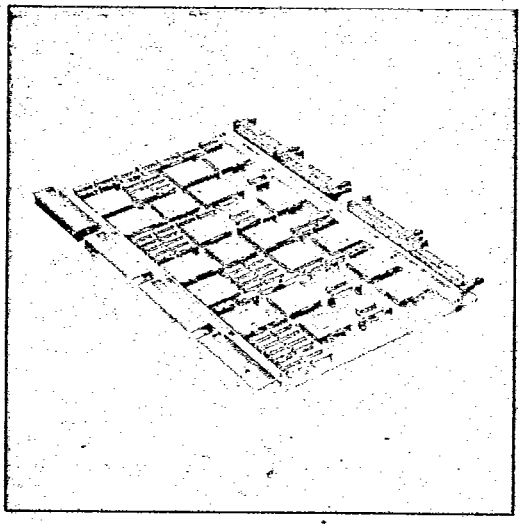


B-2000 Die, Before Metalization



RIT-135 Package

B-2000 Die, After Metalization



Fujitsu Gate Arrays, Replacing a Lot of MSI/SSI

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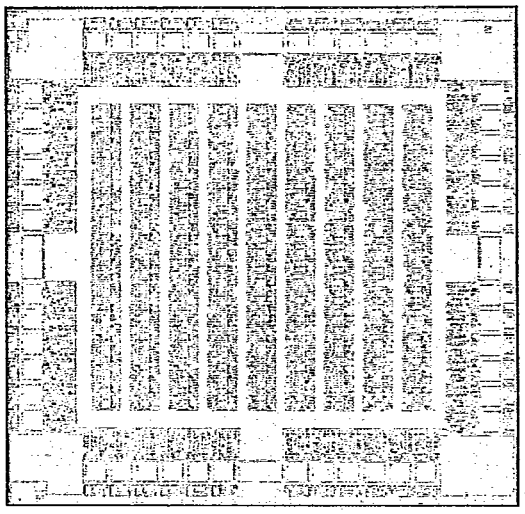
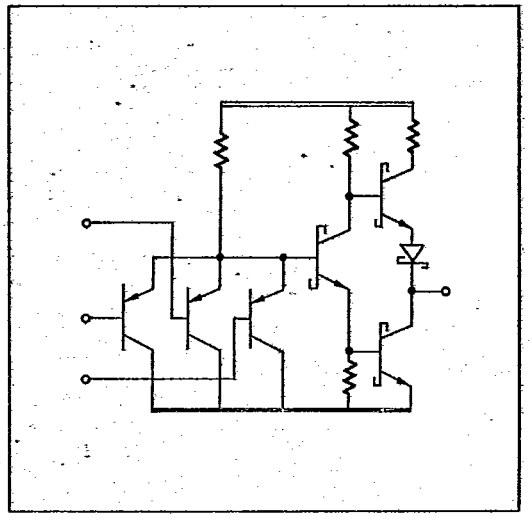
Bipolar Gate Array

FEATURES

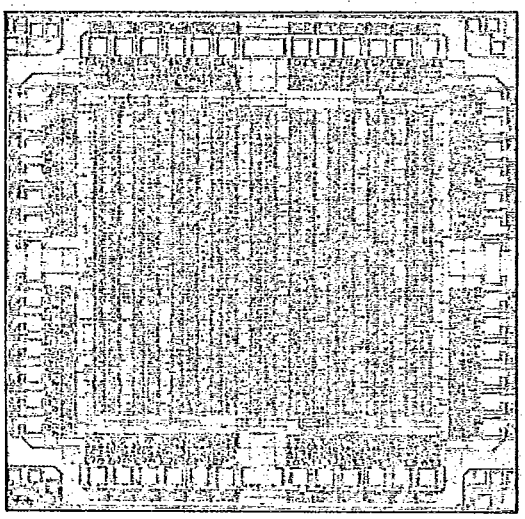
- Fast turn-around on design
- Replaces typically 30 to over 100 TTL SSI/MSI packages
- Simplified customer interface
  (only logic design and test pattern information required)
- Design support on major CAE workstations
- Fully supported by FUJITSU CAD system
  (logic validation, physical layout, metal interconnection and test program)
- Variety of software macros called "F-MACRO", equivalent to MSI functions
- Two speed versions, standard and high speed, available for the Logic Block Family of B-240, B-350, B-600, and B-1100.
- TTL Compatible Input/Output characteristics
- High-speed, low-power internal gate
- High input impedance input buffer with PNP transistor
- Four output buffer options
  (totem-pole, open-collector, 3-state, bidirectional)
- The B-240, B-350, B-600, B-1100 and B-2000 are alternate sourced by Texas Instruments Incorporated, USA and Monolithic Memories Incorporated, USA.



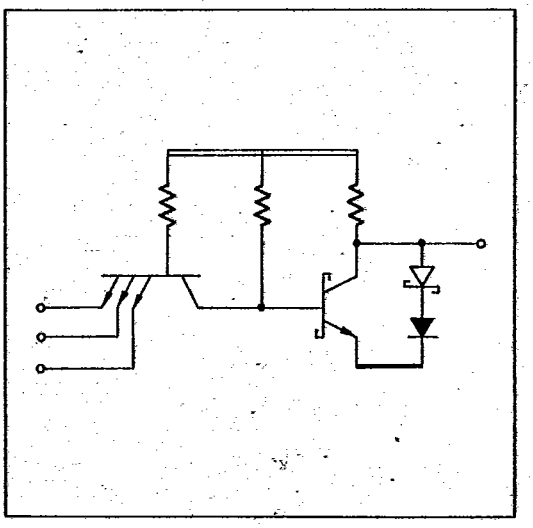
B-350 Die, Before Metalization



Internal Basic Gate Schematic for B-240, B-350, B-600 and B-1100



B-350 Die, After Metalization



Internal Basic Gate Schematic for B-2000

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Bipolar Gate Array

DEVICE DESCRIPTION

Device Name	Part Number	Complexity[1]	Cell[2] Propagation Delay	Max. Number of Signal Pins	Output Options	Supply Voltage	Operating Temp. Range
B-240	MB 111Δ[5]xxx	240 gates	1.65 ns (Standard)[6] 1.0 ns (H-version)[6]	40	Totem pole Open-collector 3-state Bidirectional	5V ± 5%	0 to 70°C
B-350	MB 112Δ[5]xxx	360 gates		48			
B-600	MB 113Δ[5]xxx	616 gates		64			
B-1100	MB 114Δ[5]xxx	1120 gates		88			
B-2000	MB 17xxx	2108 gates	0.95 ns	112		5V ± 5% 2.3 ± 0.2V	

1: 3-input NAND equivalent.
2: 3-input NAND, Ring Oscillator, F/O = 1.
3: From the customer's design approval to engineering sample shipment.
4: I_{OL} = 24mA is possible with a certain restriction on pin assignment.
5: Δ will be "S", "T" or "F" depending on the number of power supply and ground pins.
6: Two speed versions, standard and high speed (H-version), available.

PACKAGE OPTIONS

Device Name	DIP-14	DIP-16	DIP-18	DIP-20	DIP-22	DIP-24	DIP-28	DIP-40	DIP-42
B-240	■	◆ ■	◆ ■	◆ ■	◆ ■	◆ ■	◆ ■ ▮	◆ ■	■ ▮
B-350					◆ ■	◆ ■	◆ ■ ▮	◆ ■	■ ▮
B-600						◆ ■	◆ ■	◆ ■	◆ ■ ▮
B-1100									
B-2000									

◆: Ceramic
■: Plastic
▮: Plastic (Shrink type DIP: Lead spacing center to center: 0.07")

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Power Dissipation	DC Characteristics					Normal[3] Max Turn-around Time	Device Name
	Output High Voltage	Output Low Voltage	Input High Voltage	Input Low Voltage	Input Clamp Voltage		
0.8mW/gate typ. (Standard)[6] 1.2mW/gate typ. (H-version)[6]	2.4V (min) at I_{OH} = –3.3mA	0.5V (max) at I_{OL} = 10mA or I_{OL} = 24mA[4]	2.0V (min)	0.8V (max)	–1.5V at 18mA	6 weeks	B-240
						6 weeks	B-350
						6 weeks	B-600
						6 weeks	B-1100
0.65mW/gate typ.	2.4V (min) at I_{OH} = –2.6mA	0.5V (max) at I_{OL} = 8 or 16mA			–1.5V at 18mA	8 weeks	B-2000

DIP-48	DIP-64	FPT-28	FPT-48	PLCC 44	PLCC 68	RIT-64	RIT-88	RIT-107	RIT-135	Device Name
▮		■	■	■						B-240
▮	▮		■	■		♦				B-350
♦ ▮	▮		■	■	■	♦	♦			B-600
						♦	♦	♦		B-1100
								♦	♦	B-2000

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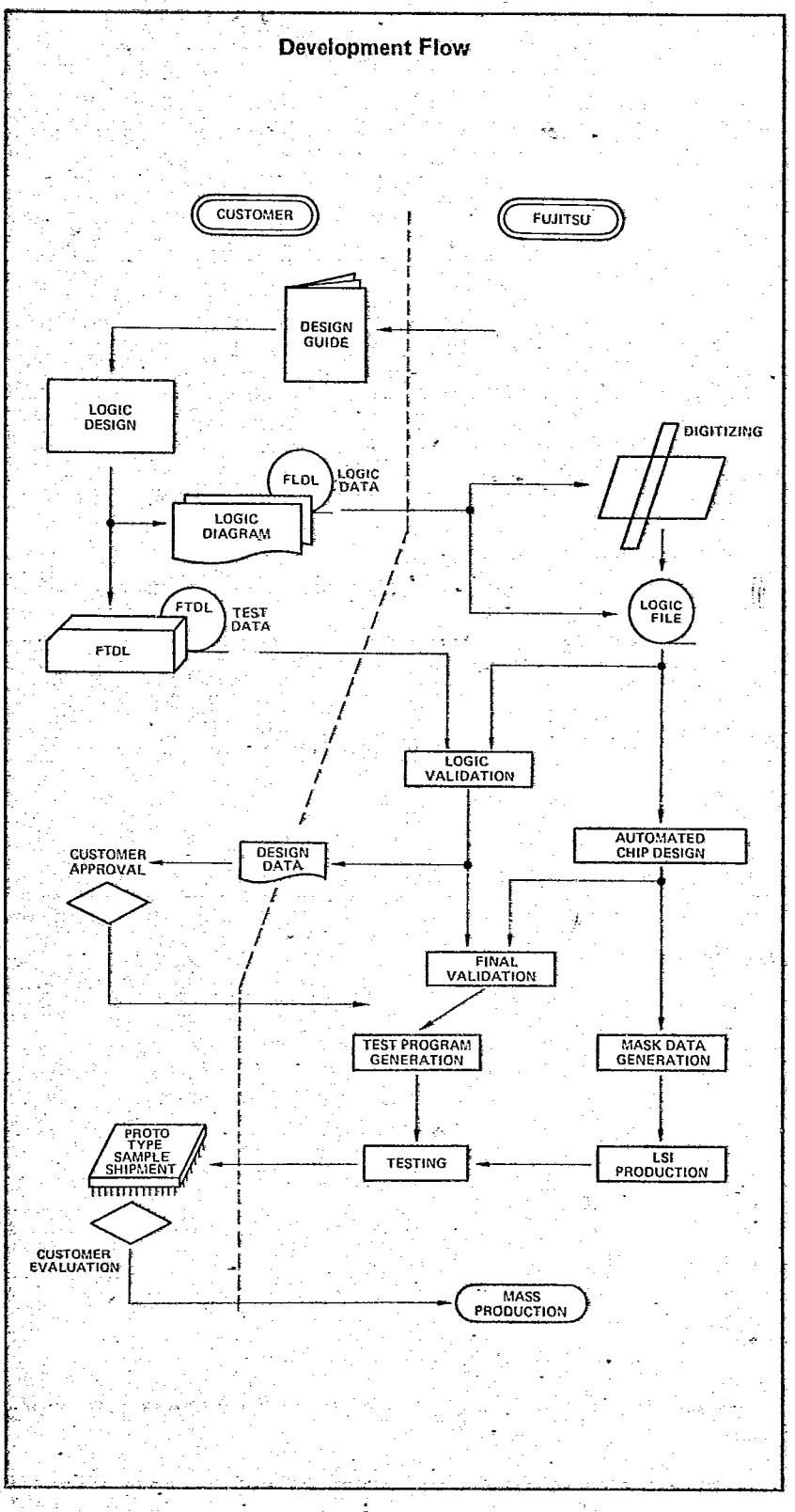
Bipolar Gate Array

CUSTOMER/FUJITSU INTERFACE

In designing a custom LSI, there is a well-known sequence of customer and supplier activities, which are prerequisites to successful definition and delivery of the final product. These include logic design, specification of minimal timing restrictions, digitizing, layout, checkout, iterations, rework, multi-mask fabrication, test program generation and final part approval. Many of these tasks are eliminated, or at least simplified, by use of Fujitsu gate arrays. There are only two data inputs required from the customer: logic data and test pattern data both prepared in Fujitsu format. These logic data define the function performed by the gate array. Fujitsu has designed many types of logic functions which are made up of combinations of the basic 3-input NAND gates. The only restriction of these logic function cells is that the design does not exceed the total number of basic 3-input NAND gates contained in each bipolar gate array. The test data simply defines the functional relationship and AC requirement between the input and output pins of the circuit. This assures that the computerized layout for the interconnect metal mask accommodates the maximum time-delay caused by the metal mask line routing.

Furthermore, with both logic and test pattern data, Fujitsu performs logic validation for error-free design of the bipolar gate arrays. An interconnect layout is produced to verify AC performance and a final test program is generated. An interconnect metal mask can then be fabricated for the final processing of wafers. Within a short time after customer approval Fujitsu can deliver prototype samples.



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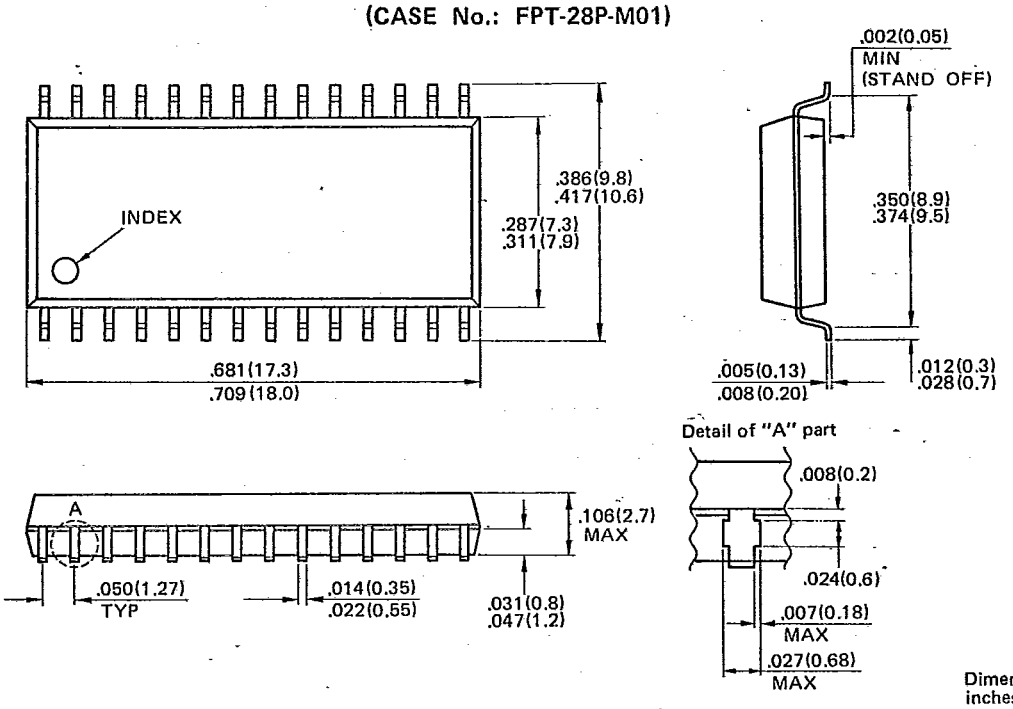
Bipolar Gate Array

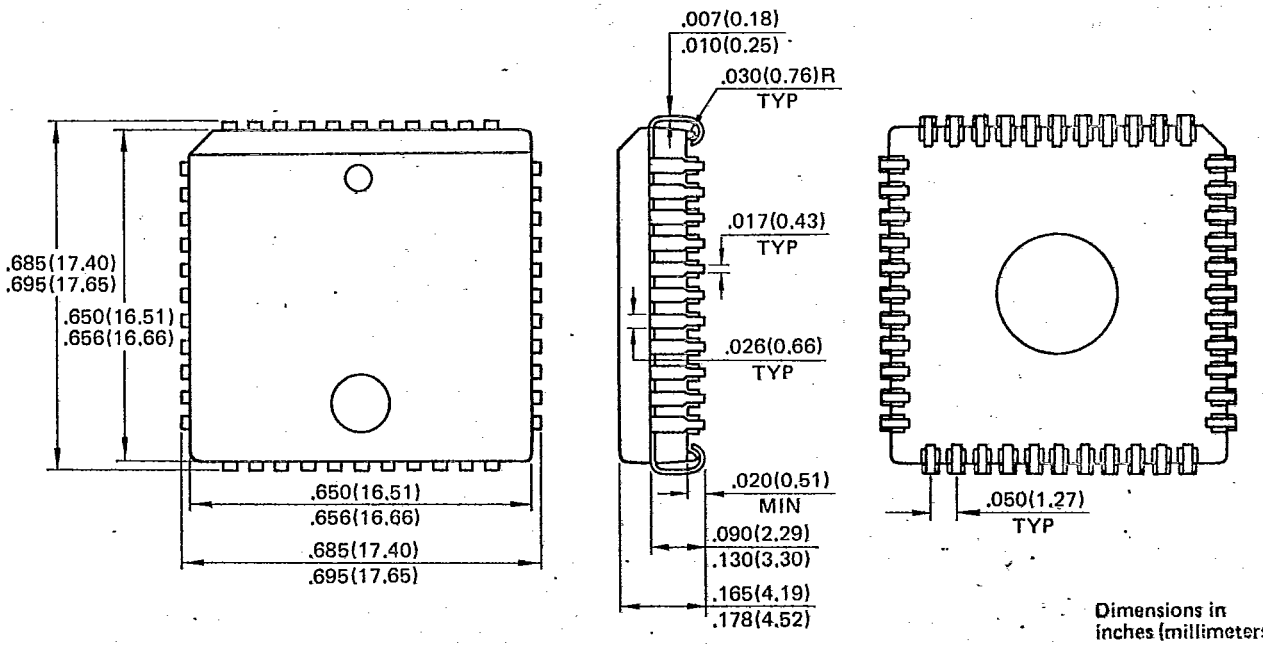
PACKAGE DIMENSIONS

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M01)



Dimensions in inches (millimeters)

44-LEAD PLASTIC CHIP CARRIER
(CASE No.: LCC-44P-M01)



Dimensions in inches (millimeters)

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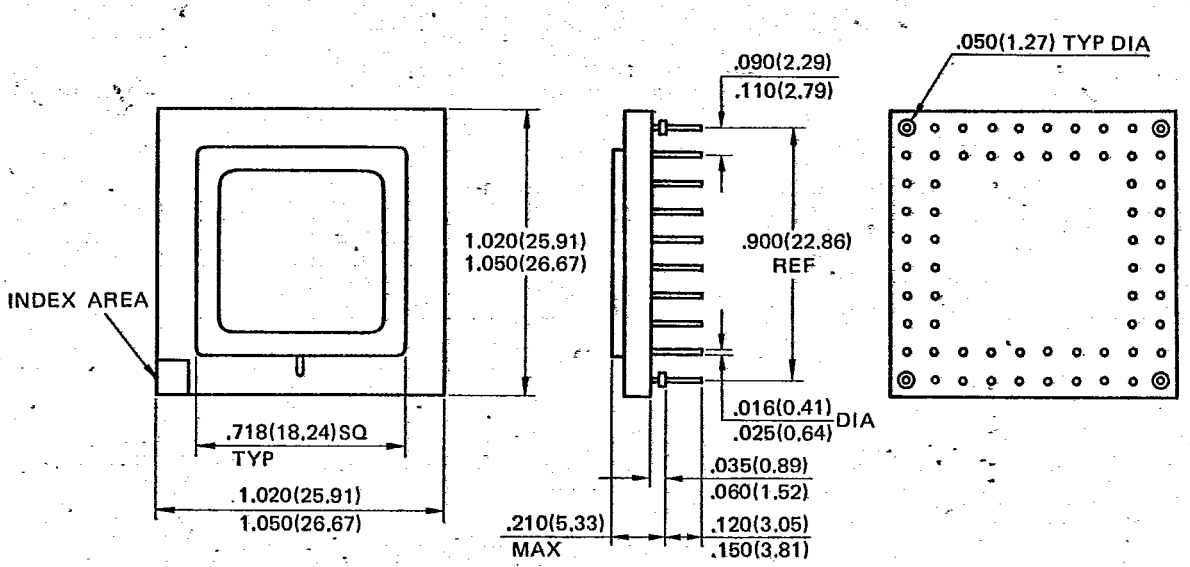
Bipolar Gate Array

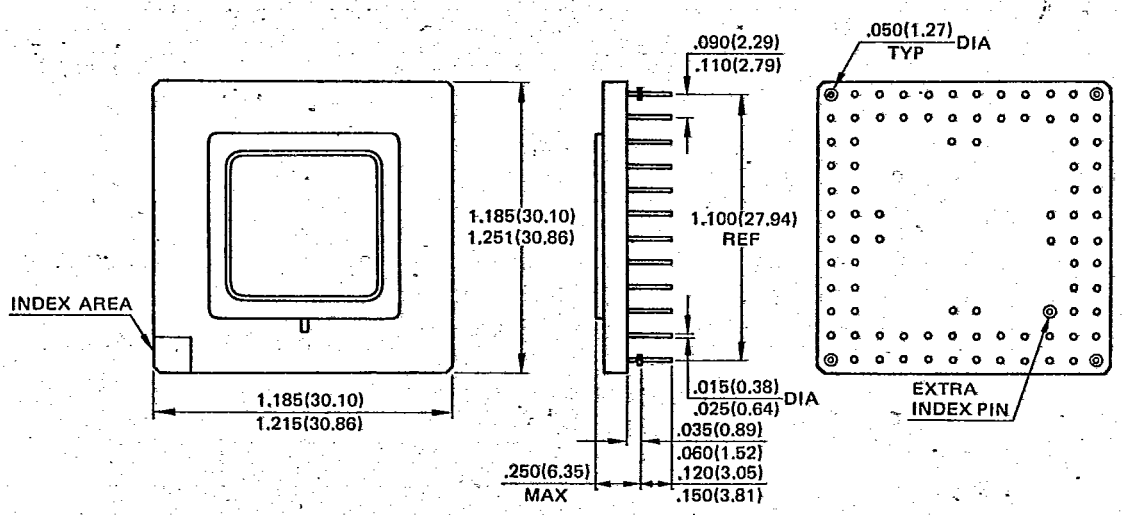
PACKAGE DIMENSIONS (cont'd)

64-LEAD CERAMIC (METAL SEAL) REPEATED QUAD IN-LINE PACKAGE
(CASE No.: RIT-64C-A01)



Dimensions in inches (millimeters)

88-LEAD CERAMIC (METAL SEAL) REPEATED QUAD IN-LINE PACKAGE
(CASE No.: RIT-88C-A02)



Dimensions in inches (millimeters)

2585 C-04

LOGIC BLOCK FAMILY

Internal Logic Block Family

Name	Function	B-240, B-350 B-600, B-1100	B-2000
ST0	Stuck at "L"	●	●
ST1	Stuck at "H"	●	●
PU1	Pull up Booster		●
PU2	Pull up Booster		●
N01	Inverter	■1 ●	●
N02	2-input NAND	■1 ●	●
N03	3-input NAND	■1 ●	●
N04	4-input NAND	■1 ●	●
N05	5-input NAND	■1 ●	●
N06	6-input NAND	■1 ●	●
N07	7-input NAND	■1 ●	●
N08	8-input NAND	■1 ●	●
N09	9-input NAND	■1 ●	●
N10	10-input NAND	■1 ●	●
N11	11-input NAND	■1 ●	●
N12	12-input NAND	■1 ●	●
A01	1-input AND	■1 ●	●
A02	2-input AND	■1 ●	●
A03	3-input AND	■1 ●	●
A04	4-input AND	■1 ●	●
A05	5-input AND	■1 ●	●
A06	6-input AND	■1 ●	●
A07	7-input AND	■1 ●	●
A08	8-input AND	■1 ●	●
A09	9-input AND	■1 ●	●
A10	10-input AND	■1 ●	●
A11	11-input AND	■1 ●	●
A12	12-input AND	■1 ●	●
EOR2	Exclusive OR	■1 ●	●
ENR2	Exclusive NOR	■1 ●	●
AN22	2-input 2-wide AND-NOR	■1 ●	●
AN32	3-input 2-wide AND-NOR	■1 ●	●
AN42	4-input 2-wide AND-NOR	■1 ●	●
AN52	5-input 2-wide AND-NOR	■1 ●	●
AN62	6-input 2-wide AND-NOR	■1 ●	●
AN23	2-input 3-wide AND-NOR	■1 ●	●
AN33	3-input 3-wide AND-NOR	■1 ●	●
AN43	4-input 3-wide AND-NOR	■1 ●	●
AN53	5-input 3-wide AND-NOR	■1 ●	●
AN63	6-input 3-wide AND-NOR	■1 ●	●
AN24	2-input 4-wide AND-NOR	■1 ●	●
AN34	3-input 4-wide AND-NOR	■1 ●	●
AN44	4-input 4-wide AND-NOR	■1 ●	●
AN54	5-input 4-wide AND-NOR	■1 ●	●
AN64	6-input 4-wide AND-NOR	■1 ●	●
NR2	2-input NOR	■1 ●	●
NR3	3-input NOR	■1 ●	●
NR4	4-input NOR	■1 ●	●
LS1	S-$\overline{R}$ Latch	■1 ●	●
LS2	Gated S-R Latch with Clear and Preset	■1 ●	●
LD1	D-Latch with Clear	■1 ●	●
LD2	D-Latch with Clear and Preset	■1 ●	●
LD3	D-Latch with Clear and Preset	■1 ●	●
FD1	D-type Flip-Flop	■1 ●	●
FD2	2-wide 2-input D-type Flip-Flop	■1 ●	●
FJ1	J-XK Type Flip-Flop	■1 ●	●
FJ3	J-XK Type Flip-Flop with 3 by 1 J-XK/CR/PR		●
FT1	Toggle Flip-Flop	■1 ●	

Note: ■1 shows the availability of H-version (High speed version) Logic Block.
The Logic Block names of H-version are suffixed with "H". The 'H-version' of N02, for example, is named N02H.

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Bipolar Gate Array

Input/Output Buffer Family

Name	Function	B-240, B-350 B-600, B-1100	B-2000
IC1	Complementary 1-input Input Buffer		●
IC1P	Complementary 1-input Input Buffer with Input Pull-up		●
IA1	1-input AND Input Buffer	■[1] ●	●
IA1P	1-input AND Input Buffer with Input Pull-up	●	●
IN1	1-input NAND Input Buffer	■[1] ●	●
IN1P	1-input NAND Input Buffer with Input Pull-up	●	●
IN1F	1-input, 2-output NAND Input Buffer	●	
IN1S	Inverting Schmitt-Trigger Input Buffer	●	●
IC2	Complementary 2-input Input Buffer		●
IA2	2-input AND Input Buffer		●
IN2	2-input NAND Input Buffer		●
ON1	1-input NAND Output Buffer	● ♦[2]	● ♦[2]
ON2	2-input NAND Output Buffer	● ♦[2]	● ♦[2]
ON3	3-input NAND Output Buffer	● ♦[2]	● ♦[2]
ON1O	1-input NAND Output Buffer (O/C type)	● ♦[2]	● ♦[2]
ON2O	2-input NAND Output Buffer (O/C type)	● ♦[2]	● ♦[2]
ON3O	3-input NAND Output Buffer (O/C type)	● ♦[2]	● ♦[2]
ON1T	1-input NAND Output Buffer (3-state output)	● ♦[2]	● ♦[2]
ON2T	2-input NAND Output Buffer (3-state output)	● ♦[2]	● ♦[2]
OA1	1-input AND Output Buffer	● ♦[2]	● ♦[2]
OA2	2-input AND Output Buffer	● ♦[2]	● ♦[2]
OA3	3-input AND Output Buffer	● ♦[2]	● ♦[2]
OA1O	1-input AND Output Buffer (O/C type)	● ♦[2]	● ♦[2]
OA2O	2-input AND Output Buffer (O/C type)	● ♦[2]	● ♦[2]
OA3O	3-input AND Output Buffer (O/C type)	● ♦[2]	● ♦[2]
OA1T	1-input AND Output Buffer (3-state output)	● ♦[2]	● ♦[2]
OA2T	2-input AND Output Buffer (3-state output)	● ♦[2]	● ♦[2]
BN1C	Bidirectional Buffer Output: 1-input NAND, Input: 1-input Complementary		●
BN2C	Bidirectional Buffer Output: 2-input NAND, Input: 1-input Complementary		●
BN1A	Bidirectional Buffer Output: 1-input NAND, Input: 1-input AND	●	●
BN2A	Bidirectional Buffer Output: 2-input NAND, Input: 1-input AND	●	●
BN1N	Bidirectional Buffer Output: 1-input NAND, Input: 1-input NAND	●	●
BN2N	Bidirectional Buffer Output: 2-input NAND, Input: 1-input NAND	●	●
BN1NF	Bidirectional Buffer Output: 1-input NAND, Input: 1-input, 2-output NAND	●	
BN2NF	Bidirectional Buffer Output: 2-input NAND, Input: 2-input, 2-output NAND	●	
BA1C	Bidirectional Buffer Output: 1-input AND, Input: 1-input Complementary		●
BA2C	Bidirectional Buffer Output: 2-input AND, Input: 1-input Complementary		●
BA1A	Bidirectional Buffer Output: 1-input AND, Input: 1-input AND	●	●
BA2A	Bidirectional Buffer Output: 2-input AND, Input: 1-input AND	●	●
BA1N	Bidirectional Buffer Output: 1-input AND, Input: 1-input NAND	●	●
BA2N	Bidirectional Buffer Output: 2-input AND, Input: 1-input NAND	●	●
BA1NF	Bidirectional Buffer Output: 1-input AND, Input: 1-input, 2-output NAND	●	
BA2NF	Bidirectional Buffer Output: 2-input AND, Input: 1-input, 2-output NAND	●	

Note: ■[1] shows the availability of H-version (High speed version) Logic Block. The Logic Block names of H-version are suffixed with "H".
♦[2] shows the availability of Driver Output Buffers. The names of Driver Output Buffers are suffixed with "D".

F-MACRO FAMILY

Name	Function Equivalent	Number of Basic Gates	
		B-240, B-350 B-600, B-1100	B-2000
F00	74LS00	4	4
F02	74LS02	8	8
F04	74LS04	6	6
F08	74LS08	8	8
F10	74LS10	3	3
F11	74LS11	6	6
F20	74LS20	4	4
F21	74LS21	4	4
F25	7425	12	12
F27	74LS27	12	12
F30	74LS30	4	4
F32	74LS32	12	12
F42	74LS42	24	34
F43	7443A	24	36
F44	7444A	24	36
F51	74LS51	4	4
F54	74LS54	4	6
F55	74LS55	4	4
F56	74LS56	56	-
F57	74LS57	52	-
F64	74S64	8	6
F68	74LS68	62	64
F69	74LS69	52	57
F73	74LS73A	20	20
F74	74LS74A	12	12
F75	74LS75	20	20
F76	74LS76A	20	20
F77	74LS77	18	18
F78	74LS78A	19	19
F82	7482	19	25
F83	74LS83A	65	75
F85	74LS85	40	52
F86	74LS86	16	16
F87	74H87	26	26
F90	74LS90	34	38
F91	74LS91	52	57
F92	74LS92	32	32
F93	74LS93	27	32
F94	7494	33	37
F95	74LS95B	35	40
F96	74LS96	38	43
F97	7497	92	109
F98	54L98	34	36
F99	54L99	38	41
F100	74100	40	46
F101	74H101	14	14
F102	74H102	13	13
F103	74H103	20	20
F106	74H106	20	20
F107	74LS107	20	20
F108	74H108	19	19
F109	74LS109A	16	16
F112	74LS112A	20	20
F113	74LS113	20	20
F114	74LS114A	19	19
F116	74116	58	48
F120	74120	20	20
F135	74S135	32	32
F137	74LS137	35	43
F138	74LS138	24	26
F139	74LS139	14	18
F147	74LS147	35	36

Name	Function Equivalent	Number of Basic Gates	
		B-240, B-350 B-600, B-1100	B-2000
F148	74LS148	34	36
F150	74150	46	56
F151	74LS151	25	25
F152	74LS152	23	29
F153	74LS153	14	16
F154	74154	44	59
F155	74LS155	15	17
F157	74LS157	15	17
F158	74LS158	10	13
F160	74LS160A	56	61
F161	74LS161A	54	62
F162	74LS162A	59	62
F163	74LS163A	58	63
F164	74LS164	56	62
F165	74LS165	70	77
F166	74LS166	73	79
F167	74LS167	-	61
F168	74S168	82	98
F169	74LS169B	73	82
F171	74LS171	24	30
F174	74LS174	42	44
F175	74LS175	24	30
F176	74176	39	45
F177	74177	35	40
F178	74178	43	47
F179	74179	43	50
F180	74180	29	33
F181	74LS181	91	117
F182	74182	28	39
F183	74LS183	22	26
F190	74LS190	71	85
F191	74LS191	68	82
F192	74LS192	62	74
F193	74LS193	58	74
F194	74LS194A	47	50
F195	74LS195A	35	42
F198	74198	91	96
F199	74199	75	81
F260	74S260	14	12
F261	74LS261	53	67
F273	74LS273	54	58
F278	74278	31	35
F279	74LS279	8	8
F280	74LS280	32	51
F283	74LS283	60	61
F290	74LS290	32	38
F293	74LS293	27	32
F298	74LS298	34	36
F352	74LS352	22	32
F375	74LS375	18	18
F377	74LS377	69	60
F378	74LS378	53	46
F379	74LS379	33	32
F381	74LS381	102	144
F382	74LS382	106	152
F386	74LS386	16	16
F390	74LS390	64	64
F393	74LS393	52	52
F396	74LS396	67	72
F398	74LS398	33	37
F399	74LS399	33	37