

74ACT158 Quad 2-Input Multiplexer

General Description

The ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The ACT158 can also be used as a function generator.

Features

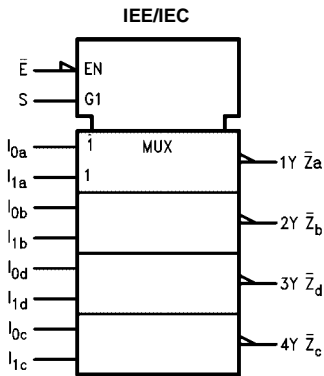
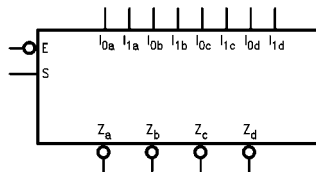
- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

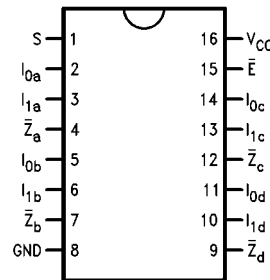
Order Number	Package Number	Package Description
74ACT158SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT158PC	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT158MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT158SJ	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
\bar{E}	Enable Input
S	Select Input
$\bar{Z}_a-\bar{Z}_d$	Inverted Outputs

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Functional Description

The ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (\bar{Z}) are forced HIGH regardless of all other inputs. The ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

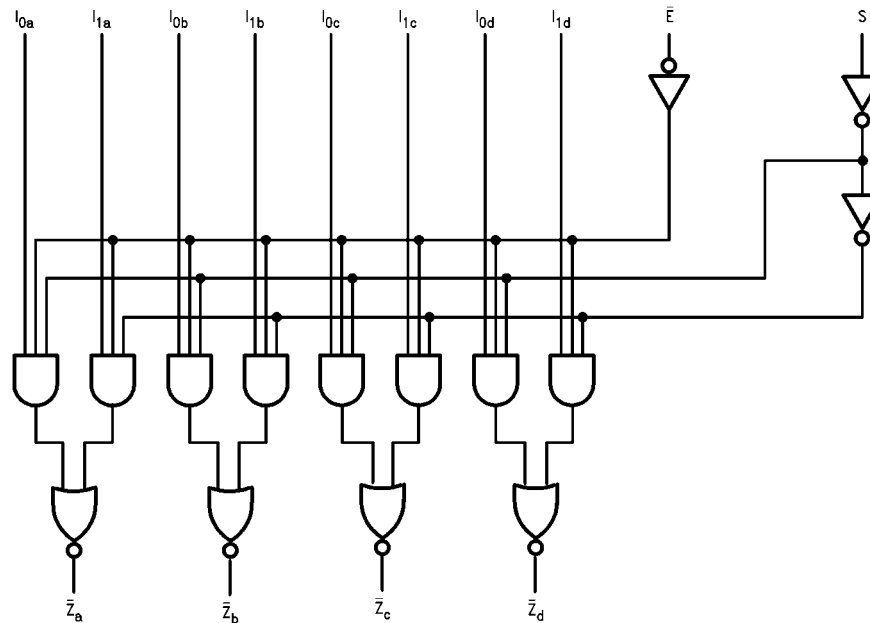
A common use of the ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

\bar{E}	Inputs			\bar{Z}
	S	I_0	I_1	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 1)		Recommended Operating Conditions	
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage (V_{CC})	4.5V to 5.5V
DC Input Diode Current (I_{IK})		Input Voltage (V_I)	0V to V_{CC}
$V_I = -0.5V$	-20 mA	Output Voltage (V_O)	0V to V_{CC}
$V_I = V_{CC} + 0.5V$	+20 mA	Operating Temperature (T_A)	-40°C to +85°C
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ($\Delta V/\Delta t$)	
DC Output Diode Current (I_{OK})		V_{IN} from 0.8V to 2.0V	
$V_O = -0.5V$	-20 mA	V_{CC} @ 4.5V, 5.5V	125 mV/ns
$V_O = V_{CC} + 0.5V$	+20 mA		
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$		
DC Output Source or Sink Current (I_O)	± 50 mA		
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		
Junction Temperature (T_J)	140°C		

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variable. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8			
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$	
		5.5		4.86	4.76			
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$	
		5.5		0.36	0.44			
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, GND$	
I_{CCT}	Maximum $I_{CC}/Input$	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
I_{OHD}		5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.
Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

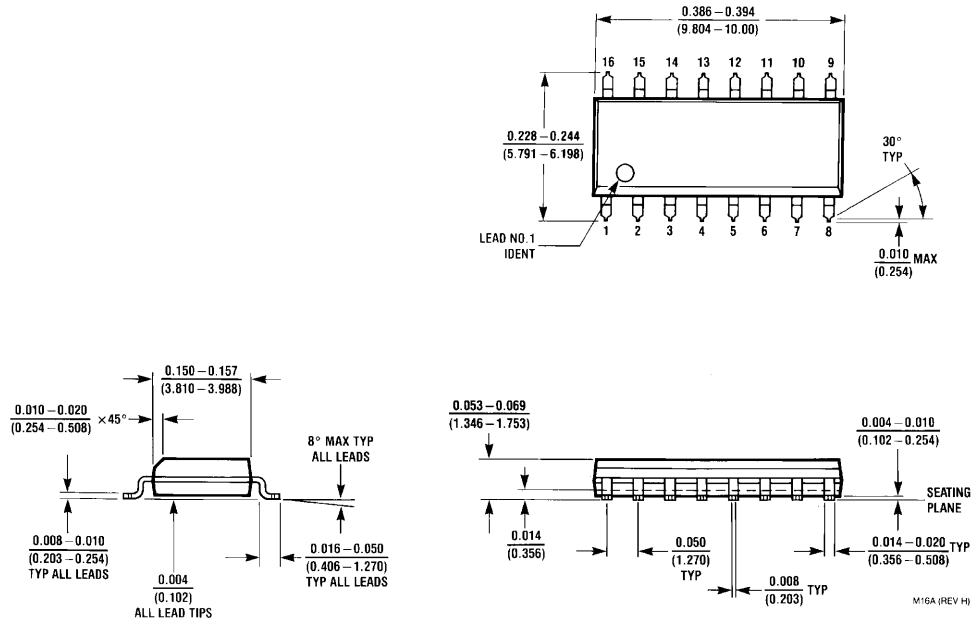
Symbol	Parameter	V _{CC} (V) (Note 4)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay S to \bar{Z}_n	5.0	2.5	6.0	9.5	2.0	11.0	ns
t _{PHL}	Propagation Delay S to \bar{Z}_n	5.0	1.5	5.5	9.0	1.5	10.0	ns
t _{PLH}	Propagation Delay \bar{E} to \bar{Z}_n	5.0	1.5	5.5	9.5	1.5	10.5	ns
t _{PHL}	Propagation Delay \bar{E} to \bar{Z}_n	5.0	1.5	5.5	9.5	1.5	10.5	ns
t _{PLH}	Propagation Delay I _n to \bar{Z}_n	5.0	1.5	4.5	8.0	1.0	8.5	ns
t _{PHL}	Propagation Delay I _n to \bar{Z}_n	5.0	1.5	4.0	6.5	1.0	7.5	ns

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	45.0	pF	V _{CC} = 5.0V

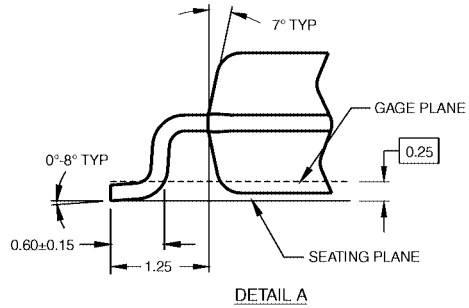
Physical Dimensions inches (millimeters) unless otherwise noted



**16- Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A**

M16A (REV H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

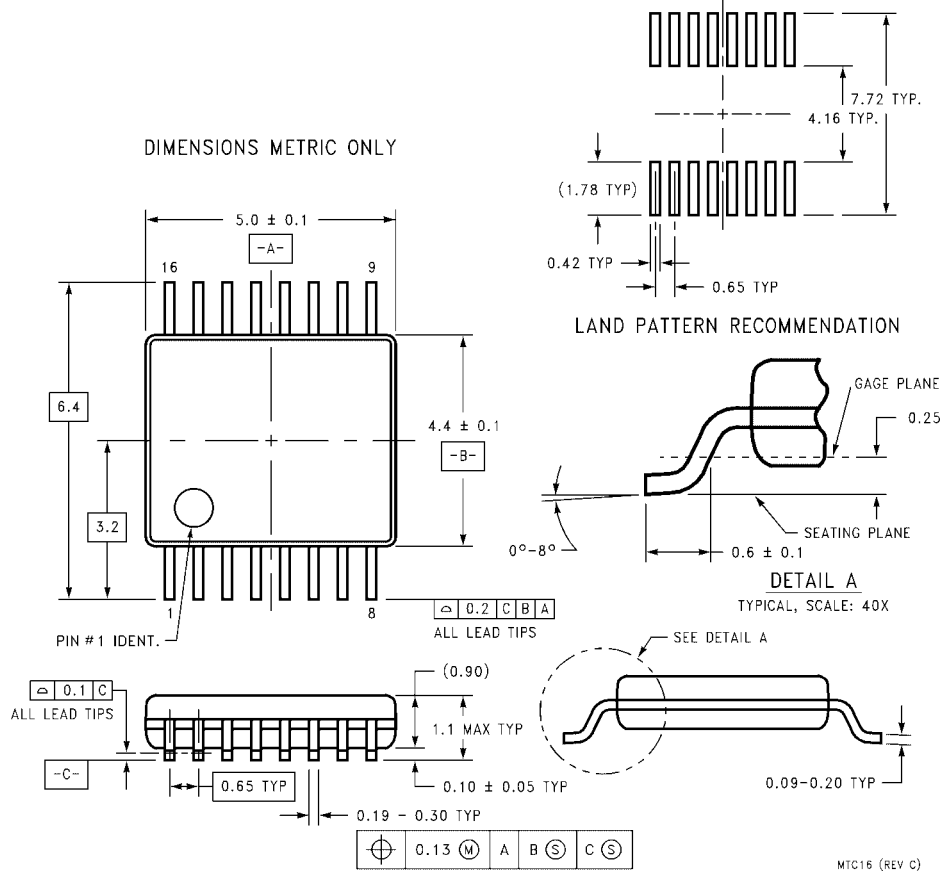


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRRevB1

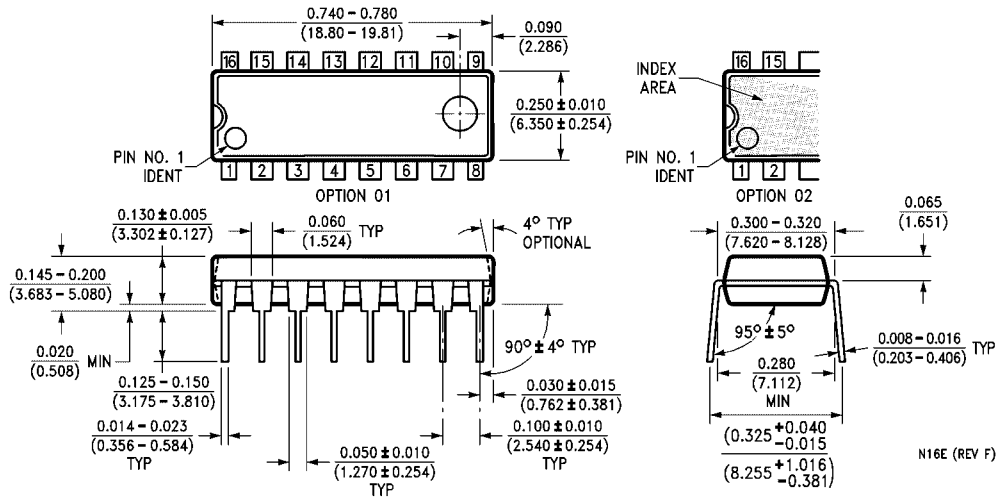
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

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