NEC
NEC Electronics Inc.

μPD9601AD/9602AD
CMOS PCM
CODEC-FILTER COMBINATION

February 1988

Description

The μPD9601AD and μPD9602AD are PCM codec-filter combo chips, A-law and μ-law compatible, respectively. These monolithic CMOS LSIs include phase-locked loops (PLL) that derive internal signal processing clocks from the transmit and receive frame sync clock inputs.
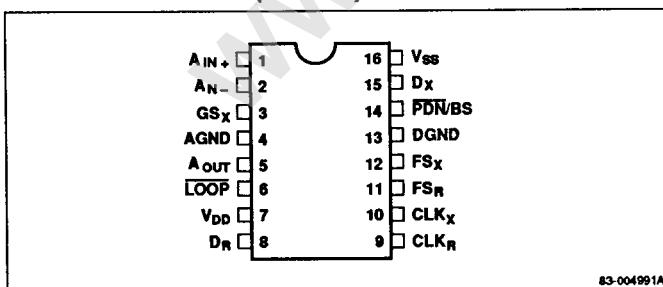
Features

☐ Transmit input operational amplifier
☐ Transmit active lowpass filter and switched-capacitor bandpass filter
☐ Autozero circuit
☐ Receive unbalanced 600-Ω output power amplifier
☐ Receive switched-capacitor lowpass filter
☐ Digital serial I/O interface circuit
☐ A-law (9601AD) and μ-law (9602AD) companding
☐ Precision reference voltage circuit
☐ Synchronous or asynchronous operation
☐ Data rate, 64 kb/s to 2.048 Mb/s
☐ Low power dissipation
   — 50 mW normal mode
   — 5 mW power-down or standby mode
☐ 16-pin ceramic DIP

Ordering Information

Part No.	Companding	Package Type
μPD9601AD	A-law	16-pin ceramic DIP (300 mil)
μPD9602AD	μ-law	

Pin Configuration

16-Pin Ceramic DIP (300 mil)

83-004991A

Pin Identification

Pin No.	Symbol	Function
1	$A_{IN}+$	Transmit analog input; noninverting input to opamp.
2	$A_{IN}-$	Transmit analog input; inverting input to opamp.
3	GS_X	Transmit opamp external gain setting resistor.
4	AGND	Analog ground; no internal connection to digital ground.
5	A_{OUT}	Receive analog output from power amplifier; unbalanced 600 Ω.
6	$\overline{LOOP}$	Input control for analog loopback test. TTL level; internal pullup. An open or connection to V_{SS} disables loopback.
7	V_{DD}	Positive 5-volt power supply (+5 ±0.25).
8	D_R	Receive PCM data input; TTL level.
9	CLK_R	Receive data clock input, 64 kHz to 2.048 MHz; TTL level. For CLK_X, either synchronous or asynchronous operation can be used; however, for FS_R, only synchronous operation can be used.
10	CLK_X	Transmit data clock input, 64 kHz to 2.048 MHz; TTL level. For CLK_R, either synchronous or asynchronous operation can be used; however, for FS_X, only synchronous operation can be used.
11	FS_R	Receive frame sync clock input. TTL level; internal pullup.
12	FS_X	Transmit frame sync clock input. TTL level; internal pullup.
13	DGND	Digital ground; no internal connection to analog ground.
14	$\overline{PDN}/BS$	Control input for power-down (9601AD, 9602AD) and bit steal (9602AD); TTL level. On 9601AD, a low level initiates power-down. On 9602AD, the low level must be maintained for more than seven frames; a low-to-high or high-to-low transition within six frames activates bit steal.
15	D_X	Transmit PCM data output (open drain).
16	V_{SS}	Negative 5-volt power supply (−5 ±0.25).

1

Block Diagram
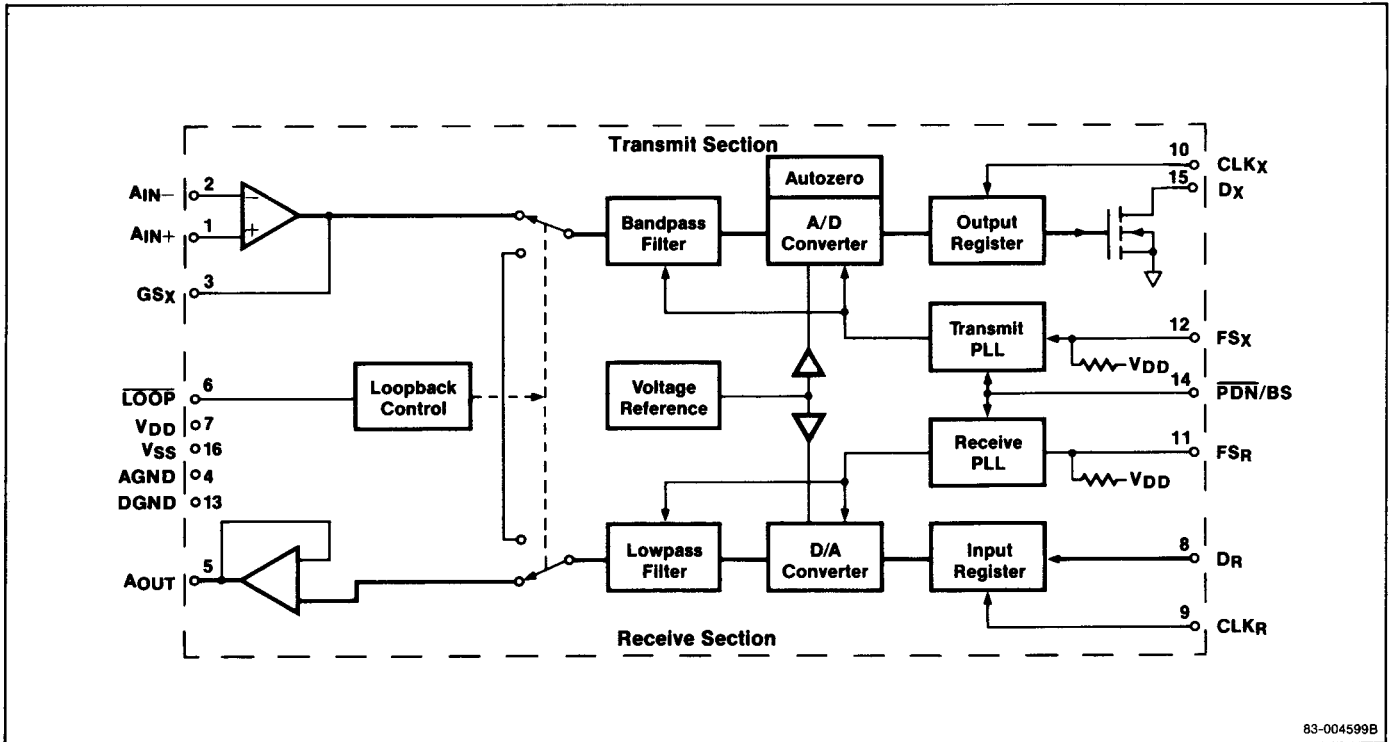
83-004599B

Operational Description

Power-Up

The μPD9601AD and μPD9602AD have internal reset circuits that protect other devices on the PCM highway during the power-up sequence. For about 5 ms after power is applied, digital output D_X is held in a high-impedance state. Analog circuits such as filters, sample-and-hold, and D/A converters begin functioning after a 15-ms settling period.

Power-Down Mode

Setting the $\overline{PDN}$/BS pin to TTL low level initiates the power-down mode. Digital output D_X goes to high-impedance state and all circuits are disabled except the power-down controller, data clocks, frame sync buffers, and PLLs.

A TTL high level on the $\overline{PDN}$/BS pin restores normal operation after the same delays as in power-up, but without the PLL lock-in time.

Standby Mode

In standby mode, each section is powered down independently by an open circuit or a TTL low level on FS_X (transmit section) or FS_R (receive section).

PCM Data Transmission

As shown in the transmit 1 timing waveform, if FS_X is high at the rising edge of CLK_X, the MSB of the channel PCM word is output at the D_X pin. Similarly, bits 2 through 8 are output at the next seven rising edges of CLK_X, after which the D_X pin is restored to the high-impedance state.

The transmit 2 timing waveform shows the condition in which CLK_X leads FS_X. In either transmit 1 or transmit 2, the overlapping high-level width of the two clocks is at least 100 ns.

The receive timing waveforms are similar to the transmit timing waveforms except data is clocked in and latched on the falling edge of CLK_R.

Bit Stealing, µPD9602AD Only

Over a 12-frame interval, in frames 1-5 and 7-11, the receive section decodes the vf information in the 8-bit channel pcm words. In signaling frames 6 and 12, the LSB (bit 8) is assigned to convey the channel signaling state. (Bit 8 is "stolen," leaving just 7 bits for vf information.) Although the µPD9602AD does not have a channel signaling interface, it performs 7-bit vf decoding in signaling frames 6 and 12. Design of the D/A converter minimizes the deterioration of gain tracking and signal-to-distortion characteristics resulting from 7-bit vf transmission in one frame out of every six.

To activate bit stealing, the associated digital equipment applies a control signal to the $\overline{PDN}$/BS pin. As shown in the receive timing waveforms, the BS signal is low and high in alternate signaling frames. In the next time slot after bit 8 of each channel pcm word in signaling frames, a pulse in the BS signal tells the decoder to ignore bit 8 and decode bits 1-7.

If the signal on the $\overline{PDN}$/BS pin is a low level for more than seven frames, the µPD9602AD goes into the power-down mode.

Analog Loopback Test

Setting the $\overline{LOOP}$ pin to TTL low level establishes the analog loopback test mode in which vf receive is looped to vf transmit internally. A 0-dBm0 digital tone input at D_R should emerge as a 0-dBm0 digital tone output at D_X.

The $\overline{LOOP}$ pin, which is pulled up internally, should be left open or connected to V_{SS} when the channel is not in this test mode.

Transmit Gain

Figure 1 shows the transmit opamp connected in the noninverting mode and gives formulas for voltage gain A_V and load resistance R_L. By selecting the values of resistors R1 and R2, voltage gain can be set between 0 and 15 dB. Load resistance should be 10 kΩ to 20 kΩ, and load capacitance C_L should be less than 100 pF.

Figure 1. Transmit Gain Setting
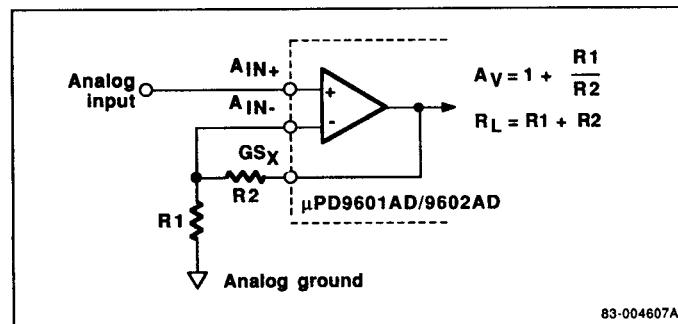
Ground

In the board layout, the AGND and DGND pins should be connected together and tied to the analog ground bus beneath the chip at the midpoint between the two pins.

Power-Up Sequence

In the power-up process, the two power pins and two ground pins should be activated in one of the five sequences listed below.

- V_{SS}, AGND, DGND, V_{DD}
- V_{SS}, AGND-DGND, V_{DD}
- V_{SS}, V_{DD}, AGND-DGND
- V_{DD}, V_{SS}, AGND-DGND
- AGND-DGND, V_{SS}, V_{DD}

Absolute Maximum Ratings

$T_A = +25°C$; $V_{DG} = V_{AG} = 0$

Parameter	Symbol	Rating	Conditions
Supply voltage	V_{DD}	−0.3 to +7.0 V	
	V_{SS}	−7.0 to +0.3 V	
Analog input voltage	V_{AIN}	V_{SS} − 0.3 to V_{DD} + 0.3 V	Pins A_{IN+}, A_{IN-}, GS_X, GS_R
Digital input voltage	V_{DIN}	−0.3 to V_{DD} + 0.3 V	
Voltage applied to digital output pin D_X	V_{DOUT}	−0.3 to V_{DD} + 0.3 V	
Power dissipation	P_T	500 mW	
Operating temperature	T_{OPT}	0 to +70°C	
Storage temperature	T_{STG}	−65 to +150°C	
Soldering temperature	T_{SOLD}	+260°C	Less than 10 seconds

Recommended Operating Conditions

$T_A = 0$ to $+70°C$; $V_{DD} = +5.0$ V ±0.25 V; $V_{SS} = -5.0$ V ±0.25 V; $V_{DG} = V_{AG} = 0$ (Note 1)

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Power						
Supply voltage	V_{DD}	+4.75	+5.00	+5.25	V	
	V_{SS}	−5.25	−5.00	−4.75	V	
Analog						
Transmit amplifier						
Input analog voltage	V_{AX}	−3.0		3.0	V	Pin A_{IN+}
Gain setting range	GR_{AX}	0		15	dB	
Load resistance	RL_{AX}	10			kΩ	Pins GS_X, A_{IN-} (Note 2)
Load capacitance	CL_{AX}			100	pF	
Receive amplifier						
Load resistance	RL_{AR}	600	160		Ω	
Load capacitance	CL_{AR}			100	pF	
Digital						
Input at digital pins						
Low voltage	V_{IL}	0		0.8	V	
High voltage	V_{IH}	2.0		V_{DD}	V	
Clock						
Data clock frequency	f_{CLK} ($1/t_{CY}$)	64		2048	kHz	
Data clock width	t_{CLK}	200			ns	
Frame synchronous clock Frequency	f_S		8.0		kHz	
High-level width	t_{WHS}	200			ns	
Low-level width	t_{WLS}	8			μs	
Frame sync clock and data clock, overlapping high-level width	t_{WHSC}	100			ns	
Clock rise time	t_R			50	ns	
Clock fall time	t_F			50	ns	
Synchronous timing margin	t_{CSD1}			100	ns	
	t_{CSD2}	40			ns	
D_R setup time	t_{DSR}	65			ns	Note 3
D_R hold time	t_{DHR}	120			ns	
BS setup time	t_{BSR}	200			ns	
BS hold time	t_{BHR}	200			ns	

Notes:

(1) Pins AGND and DGND should be connected together close to the device's analog ground pin.

(2) Pins GS_X and A_{IN-} should be connected together if the input gain is 0 dB.

(3) The rise/fall time of the digital input and clock signals used in timing tests is about 5 ns.

DC Characteristics

$T_A = 0$ to $+70\,°C$; $V_{DD} = +5.0$ V ±0.25 V; $V_{SS} = -5.0$ V ±0.25 V; $V_{DG} = V_{AG} = 0$;
$f_{CLKR} = f_{CLKX} = 2048$ kHz
All outputs are unloaded unless otherwise specified.

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Power						
Normal operating current	I_{DD}		5.0	10.0	mA	
	$|I_{SS}|$		5.0	10.0	mA	
Power-down current	I_{DDPD1}			1.0	mA	100 ms after $\overline{PDN}$ is set to low
	$|I_{SSPD1}|$			0.2	mA	
Standby current	$|I_{DDPD2}|$			1.0	mA	100 ms after FS_X and FS_R are set to low
	$|I_{SSPD2}|$			0.2	mA	
Digital Interface						
Digital input current	I_{ID}	-10		10	μA	Pins $\overline{PDN}$/BS, D_R, CLK_X, CLK_R; $V_{DIN} = 0$ to V_{DD}
Pullup current	I_{IL}	-100	-4	-0.5	μA	Pins FS_X, FS_R, $\overline{LOOP}$; $V_{DIN} = 0$ V
Digital output leakage current	I_L	-10		10	μA	Pin D_X; $V_{DIN} = 0$ to V_{DD}
Output low voltage	V_{OL}			0.4	V	Pin D_X; $R_L = 500\,\Omega$; $I_{OL} = 0.8$ mA
Output high voltage	V_{OH}	$V_{DD} - 0.3$			V	Pin D_X; $I_{OH} \leq 150\,μA$
Digital output capacitance	C_{OD}			15	pF	$f = 1$ MHz
Digital input capacitance	C_{ID}			10	pF	
Transmit Amplifier						
Input leakage current	I_B	-10	0	10	μA	Pins A_{IN+}, A_{IN-}; $V_{AIN} = -3.0$ to 3.0 V
Input resistance	R_{IN}	50			kΩ	$f = 1$ MHz
Input offset voltage	V_{IO}	-500		500	mV	Pin A_{IN+}
Output offset voltage	V_{OG}	-50		50	mV	Pin GS_X; $R_L = 10$ kΩ
Maximum output voltage	V_{OM}	-3.0		3.0	V	
Input capacitance	C_{AIN}			10	pF	
Receive Power Amplifier						
Output offset voltage	V_{OA}	-50		50	mV	Pin A_{OUT}; $D_R = +0$ code
Maximum output voltage	V_{OM}	-2.5		2.5	V	$R_L \geq 600\,\Omega$
Output resistance	R_{ORR}		1		Ω	

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{DD} = +5.0$ V ±0.25 V; $V_{SS} = -5.0$ V ±0.25 V; $V_{DG} = V_{AG} = 0$;
$f_{CLKR} = f_{CLKX} = 2048$ kHz; $R_L = 500$ Ω; $C_L = 165$ pF; $I_{OL} = 0.8$ mA; $I_{OH} \leq 150$ µA

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data enable time 1	t_{DZX1}			170	ns	Pin D_X; from FS_X to D_X
Data enable time 2	t_{DZX2}			170	ns	Pin D_X; from CLK_X to D_X
Data delay time	t_{DDX}			180	ns	Pin D_X
Data hold time	t_{HZX}		50		ns	Pin D_X

Transmission Characteristics, µPD9601AD

$T_A = +25°C$; $V_{DD} = +5.0$ V ±0.25 V; $V_{SS} = -5.0$ V ±0.25 V; $V_{DG} = V_{AG} = 0$
Analog input signal level $V_{IN} = 0$ dBm0 (f = 820 Hz); analog input gain = 0 dB; digital input signal level = 0 dBm0 (f = 820 Hz)

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Zero Transmission Level Point						
Transmit	$OTLP_X$		+4.02		dBm	
Receive	$OTLP_R$		+4.02		dBm	
Gain						
Transmit gain tolerance	G_X	−0.1		+0.1	dB	Referenced to $OTLP_X$; $V_{DD} = +5$ V; $V_{SS} = -5$ V
Receive gain tolerance	G_R	−0.1		+0.1	dB	Referenced to $OTLP_R$; $V_{DD} = +5$ V; $V_{SS} = -5$ V
G_X variation with temperature and power supply	ΔG_X	−0.2		+0.2	dB	$T_A = 0$ to $+70°C$
G_R variation with temperature and power supply	ΔG_R	−0.2		+0.2	dB	
Gain Tracking Variation of gain with input level						
Transmit gain tracking CCITT G.714, Method 2	GT_X	−0.2		+0.2	dB	+3 to −40 dBm0
		−0.4		+0.4	dB	−40 to −50 dBm0
		−0.8		+0.8	dB	−50 to −55 dBm0
CCITT G.714, Method 1	GT_X		0.0		dB	−10 to −40 dBm0
			0.0		dB	−40 to −50 dBm0
			0.0		dB	−50 to −55 dBm0

D_X Output Measurement
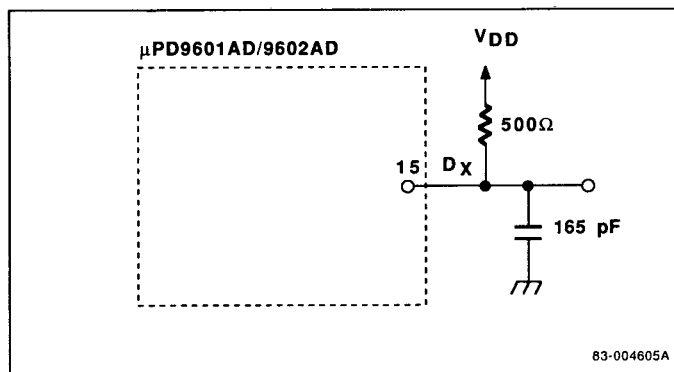
83-004605A

6

Transmission Characteristics, μPD9601AD (cont)

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Gain Tracking (cont)						
Receive gain tracking CCITT G. 714, Method 2	GT_R	−0.2		+0.2	dB	+3 to −40 dBm0
		−0.4		+0.4	dB	−40 to −50 dBm0
		−0.8		+0.8	dB	−50 to −55 dBm0
CCITT G.714, Method 1	GT_R		0.0		dB	−10 to −40 dBm0
			0.0		dB	−40 to −50 dBm0
			0.0		dB	−50 to −55 dBm0
Frequency Response Gain relative to gain at 820 Hz						
Transmit section	G_{RX1}			−24	dB	60 Hz
	G_{RX2}	−2.0		0	dB	200 Hz
	G_{RX3}	−0.15		+0.15	dB	0.3 to 3.0 kHz
	G_{RX4}	−0.65		+0.15	dB	3.2 kHz
	G_{RX5}	−0.8		0	dB	3.4 kHz
	G_{RX6}			−6.5	dB	3.78 kHz
Receive section	G_{RR1}	−0.15		+0.15	dB	0 to 3.0 kHz
	G_{RR2}	−0.65		+0.15	dB	3.2 kHz
	G_{RR3}	−0.8		0	dB	3.4 kHz
	G_{RR4}			−6.5	dB	3.78 kHz
Noise						
Transmit section	N_{XP}			−80	dBm0p	A_{IN+} is grounded to AGND; input amplifier gain = 0 dB
Receive section	N_{RP}			−80	dBm0p	D_R = +0 code
Single-frequency noise	N_{SF}			−50	dBm0	End-to-end testing; CCITT G.712 4.2
Crosstalk, transmit to receive	CT_{TR}			−65	dB	A_{IN+} = 0 dBm0, 820 Hz; D_R = lowest positive decode level
Crosstalk, receive to transmit	CT_{RT}			−65	dB	A_{IN+} is grounded to AGND; D_R = 0-dBm0, 820-Hz digital input
Power supply rejection f = 0.3 to 3 kHZ	$PSRR_1$	30			dB	±100-mV zero-to-peak signal on V_{DD} or V_{SS}
f = 3 to 4 kHz	$PSRR_2$	30			dB	
f = 4 to 50 kHz	$PSRR_3$	30			dB	

Transmission Characteristics, µPD9601AD (cont)

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Distortion						
Transmit signal-to-distortion ratio						
CCITT G.714, Method 2	SD_X	36			dB	0 to −30 dBm0
		31			dB	−30 to −40 dBm0
		26			dB	−40 to −45 dBm0
CCITT G.714, Method 1	SD_X		37		dB	−6 to −27 dBm0
			35		dB	−27 to −34 dBm0
			30		dB	−34 to −40 dBm0
			15		dB	−40 to −55 dBm0
Receive signal-to-distortion ratio						
CCITT G.714, Method 2	SD_R	36			dB	0 to −30 dBm0
		31			dB	−30 to −40 dBm0
		26			dB	−40 to −45 dBm0
CCITT G.714, Method 1	SD_R		37		dB	−6 to −27 dBm0
			35		dB	−27 to −34 dBm0
			30		dB	−34 to −40 dBm0
			15		dB	−40 to −55 dBm0
Intermodulation distortion, end-to-end						
CCITT G.712 (7.1)	IMD_1			−38	dB	
CCITT G.712 (7.2)	IMD_2			−52	dBm0	
Absolute delay, A_{IN} to A_{OUT}	D_A			480	µs	
Group delay, A_{IN} to A_{OUT}	D_0			1.40	ms	500 Hz
				0.70	ms	600 Hz
				0.20	ms	1000 Hz
				0.20	ms	2600 Hz
				1.40	ms	2800 Hz

Transmission Characteristics, µPD9602AD

$T_A = +25°C$; $V_{DD} = +5.0$ V ± 0.25 V; $V_{SS} = -5.0$ V ± 0.25 V; $V_{DG} = V_{AG} = 0$;
Analog input signal level $V_{IN} = 0$ dBm0 (f = 1020 Hz); analog input gain = 0 dB; digital input signal level = 0 dBm0 (f = 1020 Hz)

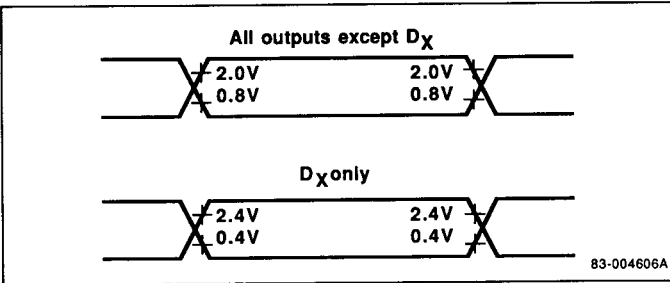| Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Zero Transmission Level Point						
Transmit	0TLP$_X$		+3.99		dBm	
Receive	0TLP$_R$		+3.99		dBm	
Gain						
Transmit gain tolerance	G$_X$	−0.1		+0.1	dB	Referenced to 0TLP$_X$; $V_{DD} = +5$ V; $V_{SS} = -5$ V
Receive gain tolerance	G$_R$	−0.1		+0.1	dB	Referenced to 0TLP$_R$; $V_{DD} = +5$ V; $V_{SS} = -5$ V
G$_X$ variation with temperature and power supply	ΔG$_X$	−0.2		+0.2	dB	$T_A = 0$ to $+70°C$
G$_R$ variation with temperature and power supply	ΔG$_R$	−0.2		+0.2	dB	
Gain Tracking Variation of gain with input level						
Transmit gain tracking	GT$_X$	−0.2		+0.2	dB	+3 to −40 dBm0
		−0.4		+0.4	dB	−40 to −50 dBm0
		−0.8		+0.8	dB	−50 to −55 dBm0
Receive gain tracking	GT$_R$	−0.2		+0.2	dB	+3 to −40 dBm0
		−0.4		+0.4	dB	−40 to −50 dBm0
		−0.8		+0.8	dB	−50 to −55 dBm0
Frequency Response Gain relative to gain at 1020 Hz						
Transmit section	G$_{RX1}$			−24	dB	60 Hz
	G$_{RX2}$	−2.0		0	dB	200 Hz
	G$_{RX3}$	−0.15		+0.15	dB	0.3 to 3.0 kHz
	G$_{RX4}$	−0.65		+0.15	dB	3.2 kHz
	G$_{RX5}$	−0.8		0	dB	3.4 kHz
	G$_{RX6}$			−6.5	dB	3.78 kHz
Receive section	G$_{RR1}$	−0.15		+0.15	dB	0. to 3.0 kHz
	G$_{RR2}$	−0.65		+0.15	dB	3.2 kHz
	G$_{RR3}$	−0.8		0	dB	3.4 kHz
	G$_{RR4}$			−6.5	dB	3.78 kHz

Transmission Characteristics, μPD9602AD (cont)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Noise						
Transmit section	N_{XC}			16	dBrnc0	A_{IN+} is grounded to AGND; input amplifier gain = 0 dB
Receive section	N_{RC}			10	dBrnc0	
Single-frequency noise	N_{SF}			−50	dBm0	End-to-end testing; CCITT G.712 4.2
Crosstalk, transmit to receive	CT_{TR}			−65	dB	A_{IN+} = 0 dBm0, 1020 Hz; D_R = lowest positive decode level
Crosstalk, receive to transmit	CT_{RT}			−65	dB	A_{IN+} is grounded to AGND; D_R = 0-dBm0, 1020-Hz digital input
Power supply rejection f = 0.3 to 3 kHz	$PSRR_1$	30			dB	±100-mV zero-to-peak signal on V_{DD} or V_{SS}
f = 3 to 4 kHz	$PSRR_2$	20			dB	
f = 4 to 50 kHz	$PSRR_3$	30			dB	
Distortion						
Transmit signal-to-distortion ratio, CCITT, G.714, Method 2	SD_X	36			dB	0 to −30 dBm0
		31			dB	−30 to −40 dBm0
		26			dB	−40 to −45 dBm0
Receive signal-to-distortion ratio CCITT G.714, Method 2	SD_R	36			dB	0 to −30 dBm0
		31			dB	−30 to −40 dBm0
		26			dB	−40 to −45 dBm0
Intermodulation distortion	IMD_1			−38	dB	End-to-end measurement; CCITT G.712 (7.1)
	IMD_2			−52	dBm0	End-to-end measurement; CCITT G.712 (7.2)
Absolute delay, A_{IN} to A_{OUT}	D_A			480	μs	
Group delay, A_{IN} to A_{OUT}	D_0			1.40	ms	500 Hz
				0.70	ms	600 Hz
				0.20	ms	1000 Hz
				0.20	ms	2600 Hz
				1.40	ms	2800 Hz

Timing Waveforms

Timing Measurement Points

All outputs except D_X

2.0V · · · 2.0V
0.8V · · · 0.8V

D_X only

2.4V · · · 2.4V
0.4V · · · 0.4V

83-004606A

Transmit Timing 1

FSX

t_{WHSC}

t_{CSD1}

CLKX 1 2 8

t_{DZX1}

DX MSB 2nd 7th LSB

83-004602B

Transmit Timing 2

t_R · · · t_F

t_{WHS} t_{WLS}

FSX

t_{CSD2}

t_{CY} · · · t_{CLK}

t_{WHSC} · · · t_R · · · t_F

CLKX 1 2 8

t_{CLK}

t_{DZX2} · · · t_{DDX} · · · t_{HZX}

DX MSB 2nd 7th LSB

83-004601B
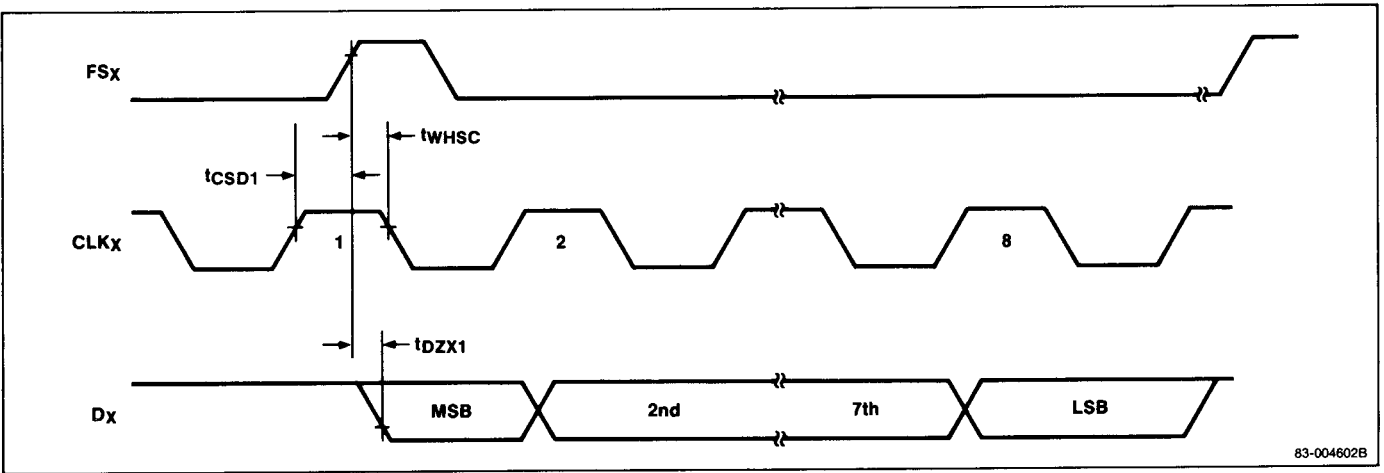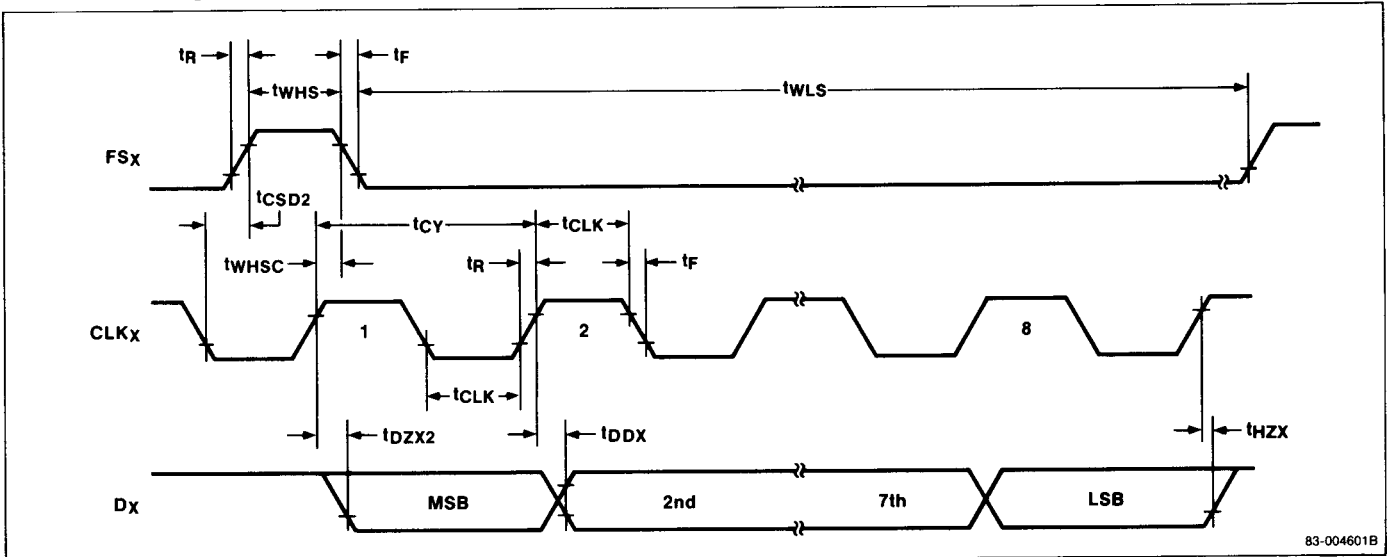
Timing Waveforms (cont)

Receive Timing 1

Note: X = don't care

83-004603B

Receive Timing 2

83-004604B
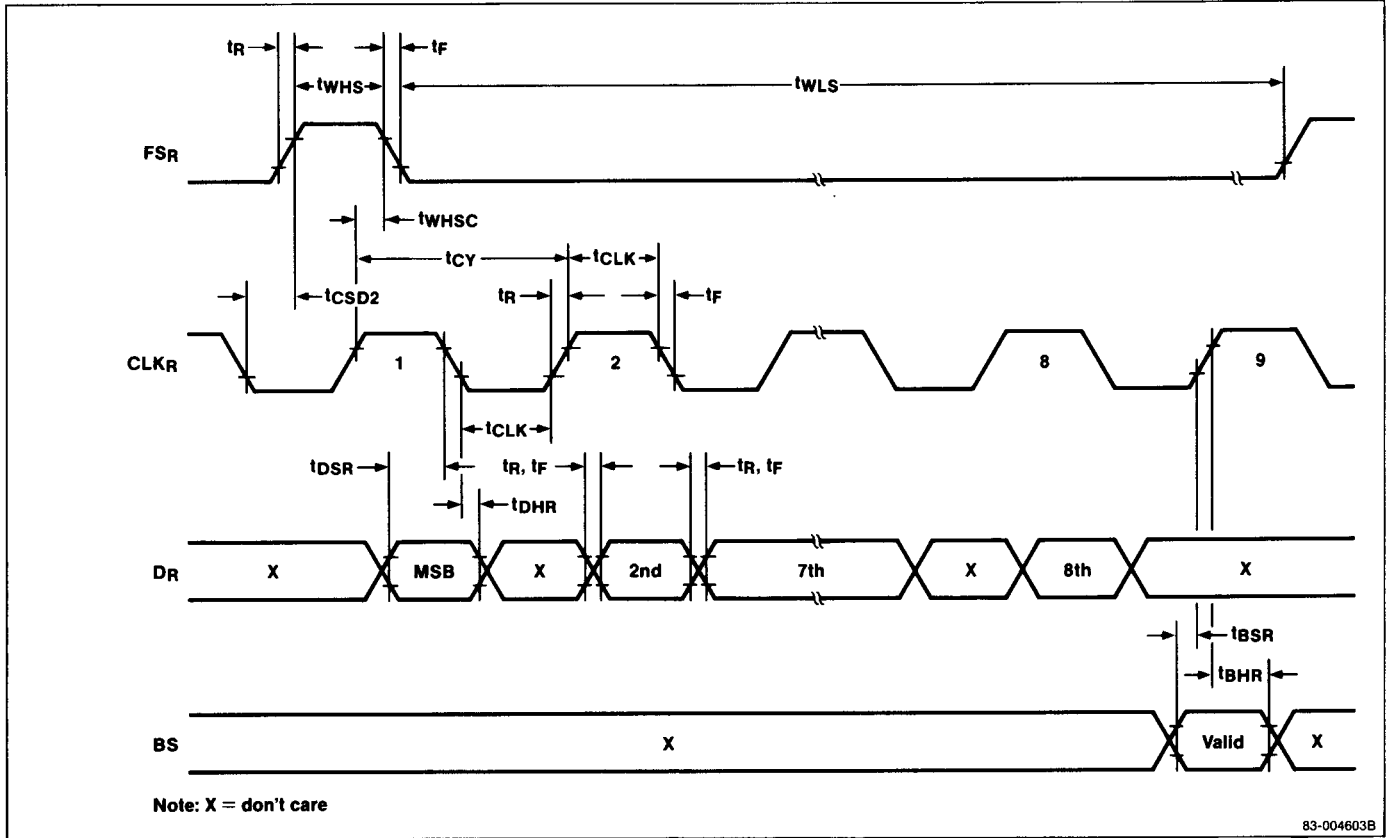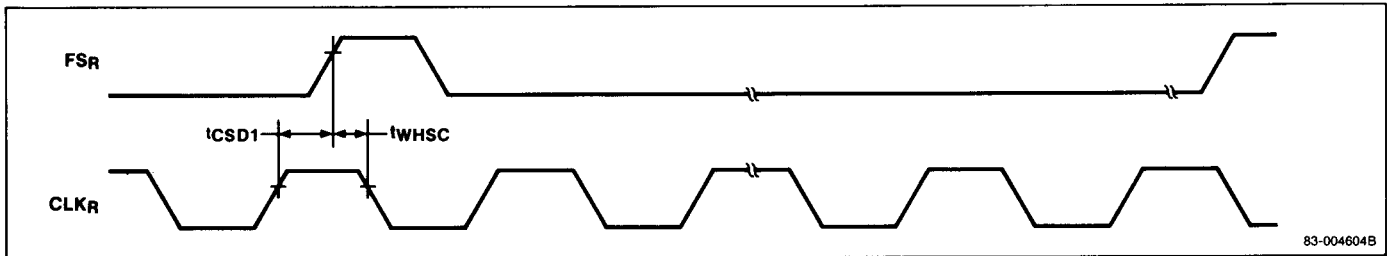
Package Drawing

16-Pin Ceramic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.46 ±0.05	.018 ±.002
E	1.42 min	.056 min
F	3.5 ±0.3	.138 ±.012
G	0.51 min	.020 min
H	3.80	.150
I	5.08 max	.200 max
J	7.32	.288
K	7.62 [TP]	.300 [TP]
L	0.25 ±0.05	.010 ±.002
M	0.89 min	.035 min

Notes:

[1] Each lead centerline is located within 0.25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.
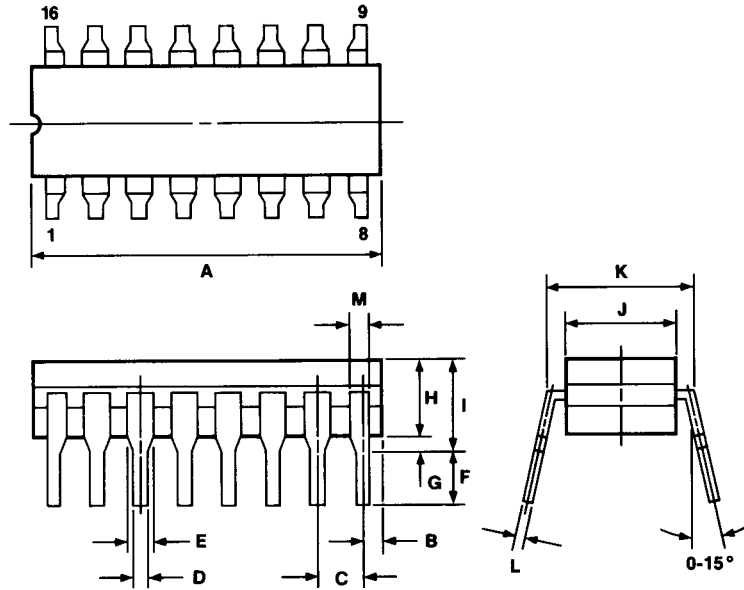
83-004657B
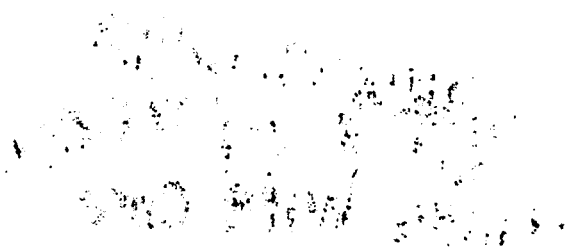
μPD9601AD/9602AD

NEC

NEC Electronics Inc.

For Literature Call Toll Free: 1-800-632-3531
1-800-632-3532 (In California)

NECEL-001035
STOCK NO. 220208

008639