MB86951

CMOS ETHERNET ENCODER/DECODER

FUJITSU

DATA SHEET

APRIL1993

FEATURES

- 10 Mbit/sec Manchester encoder/decoder
- Compatible with IEEE 802.3 10BASE2, 10BASE5 and 10BASE-T specifications
- Receiver clock recovery with dual phase locked loop for high stability
- Decodes Manchester data with up to ±20 ns of jitter.
- Loopback capability for diagnostics
- TTL compatible host interface
- Interfaces directly to the AUI (transceiver) cable
- High speed CMOS technology with a single 5 V supply
- Low power consumption, typically 16 mA
- Power Down Mode: I_{CC} = 5 mA typ
- Available in 24-pin plastic DIP and SOP packages

GENERAL DESCRIPTION

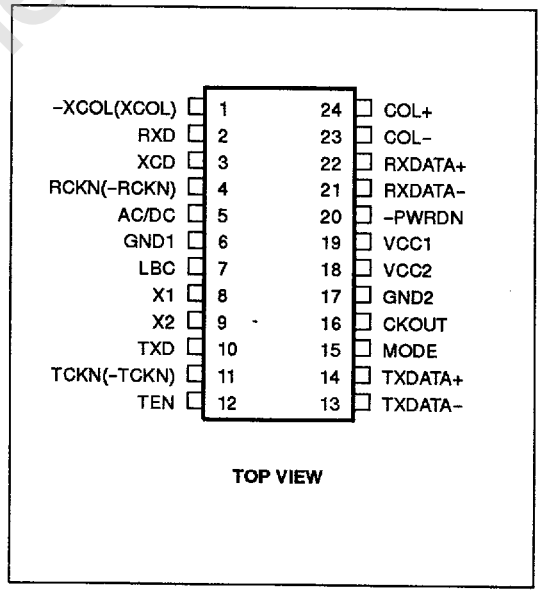
The MB86951 is a 10 Mbit/sec Manchester encoder/decoder that is designed to meet the requirements for Ethernet local area networks. This device, when used with companion chips such as Fujitsu's MB86950 EtherStar™ Controller and either the MBL8392A Coaxial Transceiver or the MB86962 Twisted Pair Transceiver (see Figure 1), forms a complete chip set that meets the requirements of the ISO/ANSI/IEEE 8802-3 international standard for Ethernet, Thin Net, and 10BASE-T networks.

The encoder/decoder interfaces with the network controller on the system side and with the transceiver on the network side. It contains a receiver with phase locked loop, a driver, a collision signaling detector, and an oscillator.

During transmit operation, the MB86951 receives NRZ (non-return-to-zero) data from the controller and converts the serial binary data stream into a Manchester encoded stream which is transmitted out on a balanced differential pair to the transceiver. During receive operation it converts Manchester encoded data on a balanced differential pair from the transceiver into NRZ data and forwards it to the controller, together with a 10 MHz synchronous receive data clock. A phase locked loop is used for clock recovery to allow a worst case jitter of ±20 ns.

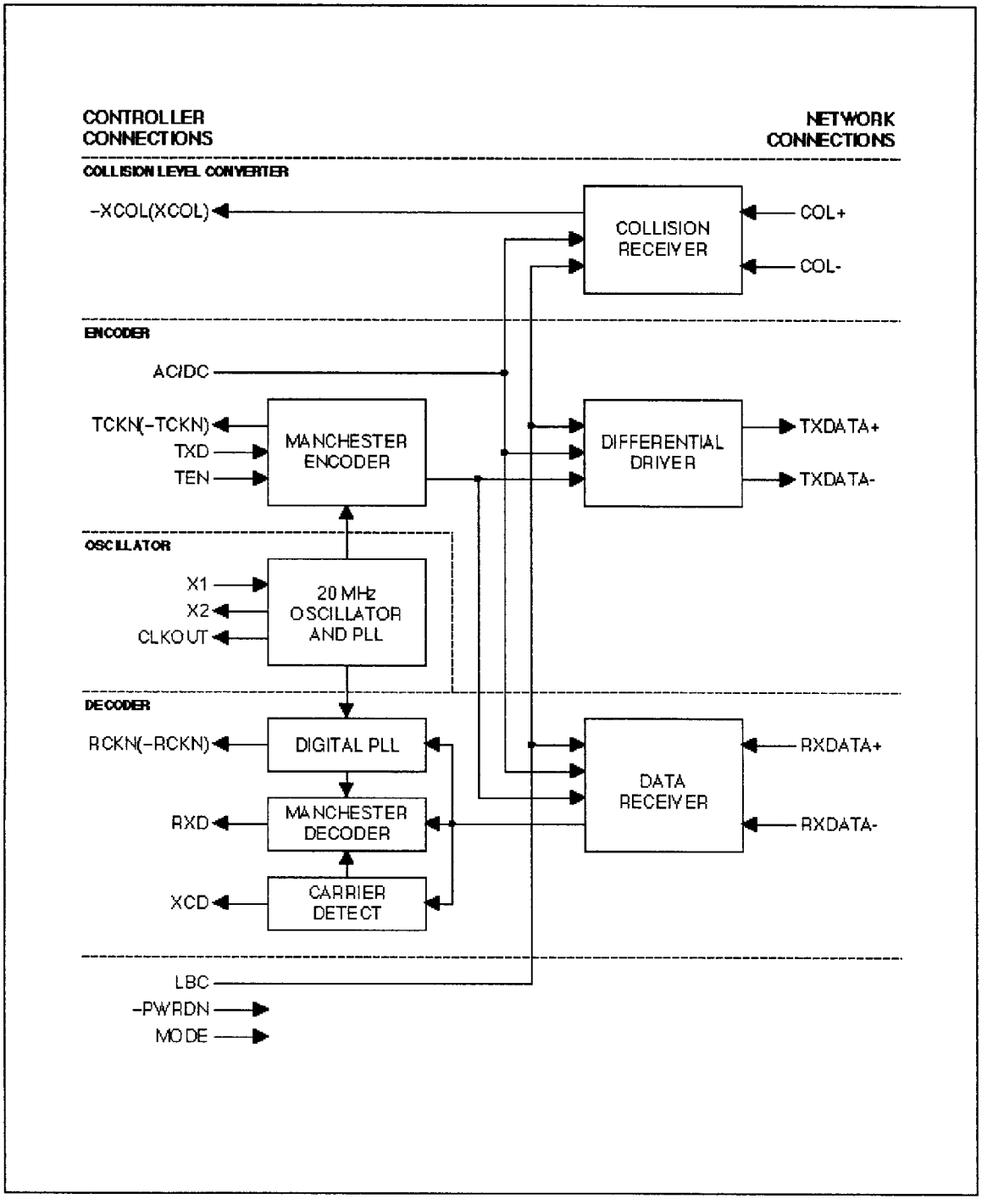
The MB86951 is fabricated using Fujitsu's high speed, low power, CMOS technology and is supplied in 24-pin plastic DIP and small outline (SOP) packages.

PIN CONFIGURATION



TOP VIEW

BLOCK DIAGRAM



ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V_{CC} = +5 V ± 5%, T_A = 0 to +70°C
24-Pin Plastic Dual In-line	DIP-24P-M03	MB86951P-G
24-Pin Plastic Small Outline	FPT-24P-M02	MB86951PF-G

SIGNAL DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
-XCOL(XCOL)	O	**COLLISION PRESENCE:** This output indicates that the collision inputs to the MB86951 (COL±) are active, signifying that the transceiver has detected a collision on the media. If MODE = 0, -XCOL(XCOL) is a normally low output which changes to a high state during collision detection. If MODE = 1, -XCOL(XCOL) is a normally high output which changes to a 10 MHz pulse stream during collision detection. See also Mode Control section.
RXD	O	**RECEIVED SERIAL DATA:** Output NRZ serial bit stream from the Manchester decoder. Changes in the state of RXD are synchronous with the rising edge of RCKN if MODE = 0, and synchronous with the falling edge of RCKN if MODE = 1.
XCD	O	**RECEIVED CARRIER DETECT**: Assertion of this active high output indicates that a carrier has been detected at the RXDATA± inputs.
RCKN(-RCKN)	O	**RECEIVED DATA CLOCK:** The data clock recovered by the DPLL within the MB86951 while data is being received. RCKN(-RCKN) is a free running 10 MHz clock when the receive inputs are idle. See also Mode Control and Data Decoder sections.
AC/DC	I	**AC/DC COUPLING SELECT:** AC/DC = 0 selects DC coupling, AC/DC = 1 selects AC coupling for the TXDATA± outputs. When AC coupling is selected, both TXDATA+ and TXDATA- are driven to the same output voltage level during transmit idle periods to prevent saturation of the isolation transformer.
LBC	I	**LOOPBACK CONTROL:** When this input is asserted (high) the MB86951 is placed in the loopback mode.
X1	I	**CRYSTAL INPUT:** Connection for one side of the 20 MHz crystal or input for an external 20 MHz clock.
X2	O	**CRYSTAL OUTPUT:** Connection for the other side of the 20 MHz crystal. Leave unconnected if an external clock is used.
TXD	I	**TRANSMIT SERIAL DATA INPUT:** NRZ serial data stream which is fed to the Manchester encoder. Changes in TXD should be synchronized to the rising edge of TCKN(-TCKN) if MODE = 0 and to the falling edge of TCKN(-TCKN) if MODE = 1.
TCKN(-TCKN)	O	**TRANSMIT DATA CLOCK:** 10 MHz clock output used by the controller to synchronize the TXD input to the MB86951. See also Mode Control and Data Encoder sections.
TEN	I	**TRANSMIT ENABLE:** When asserted (high) TEN enables encoding of the transmitted data.
TXDATA+ TXDATA-	O	**TRANSMIT DATA:** These are the Manchester encoded differential outputs to the transceiver. They require 270Ω pulldown resistors and are capable of driving a 78Ω differential transmission line.
MODE	I	**MODE:** MODE = 1 selects the normal (Fujitsu- controller compatible) mode. When MODE = 0, the part is functionally and electrically compatible with the National DP83910 and AMD Am7992B. See also Mode Control section.
CKOUT	O	**CLOCK OUTPUT:** 20 MHz free running clock output.

Note: Signal names preceded by a minus sign (-) indicate an active low state. Dual function pins have two names with the second enclosed in parentheses ( ).
Signal names preceded by a minus sign (-) indicate an active low state. Dual function pins have two names separated by a slash (/).

SIGNAL DESCRIPTIONS (continued)

SYMBOL	TYPE	DESCRIPTION
-PWRDN	I	**POWER DOWN:** Active low input for selecting power down mode. Note: LBC (pin 7) must be 0 during power down, otherwise the device will enter a test mode used by the factory. Tie -PWRDN high for normal operation.
RXDATA+ RXDATA-	I	**RECEIVED DATA:** These are the Manchester encoded differential inputs to the MB86951 from the transceiver.
COL+ COL-	I	**COLLISION:** These differential inputs are driven with a 10 MHz signal when the transceiver detects a collision on the medium.
V_{CC}		**POWER SUPPLY:** A nominal +5 V_{DC} supply is required.
GND		GROUND

Note: Signal names preceded by a minus sign (-) indicate an active low state. Dual function pins have two names with the second enclosed in parentheses ( ).

FUNCTIONAL DESCRIPTION

The block diagram highlights the major functional blocks of the MB86951: oscillator, data encoder, data decoder, collision signal detector, and loopback control. Figure 1 illustrates a typical interface for the device when driving an AUI (transceiver) cable on the network side and connected to Fujitsu's MB86950 EtherStar controller on the system side.

OSCILLATOR

The IEEE 802.3 standard specifies a clock rate of 10 Mbits/sec. This is obtained from a 20 MHz clock generated by the oscillator, which operates from an external crystal reference connected between pins X1 and X2 of the MB86951. Crystal capacitance as specified by the manufacturer should be connected from X1 and X2 to ground, considering any stray capacitance which can vary the crystal's frequency. If an external 20 MHz clock is available, it may be applied to X1 with X2 left unconnected.

The 20 MHz oscillator output is provided on CKOUT for external use. It is also divided by two to produce the required 10 MHz clock, which is used internally and furnished on TCKN(-TCKN) for use by the network controller. The 20 MHz clock also serves as a reference for an internal phase locked loop used for clock and data recovery in the decoder section.

DATA ENCODER

Manchester encoding is used for the transmission of data from the MB86951. Manchester encoding is a binary signaling mechanism that combines data and clock into bit symbols. Each bit symbol is split into two halves, with the signal polarity of the second half being the inverse of that of the first half. A transition always occurs in the middle of each bit symbol, with logic '0' and '1' encoded as 1-to-0 and 0-to-1 transitions respectively. See Figure 2. In the case of the MB86951, the controller asserts

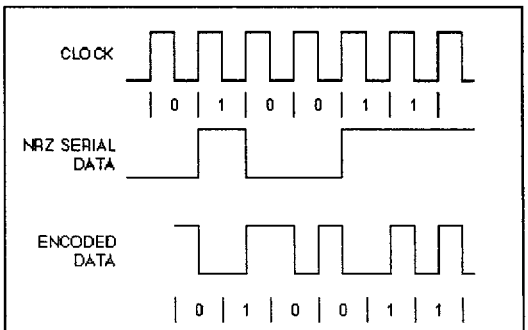


Figure 2. Manchester Encoding

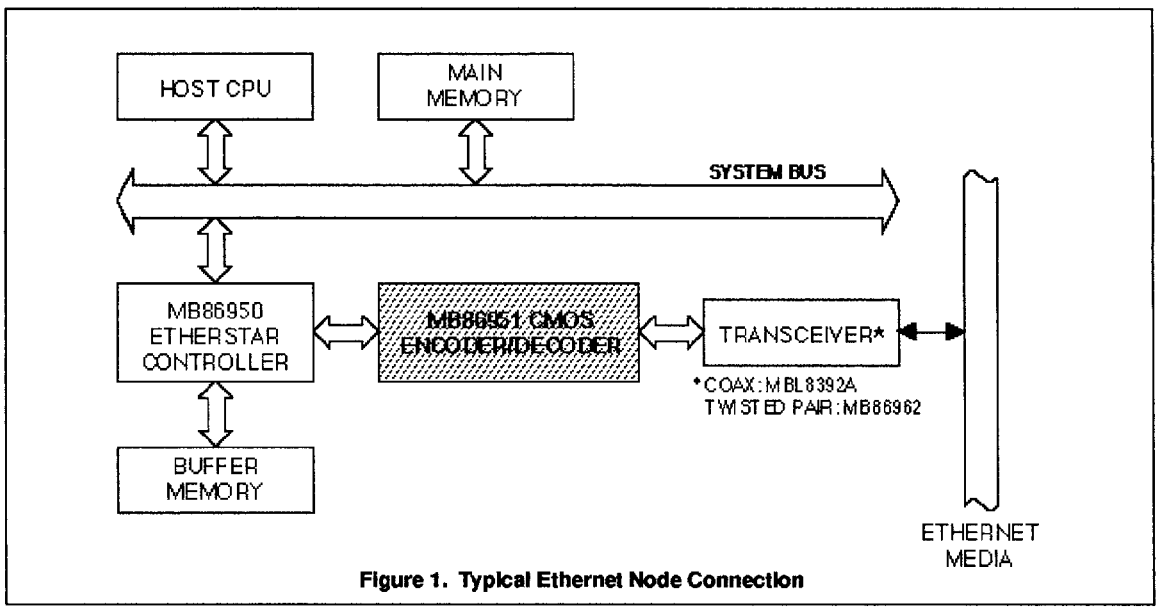


Figure 1. Typical Ethernet Node Connection

transmit enable (TEN) to indicate that the outgoing packet on TXD is valid data. This NRZ serial data input must be supplied synchronously with the TCKN(-TCKN) clock as required by the setting of MODE. If MODE=1, TXD is valid during the rising edge of TCKN(-TCKN); if MODE=0, TXD is valid during the falling edge. The Manchester-encoded signals are output through a differential driver to the transceiver through TXDATA+ and TXDATA-, and are present as long as the TEN pin remains affirmed.

The differential driver is capable of driving a 50 meter segment of 78Ω interface cable, as specified in the ISO/ANSI/IEEE 8802-3 standard. 270Ω resistors are required externally to pull down TXDATA+ and TXDATA-. See Figure 3.

DATA DECODER

The data decoder section performs three functions on the data received at the differential receive inputs (RXDATA+ and RXDATA-) from the transceiver: carrier detection, clock recovery, and Manchester data decoding.

Clock recovery is accomplished by use of phase locked loop circuitry which uses the crystal oscillator as a reference. Use of a PLL provides the most reliable and robust clock recovery. It allows signal acquisition to be accomplished within six bit times from first detection of the signal, and permits stable operation with input signal jitter of up to ±20 ns. Carrier detection is indicated to the controller by affirmation of the XCD output, which occurs shortly after a signal appears at the differential inputs.

The recovered clock is supplied to the controller on RCKN(-RCKN), and is also used to convert the Manchester encoded data to NRZ format, which is then output on RXD. The phase relationship between RCKN(-RCKN) and RXD is controlled by the MODE input. Transitions in the state of RXD are synchronous with the rising edge of RCKN(-RCKN) if MODE = 0, and synchronous with the falling edge of RCKN(-RCKN) if MODE = 1. RCKN(-RCKN) is a free running 10 MHz clock when no receive signal is present.

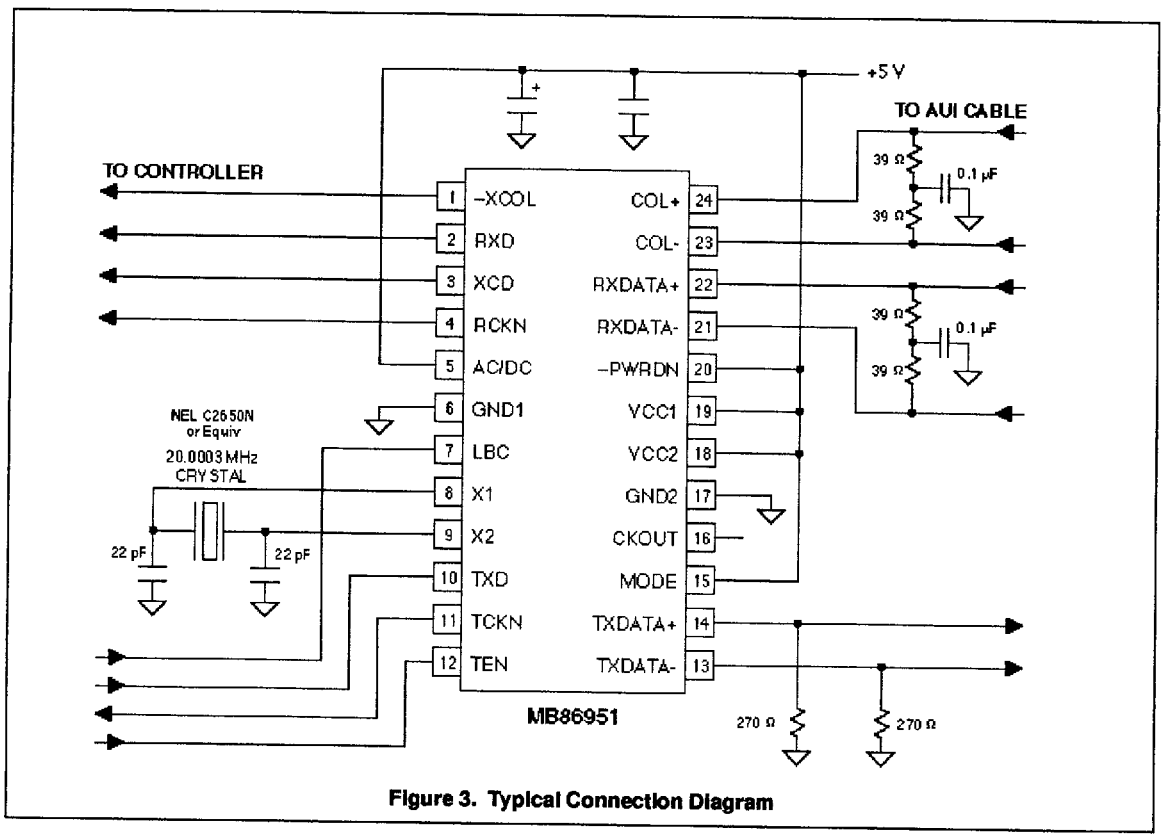


Figure 3. Typical Connection Diagram

The RXDATA+ and RXDATA- differential inputs must be terminated with two 39Ω resistors in series with a 0.1 μF bypass capacitor at their junction, as illustrated in Figure 2.

COLLISION SIGNALING DETECTOR

As collisions are detected on the network media, the transceiver generates a 10 MHz signal on the COL+ and COL- differential inputs to the MB86951. This signal is detected by the MB86951, converted to a logic-level signal appropriate for the controller and output on -XCOL(XCOL). If MODE = 0, -XCOL(XCOL) is normally low and changes to a high state during collision detection. If MODE = 1, -XCOL(XCOL) is normally high and changes to a 10 MHz pulse stream during collision detection.

The COL+ and COL- differential inputs require 78Ω Ω termination like that for the RXDATA+ and RXDATA- inputs. See Figure 2.

LOOPBACK

The loopback control input (LBC) causes transmitted data from the controller to be routed through the internal circuits of the MB86951 and back to the received data output to test for proper system operation. While LBC is affirmed, the encoded transmit data is supplied to the data decoder instead of the receive data from the RXDATA+ and RXDATA- inputs. Also, the differential transmit drivers and the collision signal detector are disabled. Note that changes in LBC while data is being received may cause errors in the received data output.

MODE CONTROL

The MODE input selects one of two modes of operation for the MB86951. The setting of this input changes the phase relationship between certain clocks and signals, and the format of the -XCOL(XCOL) output. The three signal pins which are affected are -XCOL(XCOL), RCKN(-RCKN) and TCKN(-TCKN). MODE =1 selects the normal mode in which these signals are compatible with Fujitsu controllers such as the MB86950. When MODE = 0 the MB86951 is functionally and electrically compatible with the National DP83910 and the AMD Am7992. Polarity of the three signal pins shown in their names in parentheses corresponds to MODE = 0. See the Pin Descriptions section and the timing diagrams at the end of this data sheet for additional information.

POWER DOWN

The power down mode is selected by driving both -PWRDN (pin 20), and LBC (pin 7) low. In this mode, power consumption is reduced to 6 mA typical.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1,2,3]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.5	6.0	V
V_{ITL}	TTL level input voltage		-0.5	V_{CC} + 0.5	V
I_{ODF}	Differential output current			-40	mA
T_{STG}	Storage temperature		-40	125	°C
T_{OP}	Operating temperature		-25	85	°C
V_{DCI}	RxDATA± / COL± DC input voltage		0.5	16	V
V_{DCO}	TxDATA± / COL± DC output voltage	with transformer without transformer	-0.5 -0.5	16 10	V V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Units
T_A	Operating ambient temperature	0 to +70	°C
V_{CC}	Supply voltage	5.0 ± 5%	V
I_{OH}	Maximum TTL high level output current	-2.0	mA
I_{OL}	Maximum TTL low level output current	3.2	mA
R_L	Driver load resistor (see Figure 4)	270	Ω
R_T	Differential termination resistor (see Figure 4)	78	Ω
C_{OSC}	Oscillator capacitors [5]	22	pF
f_{XTAL}	Oscillator crystal frequency	20.000 ± 0.005%	MHz

DC SPECIFICATIONS[3,4] (Recommended Operating Conditions Unless Otherwise Indicated)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Operating power supply current	no output load	—	30	60	mA
I_{CCPD}	Power down supply current	no output load -PWRDN=0 , LBC=0	—	6	10	mA
V_{IH}	TTL high level voltage		2.2	—	V_{CC}	V
V_{IL}	TTL low level input voltage		0	—	0.8	V
V_{OH}	TTL high level output voltage	I_{OH} = -2.0 mA	4.2	—	V_{CC}	V
V_{OL}	TTL low level output voltage	I_{OL} = 3.2 mA	0	—	0.4	V
I_{LI}	TTL input leakage current	V_{IN} = 0 or V_{CC}	-10	—	10	µA
V_{OP}	TxDATA± peak output voltage	R_L = 270Ω Ω	±0.5	—	±1.3	V
V_{OB}	TxDATA± output voltage imbalance	R_T = 78Ω Ω	—	—	±40	mV
V_{CMO}	TxDATA± DC common mode output		2.4	3.4	4.4	V
V_{IT1}, V_{IT2}	RxDATA± squelch threshold	AC/DC=0 AC/DC=1	-80 -300	0 -220	80 -140	mV

DC SPECIFICATIONS[3,4] (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IP}	RxDATA ± peak input voltage		±0.3	—	±1.5	V
V_{IB}	RxDATA ± DC input bias voltage		2.2	3.2	4.2	V
I_{IHD}	RxDATA ± input high level current	$V_{IN} = V_{CC}$	—	—	250	µA
I_{ILD}	RxDATA ± input low level current	$V_{IN} = 0$	—	—	-400	µA
V_{ITD1}	RxDATA ± input threshold	AC/DC = Low	-80	0	80	mV
V_{ITD2}		AC/DC = High [6]	-300	-220	-140	mV
I_{CCS}	Static power supply current	-PWRDN = 0, X_1=V_{CC}, differential inputs open, TTL inputs = 0 or V_{CC}, no output loads	—	—	100	µA
I_{CC}	Operating power supply current	No output loads	—	25	50	mA

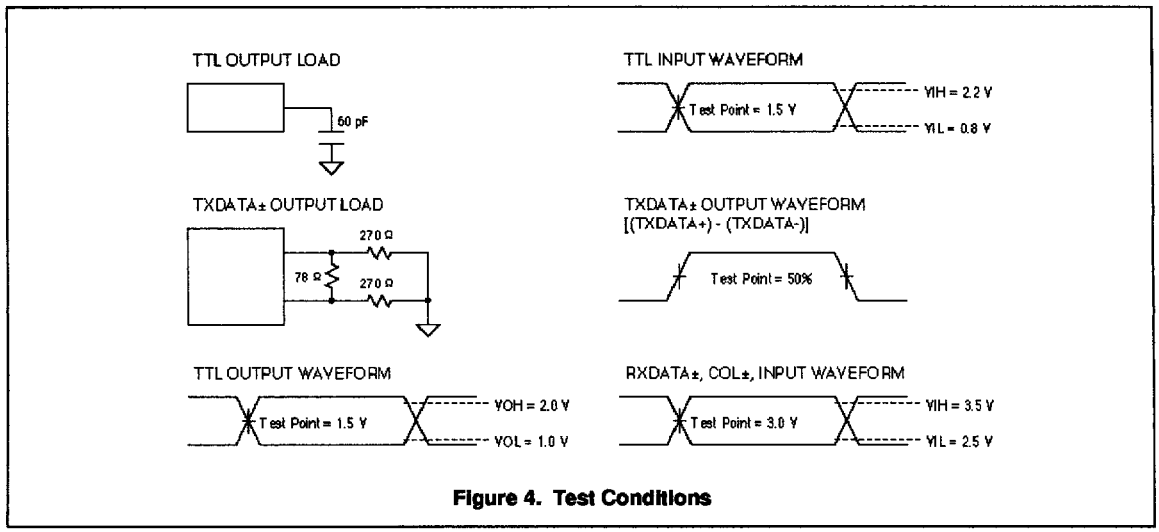


Figure 4. Test Conditions

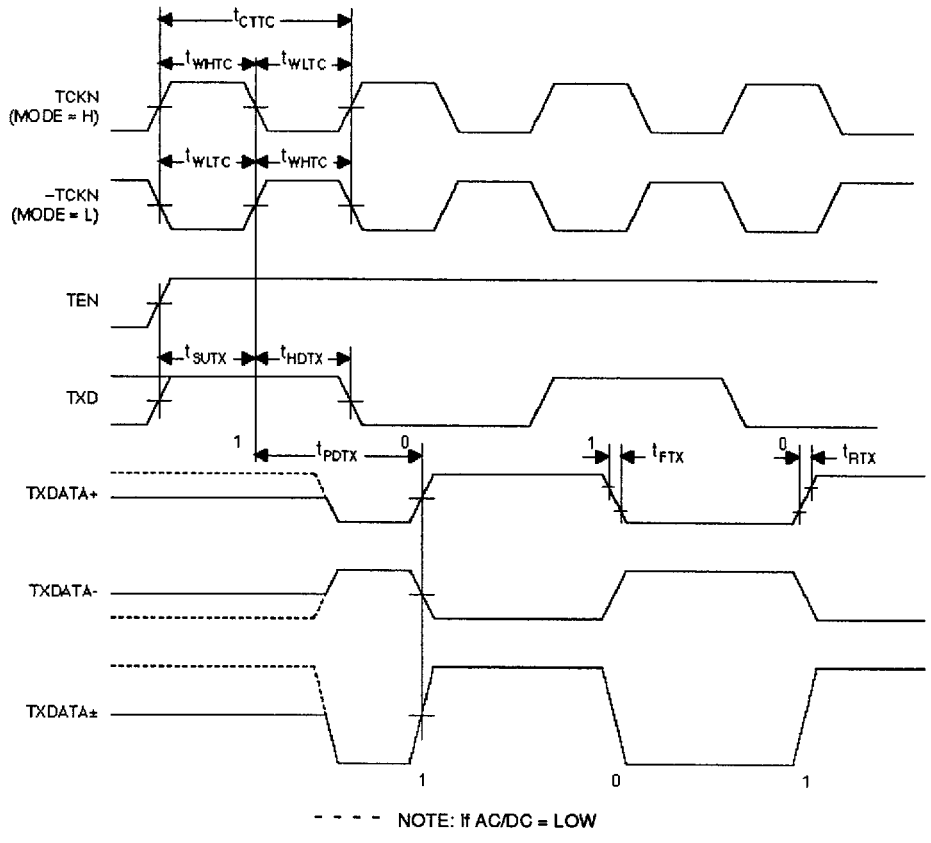


Figure 5. Transmit Start Timing

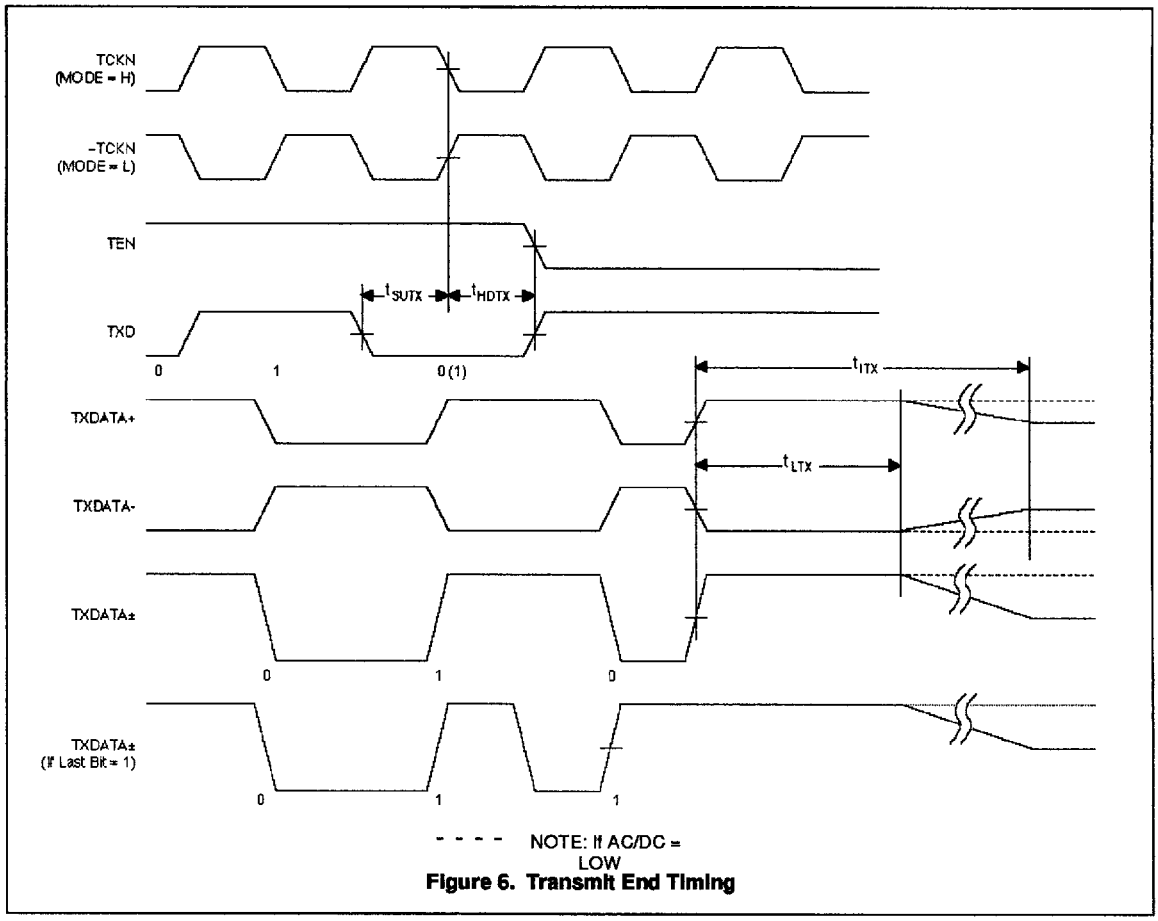


Figure 6. Transmit End Timing

AC CHARACTERISTICS[3,4] (Recommended Operating Conditions Unless Otherwise Indicated)

Transmit Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{CTTC}	5	TCKN cycle time		99.99	100	100.01	ns
t_{WLTC}	5	TCKN low time		40	50	60	ns
t_{WHTC}	5	TCKN high time		40	50	60	ns
t_{PDTX}	5	TXDATA ± encode time		—	95	—	ns
t_{RTX}	5	TXDATA ± rise time	20% to 80%	—	2	—	ns
t_{FTX}	5	TXDATA ± fall time	20% to 80%	—	2	—	ns
t_{LTX}	6	TXDATA ± level hold time	AC/DC = High	200	—	—	ns
t_{ITX}	6	TXDATA ± idling time	AC/DC = High	—	—	8000	ns
t_{SUTX}	5,6	TXD, TEN setup time to TCKN		20	—	—	ns
t_{HDTX}	5,6	TXD, TEN hold time from TCKN		10	—	—	ns

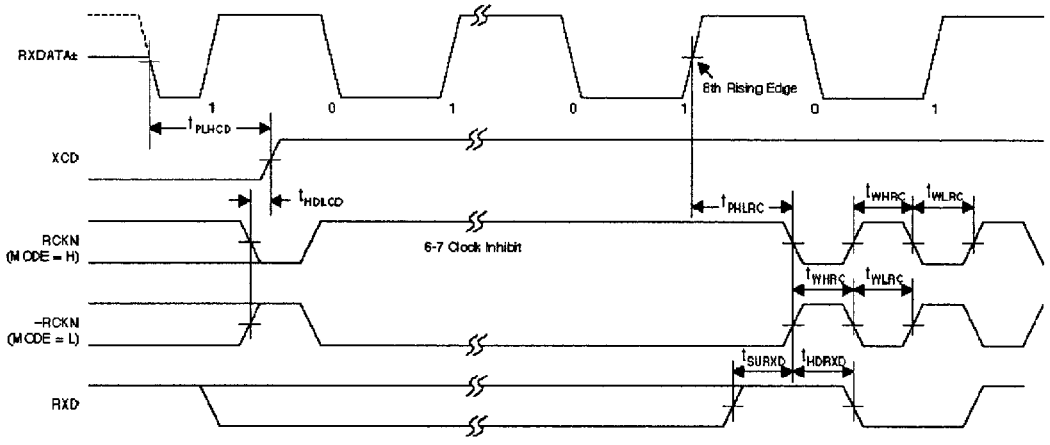


Figure 7. Receive Start Timing

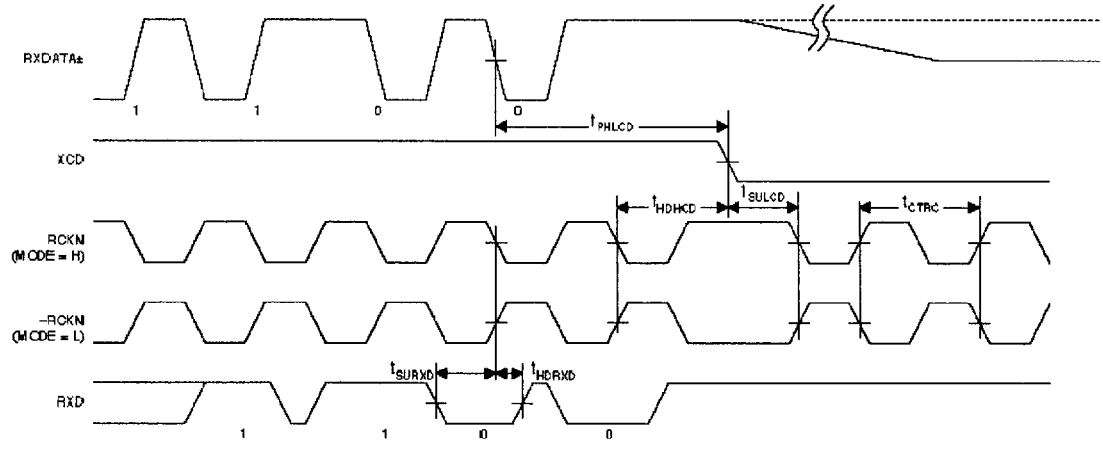


Figure 8. Receive End Timing

Receive Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{CTRC}	8	RCKN cycle time during idle		99.99	100	100.01	ns
t_{WLRC}	7	RCKN low time		35	50	—	ns
t_{WHRC}	7	RCKN high time		35	50	—	ns
t_{PHLRC}	7	RCKN delay time		—	125	—	ns
t_{PLHCD}	7	XCD on delay time		—	90	120	ns
t_{PHLCD}	8	XCD off delay time		—	260	—	ns
t_{HDLCD}	7	XCD low hold time		10	—	—	ns
t_{HDHCD}	8	XCD high hold time		—	130	—	ns
t_{SULCD}	8	XCD low setup time		—	70	—	ns
t_{SURXD}	7,8	RXD setup time to RCKN		20	60	—	ns
t_{HDRXD}	7,8	RXD hold time from RCKN		10	20	—	ns

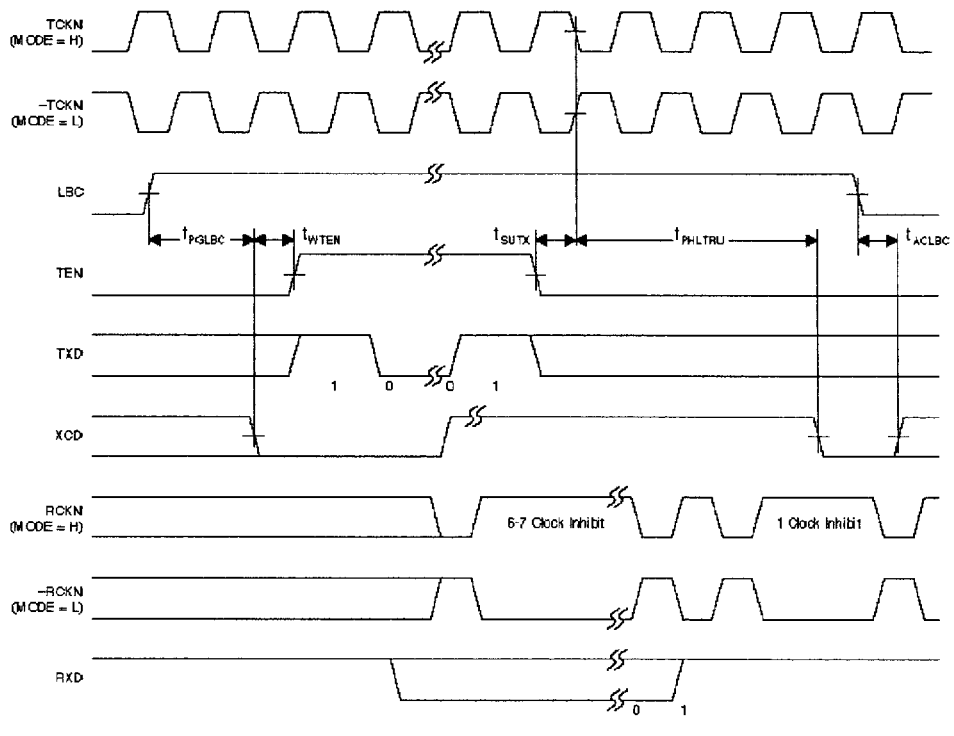
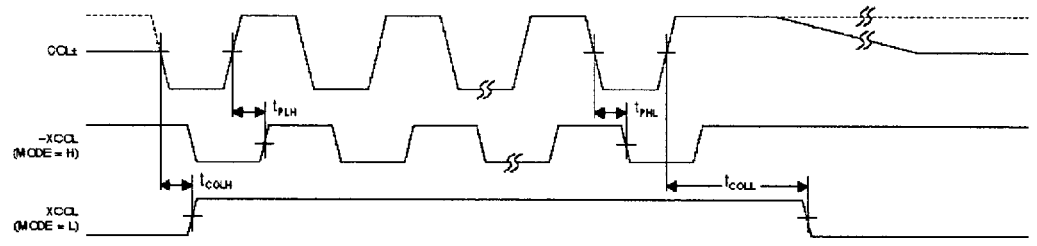


Figure 9. Loopback Timing

Loopback Timing[7]

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{PGLBC}	9	LBC receiving data purge time		—	260	—	ns
t_{ACLBC}	9	LBC receiving data accept time		—	80	—	ns
t_{PHLTRU}	9	Data through time		—	280	—	ns
t_{WTEN}	9	Wait time from XCD low to TEN high		0	—	—	ns



- - - - NOTE: If AC/DC = LOW

Figure 10. Collision Timing

Collision Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	10	COL± to -XCOL(XCOL) propagation delay time	MODE = High	—	15	50	ns
t_{PHL}	10		MODE = High	—	15	50	ns
t_{COLH}	10		MODE = Low	—	—	50	ns
t_{COLL}	10		MODE = Low	—	—	350	ns

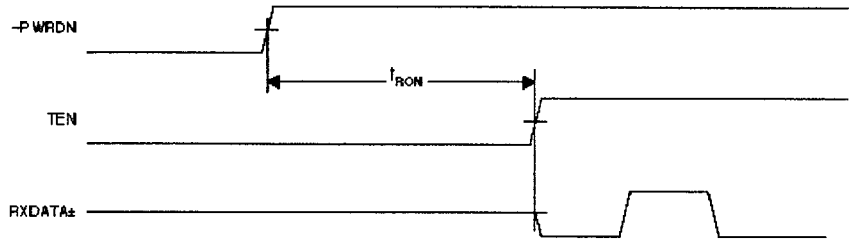


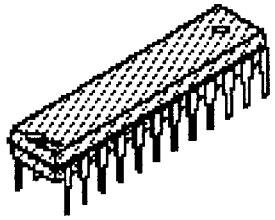
Figure 11. Reset Timing

Reset Timing

Symbol	Figure	Parameter Description	Conditions	Min.	Typ.	Max.	Units
t_{RON}	11	Start-up time after reset		200	—	—	µs

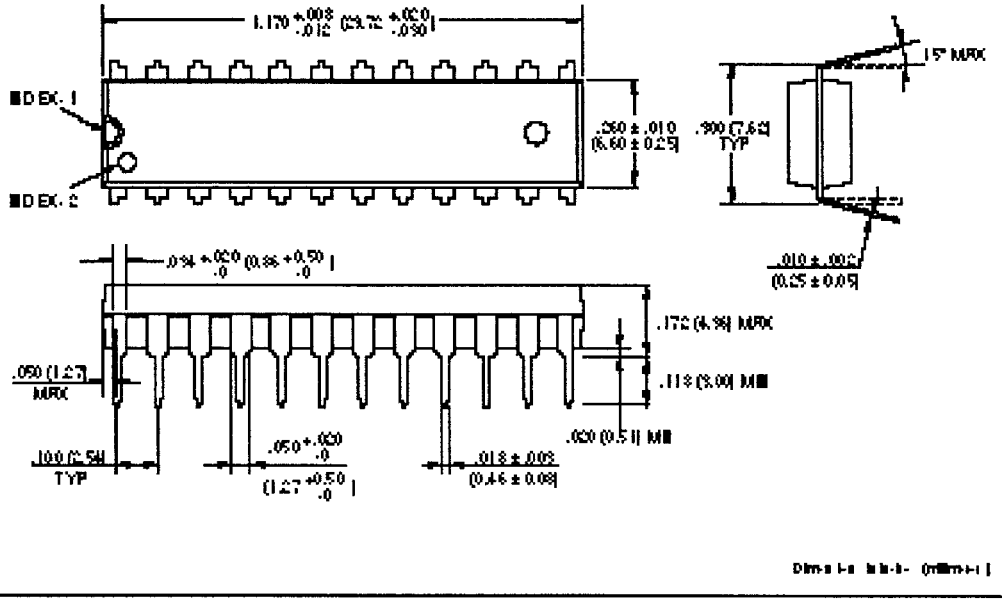
Notes:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. All voltage measurements are referenced to ground. See Figure 4 for test conditions.
4. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
5. The values of the oscillator capacitors may have to be tuned for a particular component layout. However, once the correct values are determined for that layout, tuning for each board is not required. Both capacitors should be adjusted for maximum voltage at X1.
6. The threshold of RXDATA± is changed to V_{ITD2} while AC/DC = High. (See DC Specifications for V_{ITD2}.)
7. During loopback operation, the COL± and RXDATA± inputs are ignored and the TXDATA± outputs are idle. XCD remains at a High level if MODE = Low.

24-Pin Plastic Dual In-Line Package

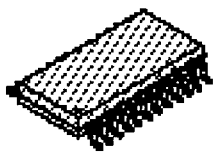


Ordering Information: MB86951P-G

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-24P-M03)



24-Pin Plastic Small Outline Package



Ordering Information: MB86951PF-G