



# Am95C96

## Optical Disk Controller

### DISTINCTIVE CHARACTERISTICS

- Supports the proposed X3B11 and ISO Continuous Composite Servo standard
- User programmable disk formats
- Minimal Rotational Latency Read/Write Operations
- 1:1 Sector Interleave Read/Write Operations
- 20 MHz System Clock
- Up to 32 MHz NRZ Serial Disk Data
- High Level Command Set
- Supports Intelligent SCSI-type Interfaces
- On-chip Buffer Management
- Direct support of DRAM Buffer (up to 4 MBytes)

### GENERAL DESCRIPTION

The Optical Disk Data Controller (ODC) is a highly programmable optical disk data format controller designed for use in both standard and custom applications. The device has been optimized for applications utilizing an embedded SCSI disk data manager, but it easily supports other intelligent proprietary interfaces as well.

As an embedded controller, the ODC handles the timing of all disk read/write control signals, the transfer of NRZ data between the disk and buffer RAM, and the transfer of disk data between a parallel host interface and buffer RAM. The ODC performs all buffer management and arbitration associated with this transfer of data while maintaining data integrity by using a dedicated interface to an external, high performance Advanced Burst Error Processor (ABEP). In addition, the ODC can perform advanced data mapping operations during data transfer, simplifying the task of cache management. The ODC can handle up to 4 Mbytes of data buffer Dynamic RAM directly, including address multiplexing and refresh, with no external logic.

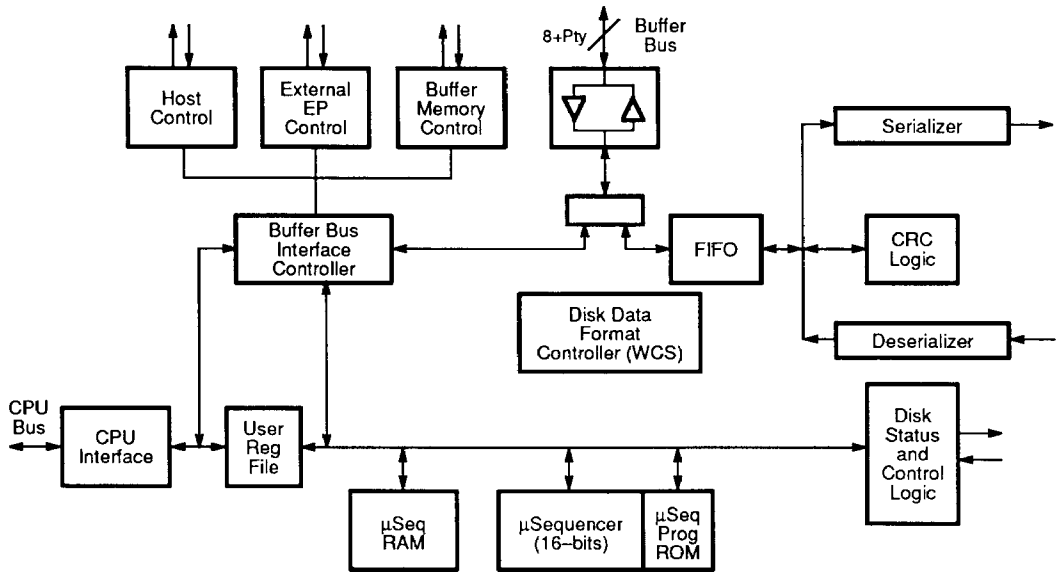
The ODC acts as an intelligent peripheral to a microprocessor or microcontroller. In an embedded SCSI disk

controller application, the control CPU (referred to in this document as simply the *CPU*), interprets all SCSI commands and controls disk head positioning and head selection, while the ODC handles all data transfers. The CPU sets up and initiates ODC operation by modifying as few as 6 ODC registers. ODC registers are directly addressable, and can be read or written directly with either an iAPX multiplexed address/data bus, or a Motorola 68xxx type non-multiplexed bus interface.

A dedicated interface to an external error processor permits the ODC to cope with the high error rates associated with optical media. Through this interface the ODC, in combination with AMD's Advanced Burst Error Processor (ABEP), can correct an error in as little as 10  $\mu$ secs. The ABEP supports 5 or 10 way interleaving with optional overlay CRC capability. The ABEP can correct up to 80 errors in a single sector in less than a millisecond. With this error correction capability, the ODC and ABEP can perform on-the-fly error correction without missing a sector. This avoids the necessity of jumping back to continue a disk read operation following a read error when handling spiral formatted media.

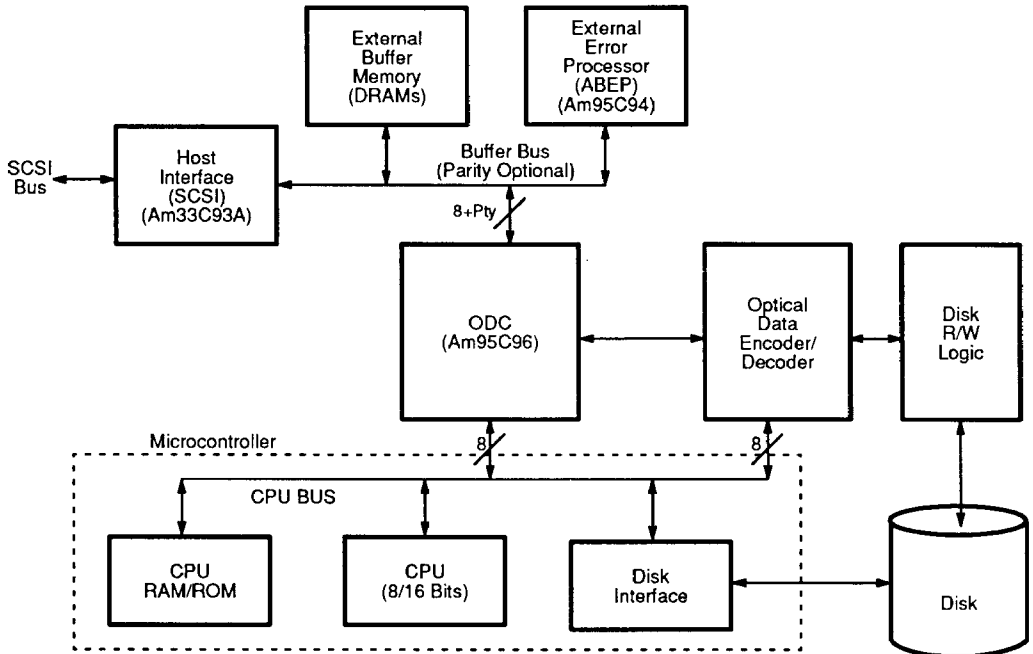
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## INTERNAL BLOCK DIAGRAM



10936-001A

## SYSTEM APPLICATION



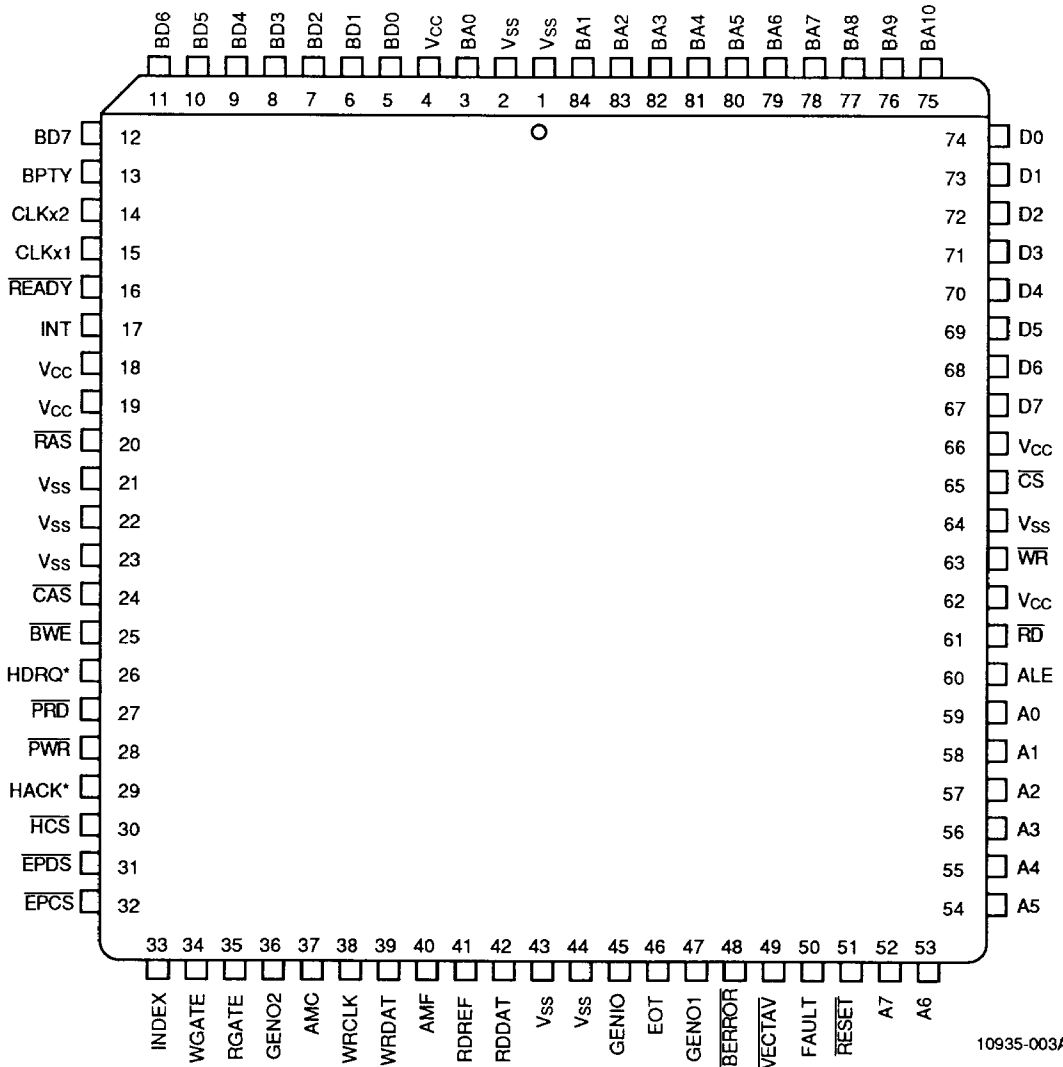
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## RELATED AMD PRODUCTS

Part Number	Description
Am33C93A	SCSI Controller
Am53C80	SCSI Controller
Am80188	Microprocessor
Am95C94	Advanced Burst Error Processor
Am80C188	CMOS Microprocessor

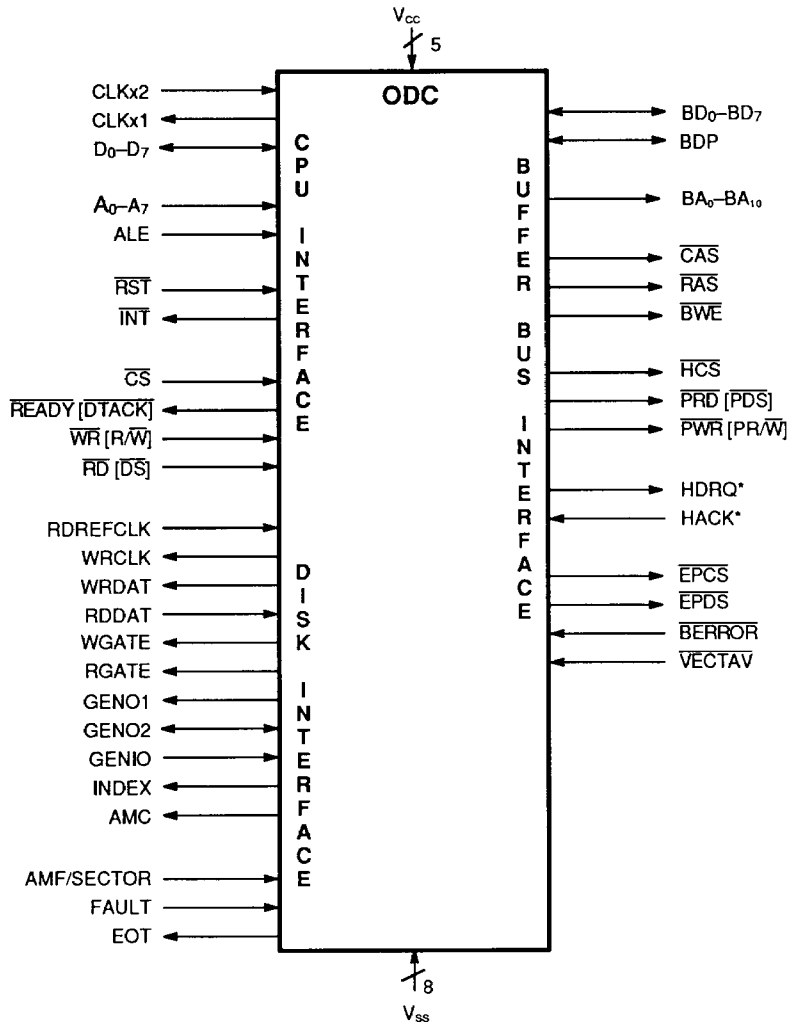
## CONNECTION DIAGRAM



10935-003A

\*These pins have programmable polarity.

# LOGIC DIAGRAM



10936-004A

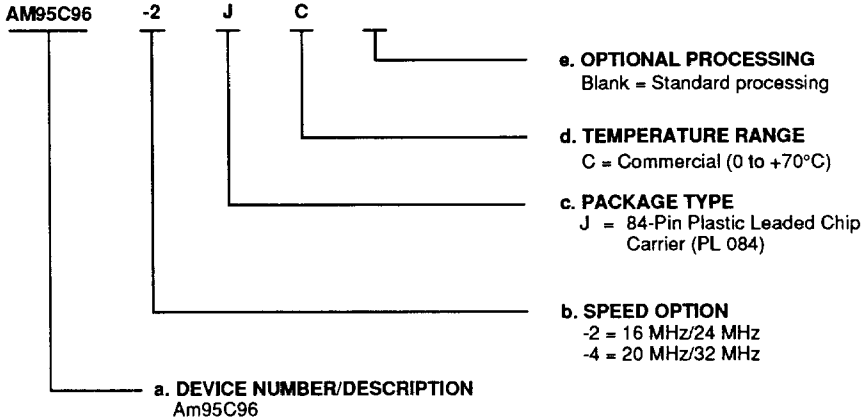
\* These pins have programmable polarity

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (If applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM95C96-2JC	JC
AM95C96-4JC	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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