2SK2684(L), 2SK2684(S)

Silicon N Channel DV–L MOS FET
High Speed Power Switching

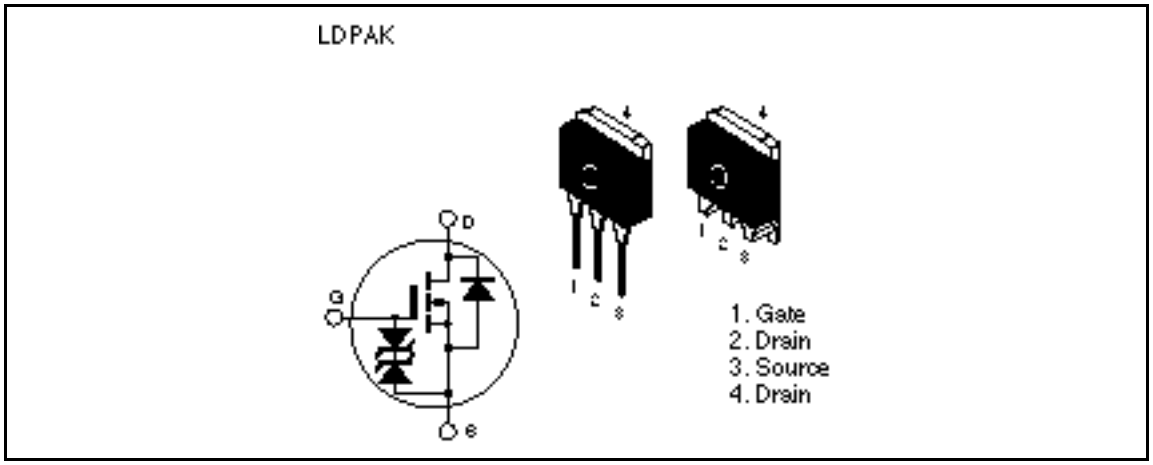
HITACHI

ADE-208-542
1st. Edition

Features

- Low on-resistance
  $R_{DS(on)}$ = 20 mΩ typ. (V_{GS} = 10V, I_D = 15 A)
- 4V gate drive devices.
- High speed switching

Outline



Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$*[1]	120	A
Body to drain diode reverse drain current	I_{DR}	30	A
Channel dissipation	Pch*[2]	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

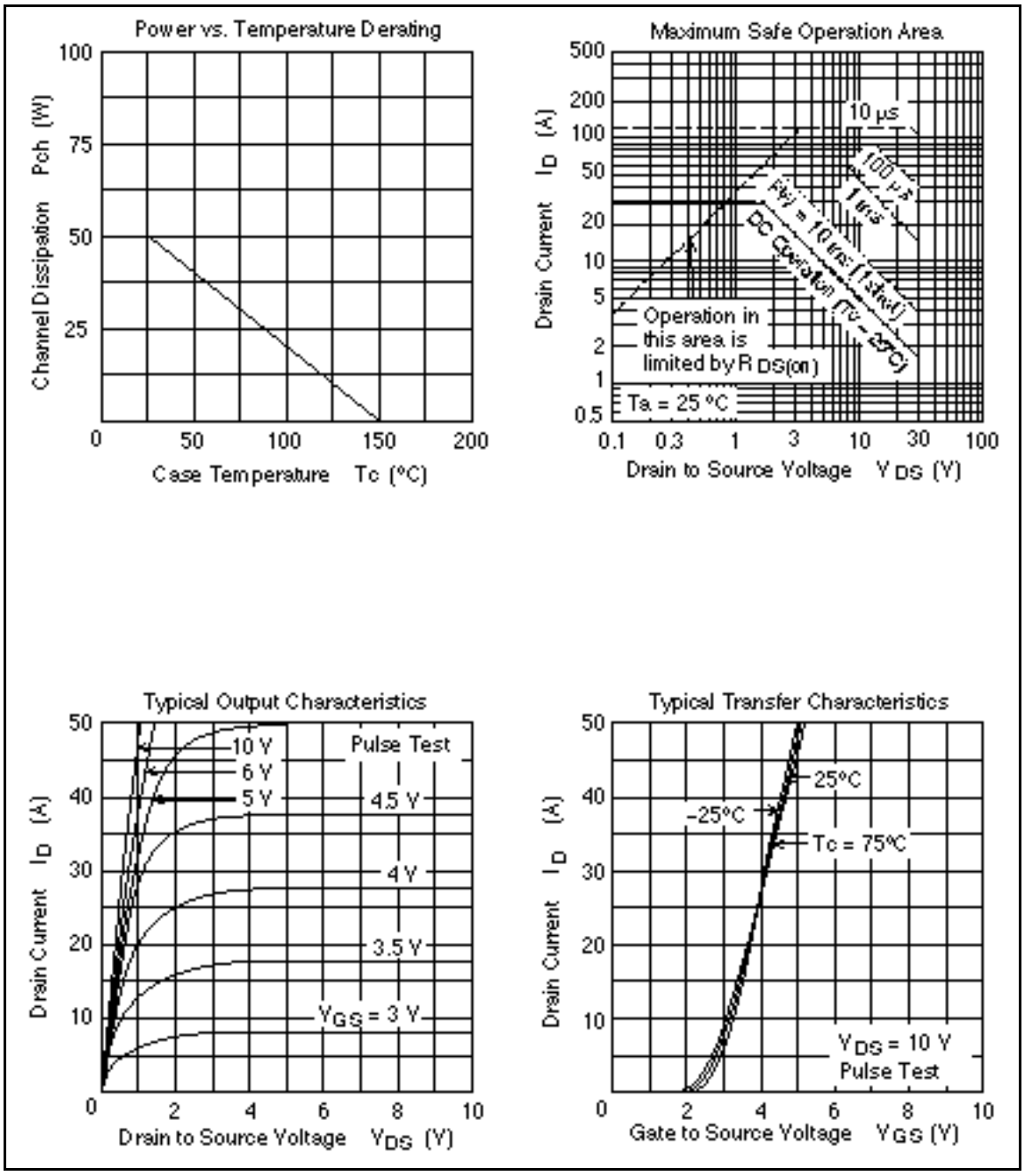
Notes: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C

Electrical Characteristics (Ta = 25°C)

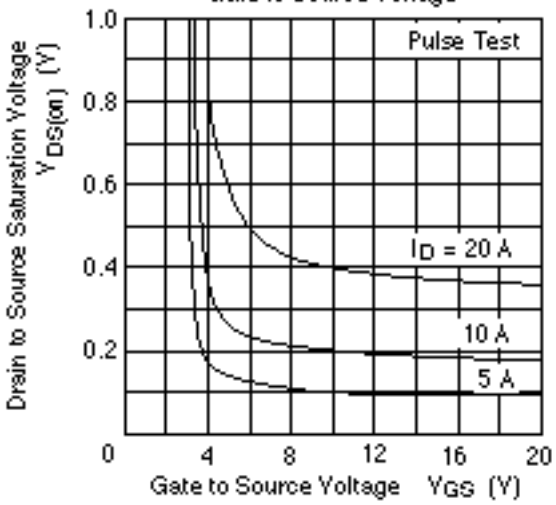
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	20	28	mΩ	I_D = 15A, V_{GS} = 10V*[1]
	$R_{DS(on)}$	—	35	50	mΩ	I_D = 15A, V_{GS} = 4V*[1]
Forward transfer admittance	$\|y_{fs}\|$	12	18	—	S	I_D = 15A, V_{DS} = 10V*[1]
Input capacitance	Ciss	—	750	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	520	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	210	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	16	—	ns	V_{GS} = 10V, I_D = 15A
Rise time	t_r	—	260	—	ns	R_L = 0.67Ω
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	90	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 30A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	45	—	ns	I_F = 30A, V_{GS} = 0 diF/ dt = 50A/µs

Note: 1. Pulse test

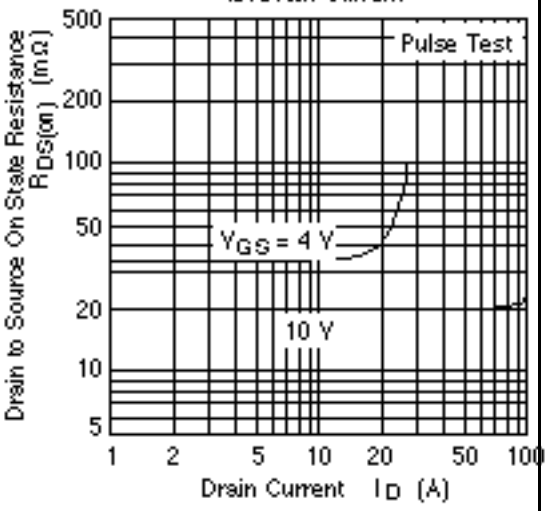
Main Characteristics



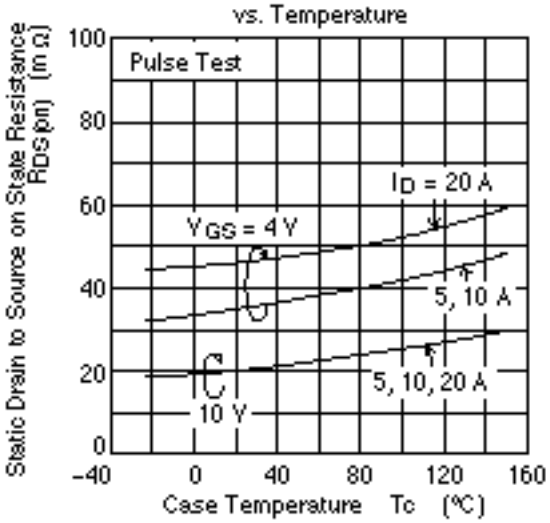
Drain to Source Saturation Voltage vs. Gate to Source Voltage



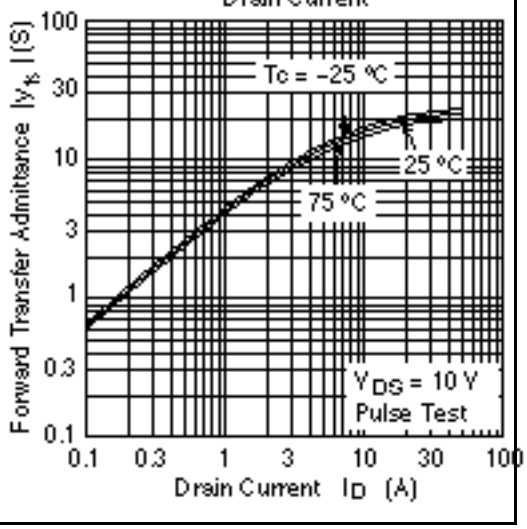
Static Drain to Source on State Resistance vs. Drain Current

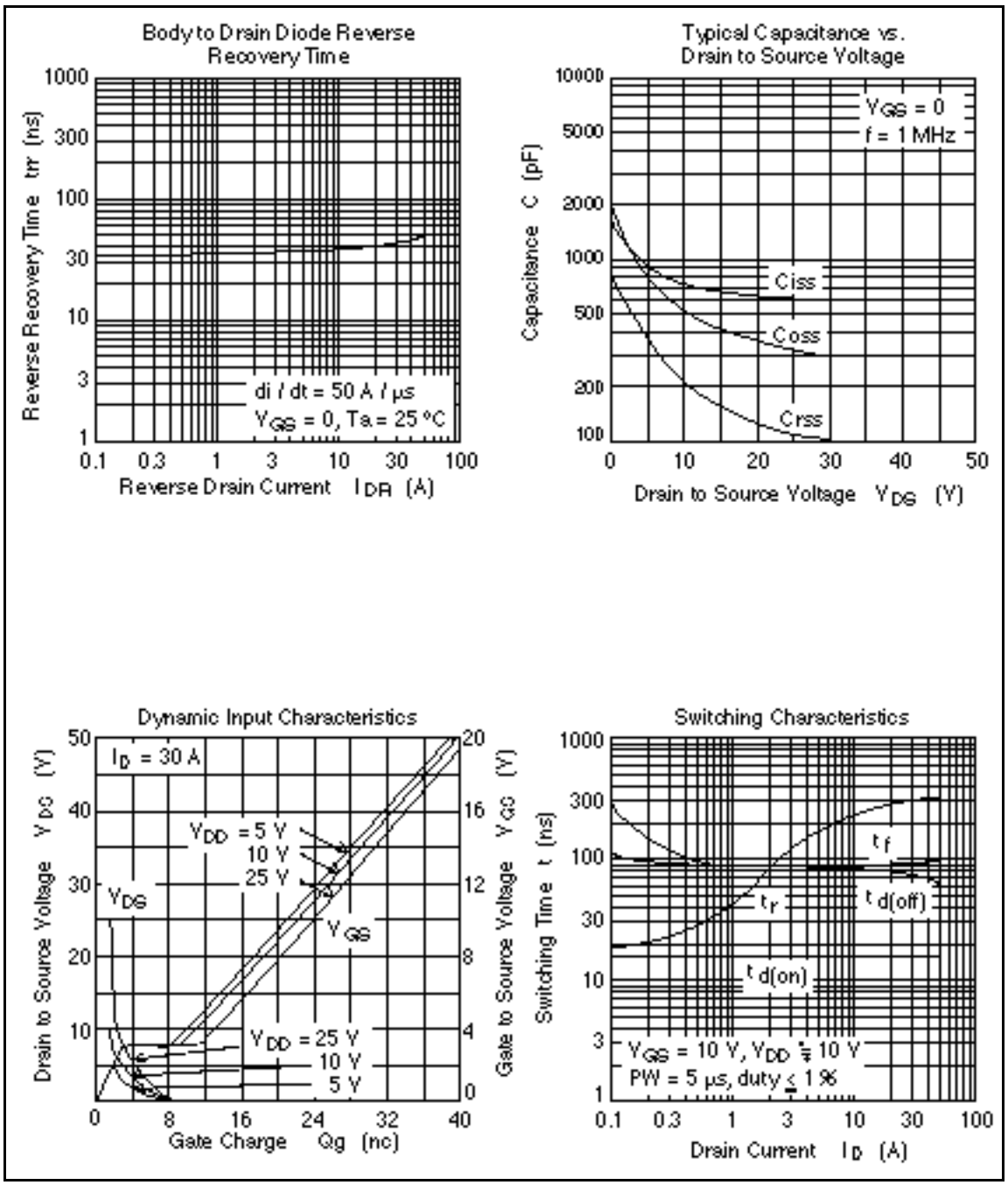


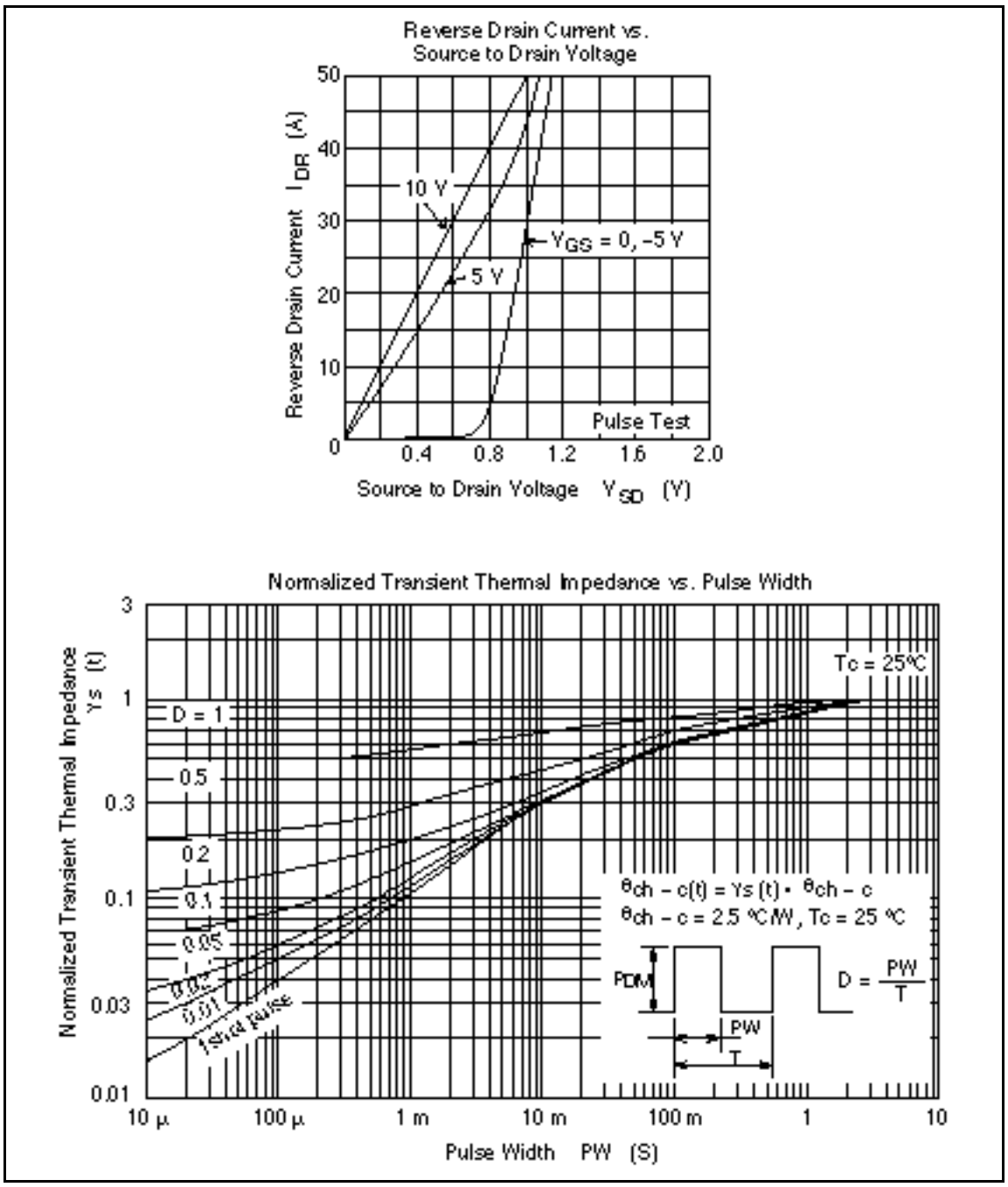
Static Drain to Source on State Resistance vs. Temperature

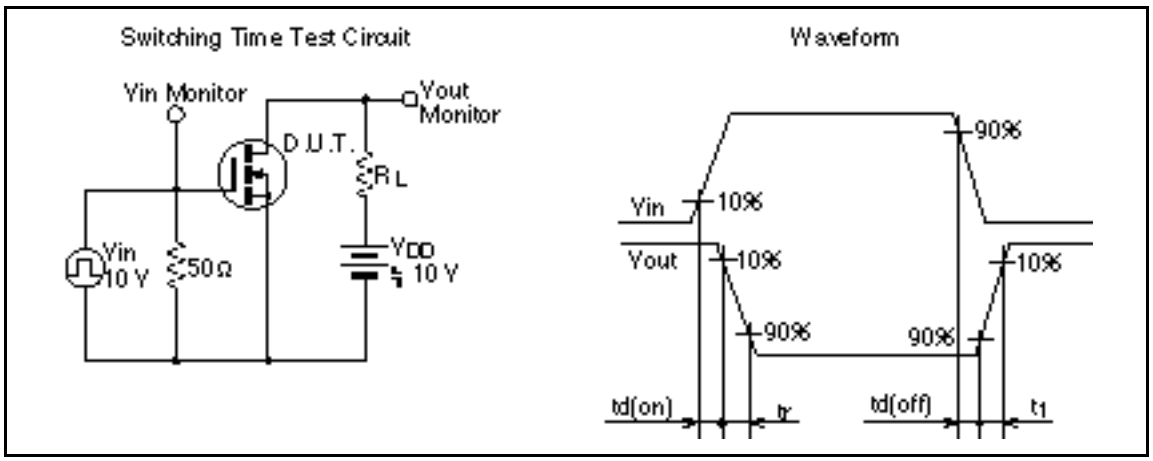


Forward Transfer Admittance vs. Drain Current



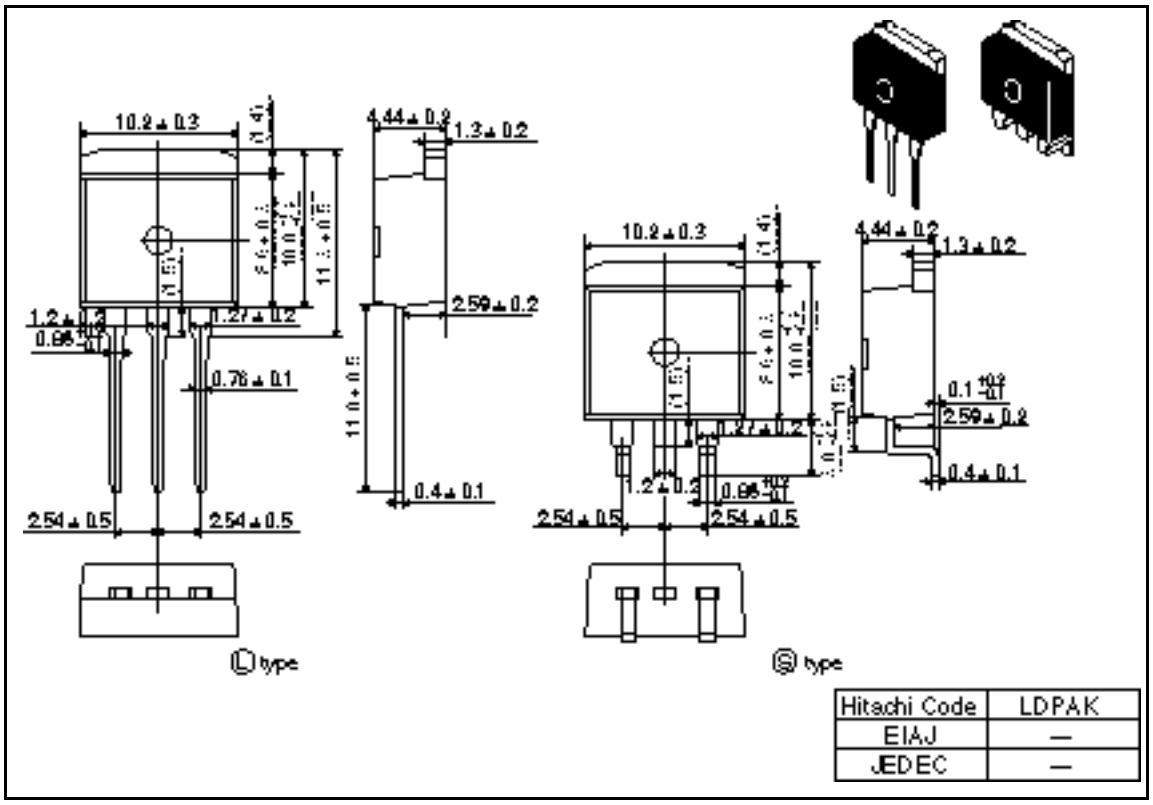

Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time trr (ns)
1000
300
100
30
10
3
1
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
0.1 0.3 1 3 10 30 100
Reverse Drain Current IDR (A)
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
5000
2000
1000
500
200
100
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
0 10 20 30 40 50
Drain to Source Voltage VDS (V)
Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
50
40
30
20
10
ID = 30 A
VDD = 5 V
10 V
25 V
VDS
VGS
VDD = 25 V
10 V
5 V
Gate to Source Voltage VGS (V)
20
16
12
8
4
0
0 8 16 24 32 40
Gate Charge Qg (nc)
Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
1
tf
tr
td(off)
td(on)
VGS = 10 V, VDD ≒ 10 V
PW = 5 µs, duty ≦ 1 %
0.1 0.3 1 3 10 30 100
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
50
40
30
20
10
0
10 V
V_{GS} = 0, -5 V
5 V
Pulse Test
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage V_{SD} (V)
Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance
γs (t)
3
1
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
Tc = 25°C
θch – c(t) = γs (t) • θch – c
θch – c = 2.5 °C/W, Tc = 25 °C
PDM
D = PW/T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
Pulse Width PW (S)


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T.
RL
Vin 10 V
50 Ω
VDD 10 V
Waveform
Vin
Vout
10%
90%
td(on)
tr
td(off)
tf

Package Dimensions

Unit: mm



Hitachi Code	LDPAK
EIAJ	—
JEDEC	—

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U.S.A.
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
#5 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071