19-2633; Rev 0; 10/02

MAXIM

4.5Ω Quad SPST Analog Switches in UCSP

General Description

The MAX4737/MAX4738/MAX4739 low-voltage, low on-resistance (R_{ON}), quad single-pole/single throw (SPST) analog switches operate from a single +1.8V to +5.5V supply. These devices are designed for USB 1.1 and audio switching applications.

The MAX4737/MAX4738/MAX4739 feature 4.5Ω R_{ON} (max) with 1.2Ω flatness and 0.4Ω matching between channels. These new switches feature guaranteed operation from +1.8V to +5.5V and are fully specified at 3V and 5V. These switches offer break-before-make switching (1ns) with t_{ON} <80ns and t_{OFF} <40ns at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply.

These switches are packaged in a chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 2mm × 2mm area and has a 4 × 4 bump array with a bump pitch of 0.5mm. These switches are also available in a 14-pin TSSOP package.

Applications

Battery-Operated Equipment

Audio/Video-Signal Routing

Low-Voltage Data-Acquisition Systems

Sample-and-Hold Circuits

Data-Acquisition Systems

Communications Circuits

UCSP is a trademark of Maxim Integrated Products, Inc.
Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features

- **USB 1.1 Signal Switching**
- **2ns (max) Differential Skew**
- **-3dB Bandwidth: >300MHz**
- **Low 20pF On-Channel Capacitance**
- **Low R_{ON}**
  4.5Ω (max) (+3V Supply)
  3Ω (max) (+5V Supply)
- **0.4Ω (max) R_{ON} Match (+3V Supply)**
- **1.2Ω (max) R_{ON} Flatness (+3V Supply)**
- **<0.5nA Leakage Current at +25°C**
- **High Off-Isolation: -55dB (10MHz)**
- **Low Crosstalk: -80dB (10MHz)**
- **Low Distortion: 0.03%**
- **+1.8V CMOS-Logic Compatible**
- **Single-Supply Operation from +1.8V to +5.5V**
- **Rail-to-Rail® Signal Handling**

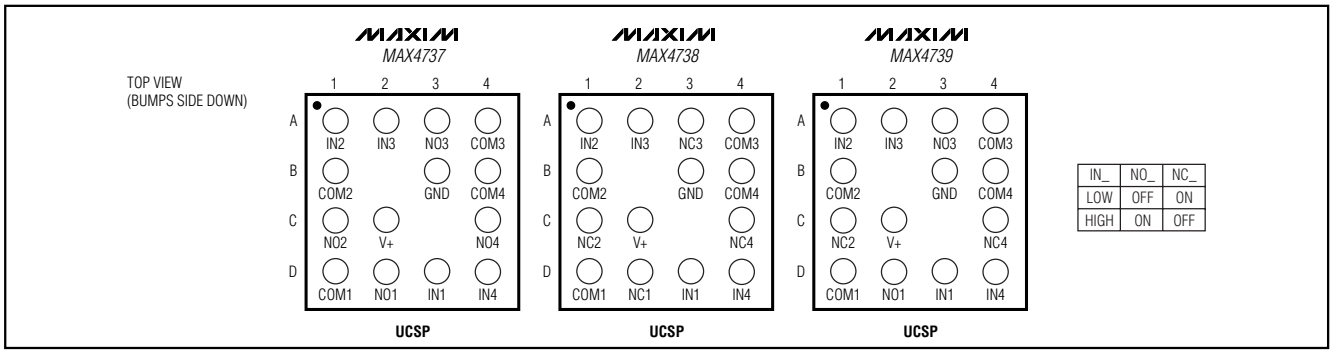
Ordering Information

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4737EUD	-40°C to +85°C	14 TSSOP	—
MAX4737EBE-T*	-40°C to +85°C	16 UCSP-16	4737
MAX4738EUD	-40°C to +85°C	14 TSSOP	—
MAX4738EBE-T*	-40°C to +85°C	16 UCSP-16	4738
MAX4739EUD	-40°C to +85°C	14 TSSOP	—
MAX4739EBE-T*	-40°C to +85°C	16 UCSP-16	4739

Note: *UCSP package requires special solder temperature profile described in the Absolute Maximum Ratings section.*

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. See the UCSP reliability notice in the UCSP Reliability section of this data sheet for more information.*

Pin Configurations/Functional Diagrams/Truth Tables



IN_	NO_	NC_
LOW	OFF	ON
HIGH	ON	OFF

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND)
V+, IN_.....-0.3V to +6.0V
COM_, NO_, NC_ (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_.....±100mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle).....±200mA
Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 6.3mW/°C above +70°C).....500mW
16-Bump UCSP (derate 8.3mW/°C above +70°C).....659mW
ESD Method 3015.7.....>2kV
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Bump Temperature (soldering) (Note 2)
Infrared (15s).....+220°C
Vapor Phase (60s).....+215°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry standard specification, JEDEC 020A, paragraph 7.6, table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
ANALOG SWITCH							
On-Resistance (Note 5)	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		3.0	4.5	Ω
			T_{MIN} to T_{MAX}			5	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.1	0.4	Ω
			T_{MIN} to T_{MAX}			0.5	
On-Resistance Flatness (Note 7)	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 1.5V, 2.0V	+25°C		0.6	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 8)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ Off-Leakage Current (Note 8)	$I_{COM\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 8)	$I_{COM\_(ON)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V, or floating	+25°C	-1	+0.01	+1	nA
			T_{MIN} to T_{MAX}	-2		+2	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		40	80	ns
			T_{MIN} to T_{MAX}			100	
Turn-Off Time	t_{OFF}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		20	40	ns
			T_{MIN} to T_{MAX}			50	
Break-Before-Make Time Delay (MAX4739 Only) (Note 8)	t_{BBM}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		8		ns
			T_{MIN} to T_{MAX}	1			
Skew (Note 8)	t_{SKEW}	R_S = 39Ω, C_L = 50pF, Figure 3	T_{MIN} to T_{MAX}		0.15	2	ns
Charge Injection	Q	V_{GEN} = 2V, R_{GEN} = 0Ω, C_L = 1.0nF, Figure 4	+25°C		5		pC
Off-Isolation (Note 9)	V_{ISO}	f = 10MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5a	+25°C		-55		dB
		f = 1MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5a			-80		
Crosstalk (Note 10)	V_{CT}	f = 10MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5b	+25°C		-80		dB
		f = 1MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5b			-110		
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C_L = 5pF, 50Ω in and out, Figure 5a	+25°C		300		MHz
Total Harmonic Distortion	THD	R_L = 600Ω	+25°C		0.03		%
NO_, NC_ Off-Capacitance	$C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$	f = 1MHz, Figure 6	+25°C		9		pF
Switch On-Capacitance	C_{ON}	f = 1MHz, Figure 6	+25°C		15		pF
DIGITAL I/O							
Input Logic High Voltage	V_{IH}		T_{MIN} to T_{MAX}	1.4			V
Input Logic Low Voltage	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	I_{IN}	V+ = 3.6V, $V_{IN\_}$ = 0 or 5.5V	T_{MIN} to T_{MAX}	-0.1		+0.1	µA

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
SUPPLY							
Supply Voltage Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Positive Supply Current	I+	V+ = 5.5V, $V_{IN\_}$ = 0V or V+	T_{MIN} to T_{MAX}			1	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$		T_{MIN} to T_{MAX}	0		V+	V
ANALOG SWITCH							
On-Resistance (Note 5)	R_{ON}	V+ = 4.2V; $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	+25°C		1.7	3.0	Ω
			T_{MIN} to T_{MAX}			35	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = 4.2V; $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	+25°C		0.1	0.3	Ω
			T_{MIN} to T_{MAX}			0.4	
On-Resistance Flatness (Note 7)	$R_{FLAT(ON)}$	V+ = 4.2V; $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 2.0V, 3.5V	+25°C		0.4	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 8)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1.0V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1.0V	+25°C	-0.5	0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ Off-Leakage Current (Note 8)	$I_{COM\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 4.5V, 1V	+25°C	-0.5	0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 8)	$I_{COM\_(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 1.0V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 4.5V, or floating	+25°C	-1	0.01	+1	nA
			T_{MIN} to T_{MAX}	-2		+2	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$, $V_{NC\_}$ = 3.0V; R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		30	80	ns
			T_{MIN} to T_{MAX}			100	
Turn-Off Time	t_{OFF}	$V_{NO\_}$, $V_{NC\_}$ = 3.0V; R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		20	40	ns
			T_{MIN} to T_{MAX}			50	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Break-Before-Make Time Delay (MAX4739 Only) (Note 8)	t_{BBM}	$V_{NO\_}$, $V_{NC\_}$ = 3.0V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		8		ns
			T_{MIN} to T_{MAX}	1			
Skew (Note 8)	t_{SKEW}	R_S = 39Ω, C_L = 50pF, Figure 3	T_{MIN} to T_{MAX}		0.15	2	ns
DIGITAL I/O							
Input Logic High Voltage	V_{IH}		T_{MIN} to T_{MAX}	2.0			V
Input Logic Low Voltage	V_{IL}		T_{MIN} to T_{MAX}			0.8	V
Input Leakage Current	I_{IN}	V+ = 5.5V, $V_{IN\_}$ = 0V or V+	T_{MIN} to T_{MAX}	-0.1		+0.1	µA
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Positive Supply Current	I+	V+ = 5.5V, $V_{IN\_}$ = 0V or V+	T_{MIN} to T_{MAX}			1	µA

Note 3: UCSP parts are 100% tested at +25°C only, and guaranteed by design over the specified temperature range. TSSOP parts are 100% tested at T_{MAX} and guaranteed by design over the specified temperature range.

Note 4: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

Note 5: Guaranteed by design for UCSP parts.

Note 6: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 8: Guaranteed by design.

Note 9: Off-Isolation = $20\log_{10} (V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

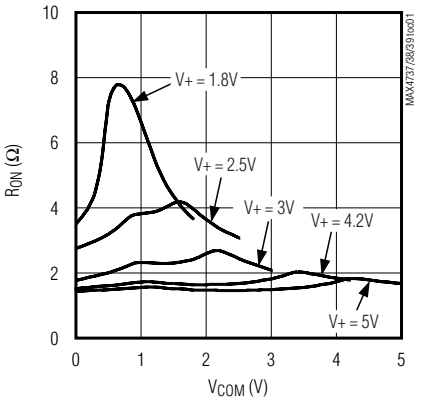
Note 10: Between any two switches.

4.5Ω Quad SPST Analog Switches in UCSP

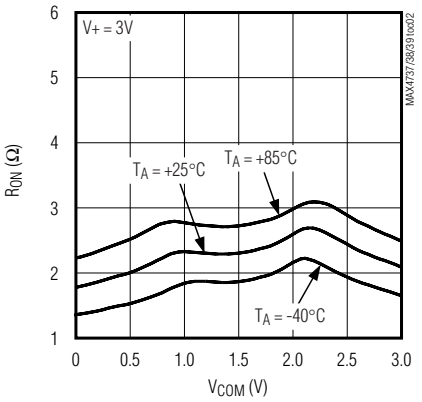
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

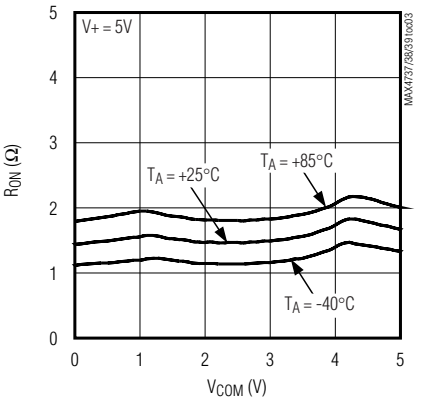
ON-RESISTANCE vs. V_{COM}



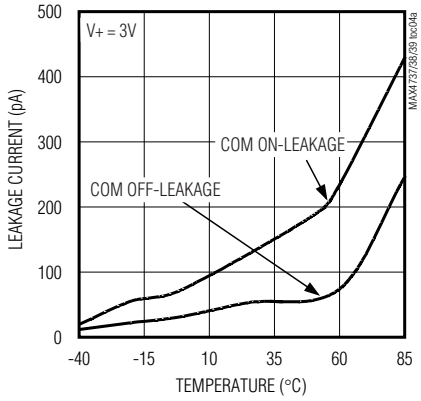
ON-RESISTANCE vs. V_{COM}



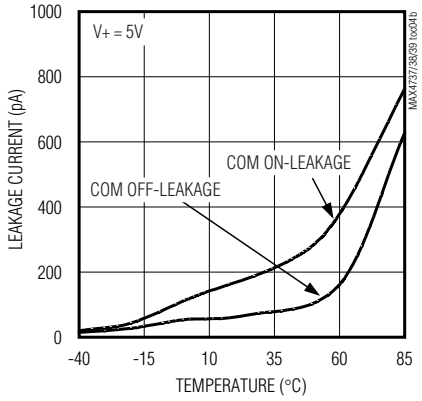
ON-RESISTANCE vs. V_{COM}



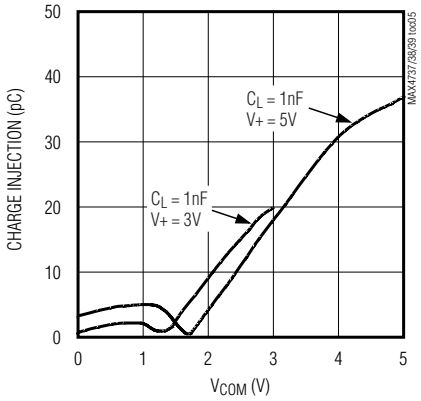
LEAKAGE CURRENT vs. TEMPERATURE



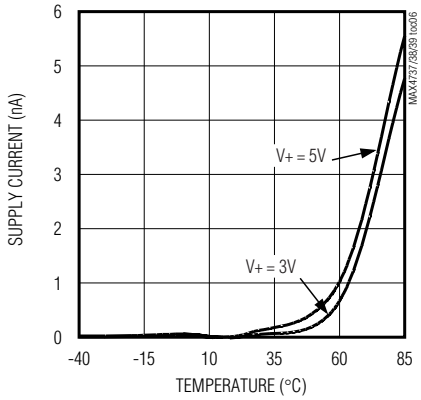
LEAKAGE CURRENT vs. TEMPERATURE



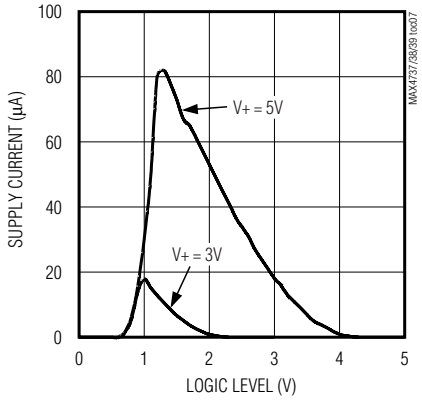
CHARGE INJECTION vs. V_{COM}



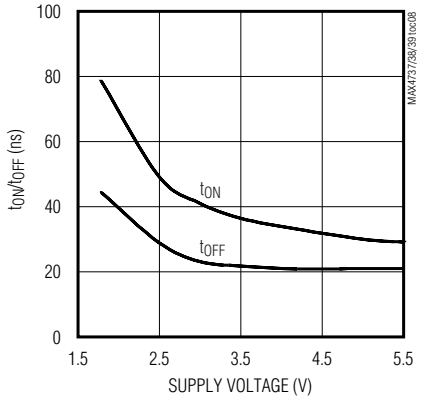
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. LOGIC LEVEL



TURN-ON/OFF TIME vs. SUPPLY VOLTAGE

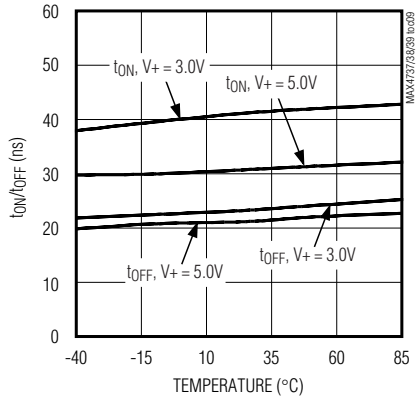


MAXIM

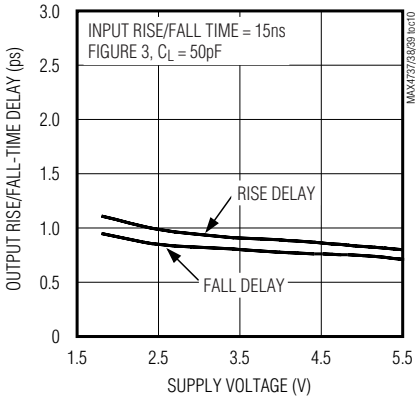
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

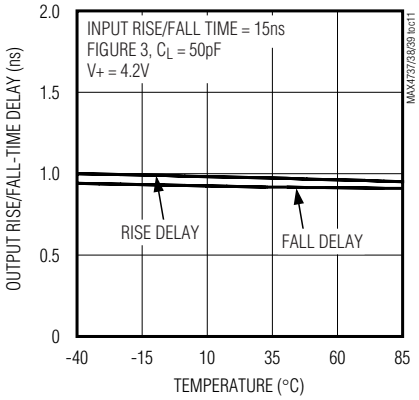
TURN-ON/OFF TIME vs. TEMPERATURE



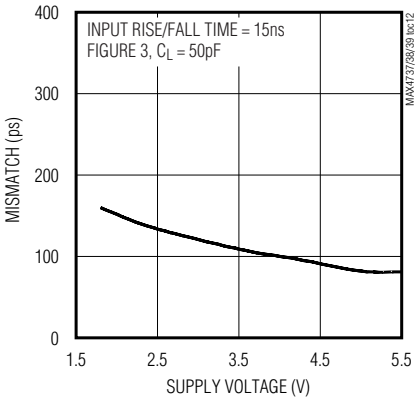
RISE/FALL-TIME DELAY vs. SUPPLY VOLTAGE



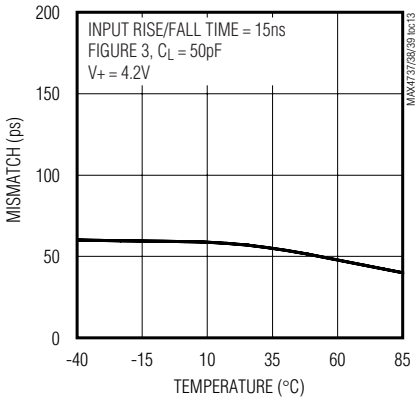
RISE/FALL-TIME DELAY vs. TEMPERATURE



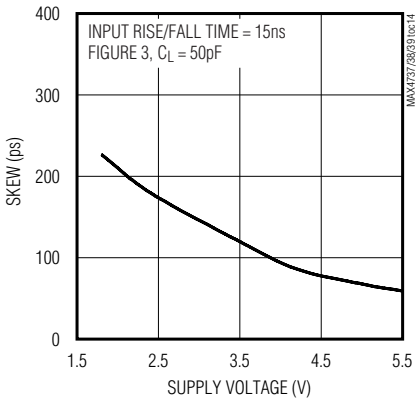
RISE TIME TO FALL TIME MISMATCH vs. SUPPLY VOLTAGE



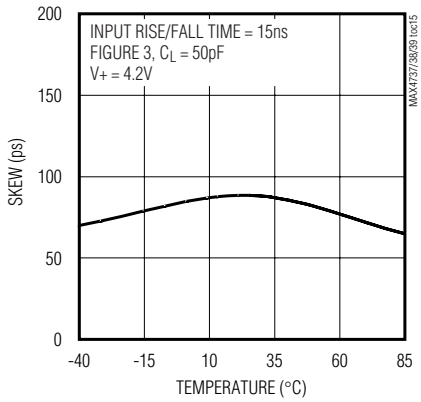
RISE TIME TO FALL TIME MISMATCH vs. TEMPERATURE



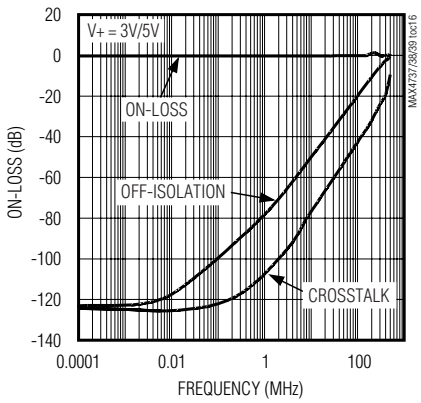
SKEW vs. SUPPLY VOLTAGE



SKEW vs. TEMPERATURE



FREQUENCY RESPONSE

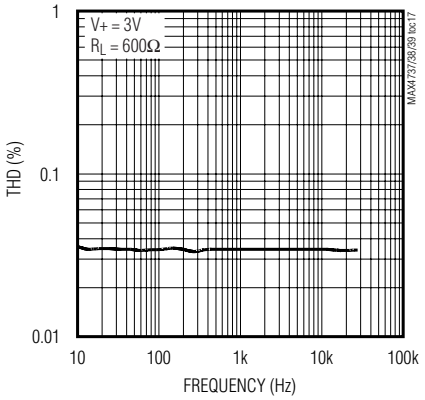


4.5Ω Quad SPST Analog Switches in UCSP

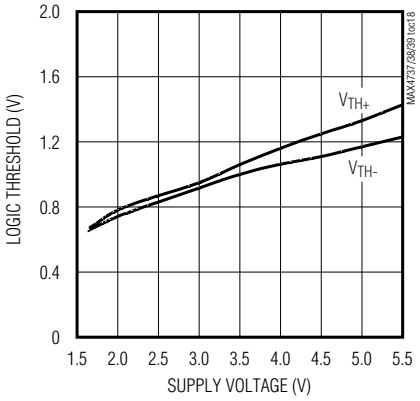
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION vs. FREQUENCY



LOGIC THRESHOLD vs. SUPPLY VOLTAGE



Pin Description

PIN						NAME	FUNCTION
MAX4737		MAX4738		MAX4739			
UCSP	TSSOP	UCSP	TSSOP	UCSP	TSSOP		
D2	1	—	—	D2	1	NO1	Analog-Switch Normally Open Terminal
—	—	D2	1	—	—	NC1	Analog-Switch Normally Closed Terminal
D1	2	D1	2	D1	2	COM1	Analog-Switch Common Terminal
C1	3	—	—	—	—	NO2	Analog-Switch Normally Open Terminal
—	—	C1	3	C1	3	NC2	Analog-Switch Normally Closed Terminal
B1	4	B1	4	B1	4	COM2	Analog-Switch Common Terminal
A1	5	A1	5	A1	5	IN2	Logic-Control Digital Input
A2	6	A2	6	A2	6	IN3	Logic-Control Digital Input
B3	7	B3	7	B3	7	GND	Ground. Connect to digital ground.
A3	8	—	—	A3	8	NO3	Analog-Switch Normally Open Terminal
—	—	A3	8	—	—	NC3	Analog-Switch Normally Closed Terminal
A4	9	A4	9	A4	9	COM3	Analog-Switch Common Terminal
B4	10	B4	10	B4	10	COM4	Analog-Switch Common Terminal
C4	11	—	—	—	—	NO4	Analog-Switch Normally Open Terminal
—	—	C4	11	C4	11	NC4	Analog-Switch Normally Closed Terminal
D4	12	D4	12	D4	12	IN4	Logic-Control Digital Input
D3	13	D3	11	D3	11	IN1	Logic-Control Digital Input
C2	14	C2	14	C2	14	V+	Positive Analog Supply

Detailed Description

The MAX4737/MAX4738/MAX4739 quad SPST analog switches operate from a single +1.8V to +5.5V supply. The MAX4737/MAX4738/MAX4739 offer excellent AC characteristics, <0.5nA leakage current, less than 1ns differential skew, and 15pF on-channel capacitance. All of these devices are CMOS-logic compatible with V+ to GND signal handling capability.

The MAX4737/MAX4738/MAX4739 are USB-complaint switches that provide 4.5Ω (max) on-resistance and 15pF on-channel capacitance to maintain signal integrity. At 12Mbps (USB full-speed data rate specification), the MAX4737/MAX4738/MAX4739 introduce less than 2ns propagation delay between input and output signals and less than 0.5ns change in skew for the output signals (see Figure 4).

The MAX4737 has four normally open (NO) switches, the MAX4738 has four normally closed (NC) switches, and the MAX4739 has two NO switches and two NC switches.

Applications Information

Digital Control Inputs

The MAX4737/MAX4738/MAX4739 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN_ can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving the control logic inputs rail-to-rail minimizes power consumption. For a +1.8V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) are passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1µF capacitor connected from V+ to GND is adequate for most applications.

UCSP Package Considerations

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Chip-Scale Package).

UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a UCSP package. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

4.5Ω Quad SPST Analog Switches in UCSP

Test Circuits/Timing Diagrams

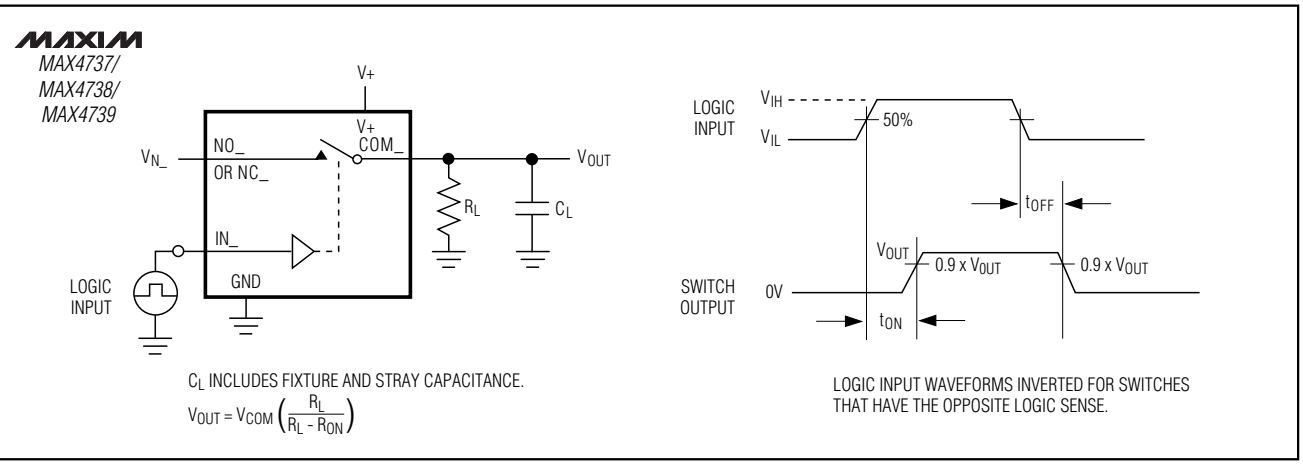


Figure 1. Switching Time

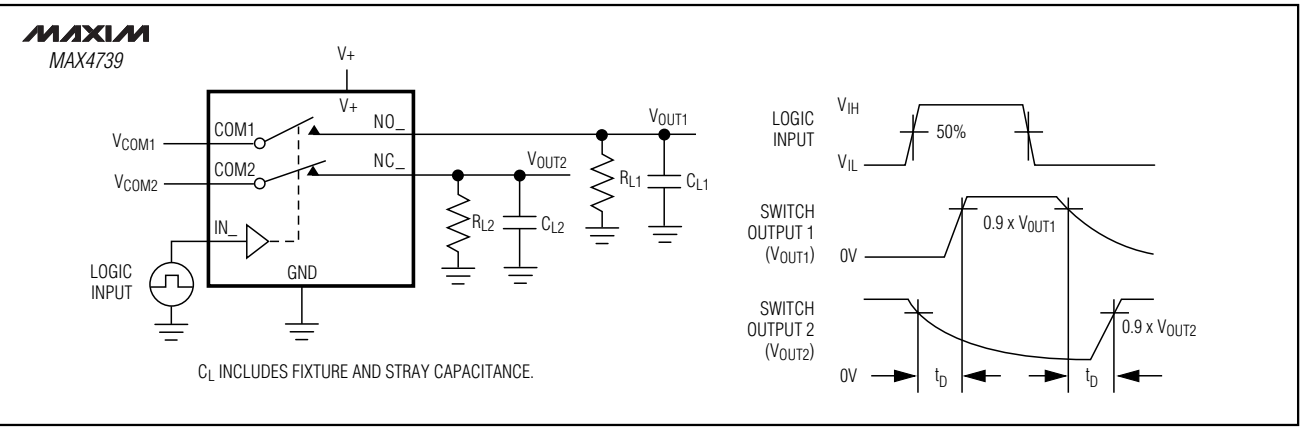
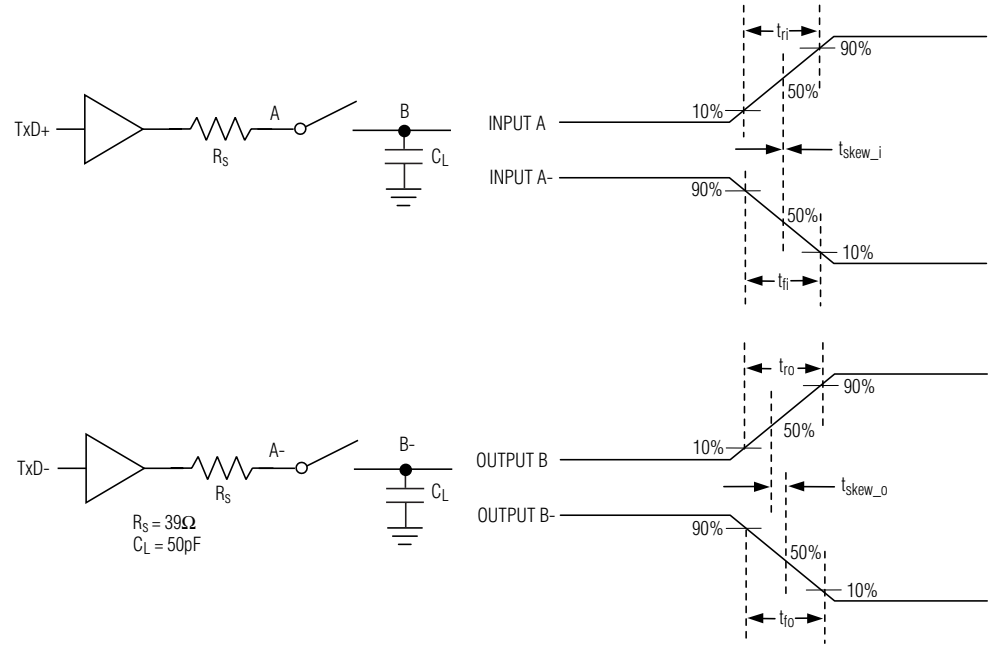


Figure 2. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)



$|t_{ro} - t_{ri}|$ DELAY DUE TO SWITCH FOR RISING INPUT AND RISING OUTPUT SIGNALS.

$|t_{fo} - t_{fi}|$ DELAY DUE TO SWITCH FOR FALLING INPUT AND FALLING OUTPUT SIGNALS.

$|t_{skew\_o}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR OUTPUT SIGNALS.

$|t_{skew\_i}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR INPUT SIGNALS.

Figure 3. Input/Output Skew Timing Diagram

4.5Ω Quad SPST Analog Switches in UCSP

Test Circuits/Timing Diagrams (continued)

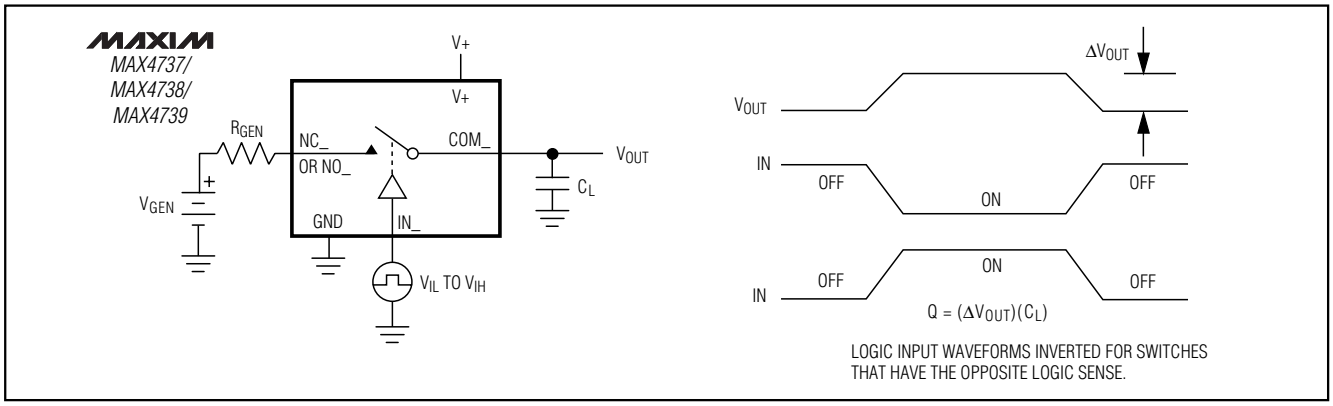


Figure 4. Charge Injection

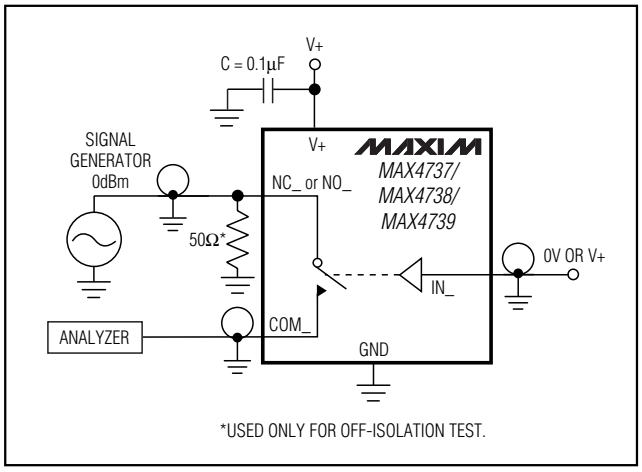


Figure 5a. On-Loss and Off-Isolation

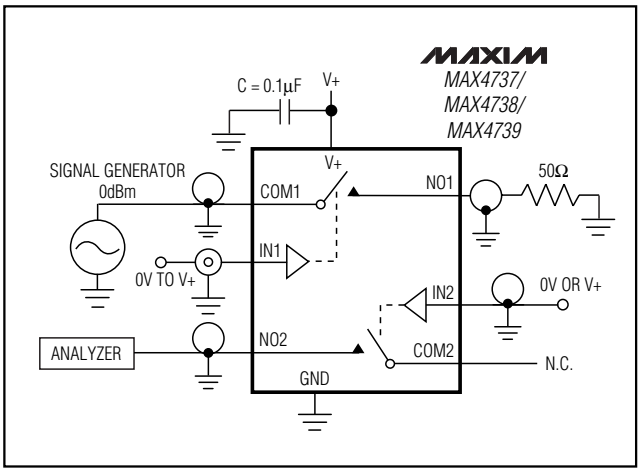


Figure 5b. Crosstalk Test Circuit

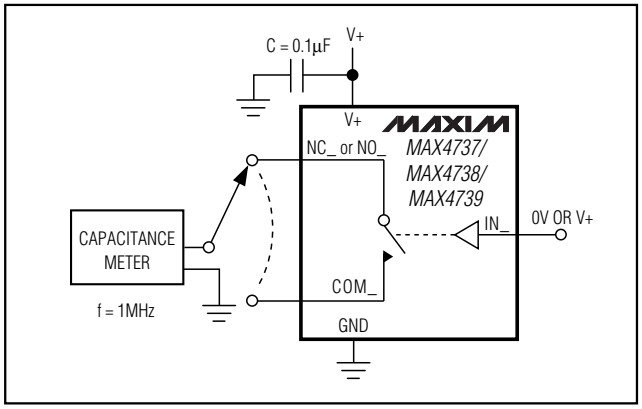


Figure 6. Channel Off/On-Capacitance

Chip Information

TRANSISTOR COUNT: 361

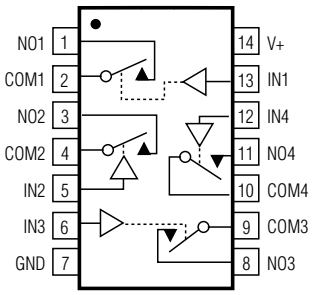
PROCESS: CMOS

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW

MAXIM

MAX4737

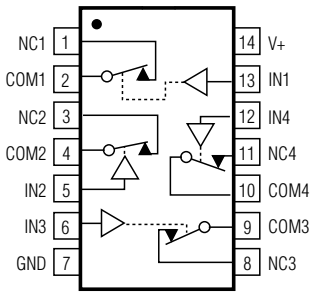


TSSOP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

MAXIM

MAX4738

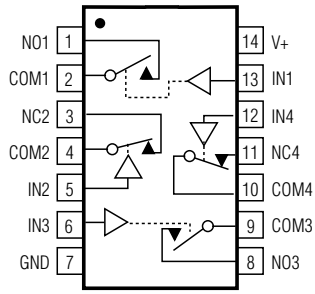


TSSOP

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

MAXIM

MAX4739



TSSOP

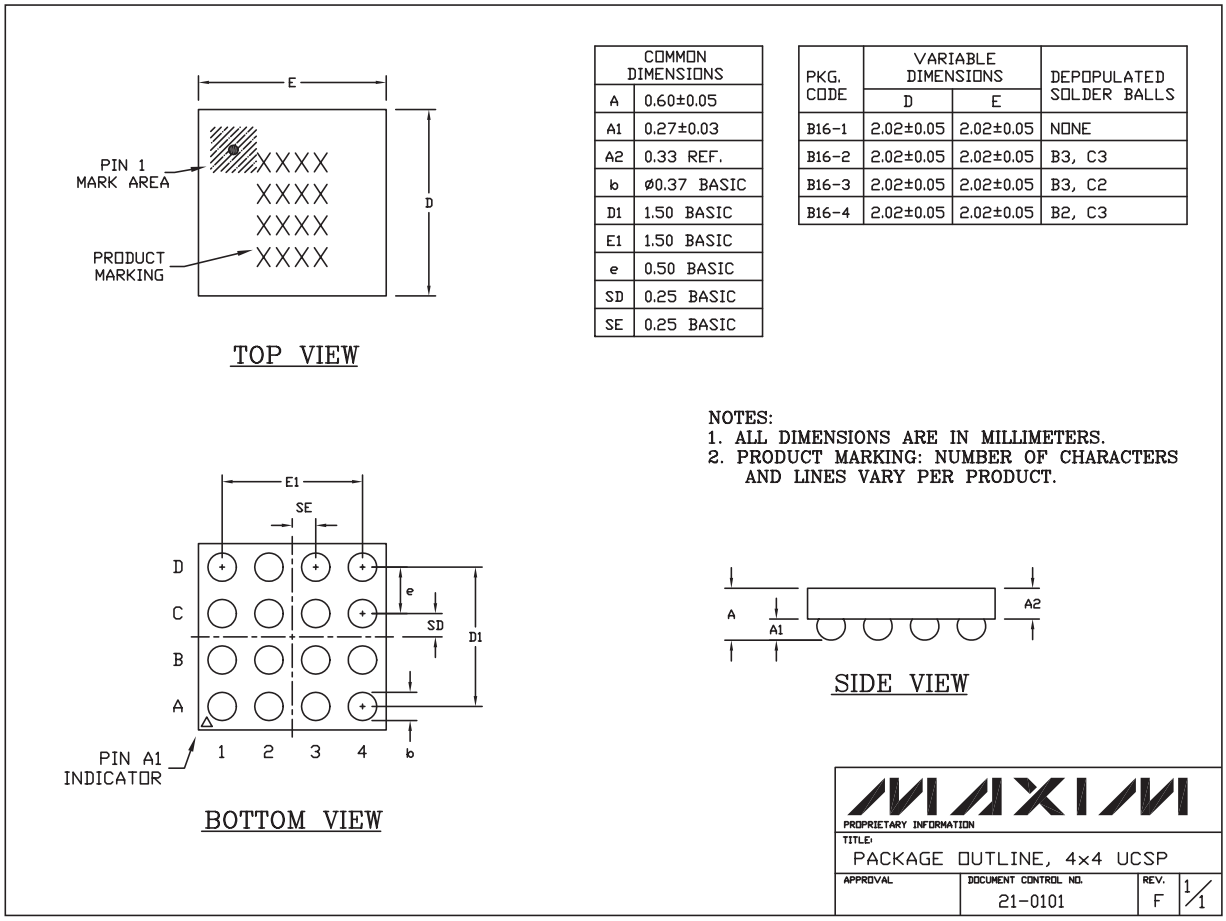
INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF

4.5Ω Quad SPST Analog Switches in UCSP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

16L,UCSP.EPS



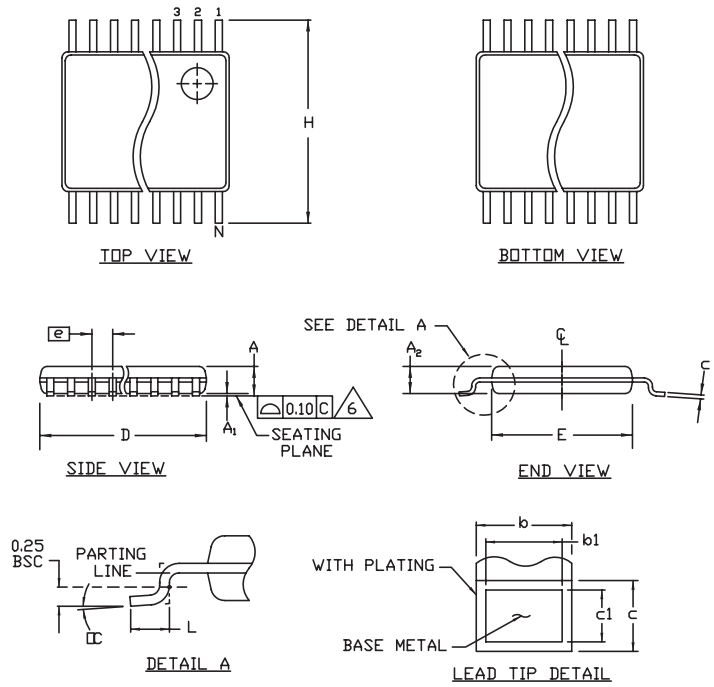
COMMON DIMENSIONS	
A	0.60±0.05
A1	0.27±0.03
A2	0.33 REF.
b	ø0.37 BASIC
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1