

# DATA SHEET

## **BSP127**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

**BSP127**

## FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

## DESCRIPTION

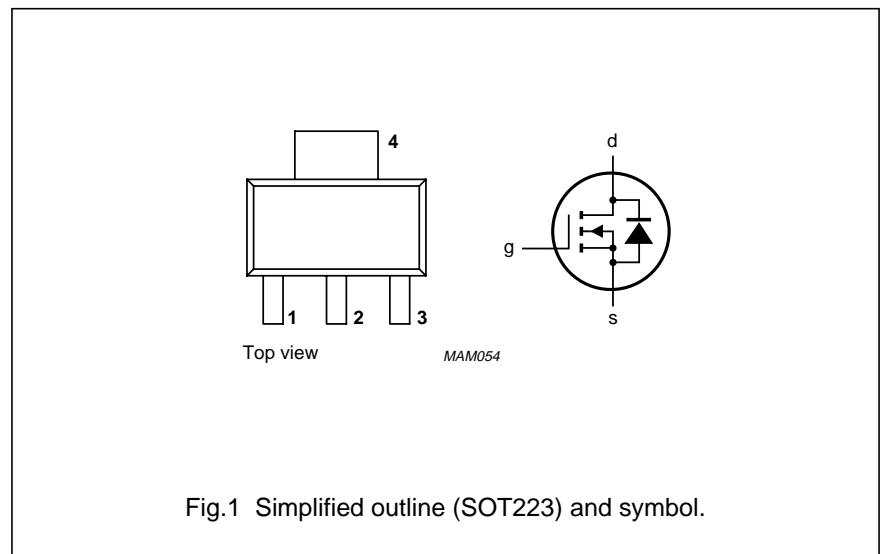
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

## PINNING - SOT223

PIN	DESCRIPTION
Code: BSP127	
1	gate
2	drain
3	source
4	drain

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	drain-source voltage	270	V
$I_D$	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	$\Omega$
$V_{GS(th)}$	gate-source threshold voltage	2	V



## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$I_D$	DC drain current		–	350	mA
$I_{DM}$	peak drain current		–	1.4	A
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ }^\circ\text{C}$ (note 1)	–	1.5	W
$T_{stg}$	storage temperature range		–65	150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$

## THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3 K/W

## Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

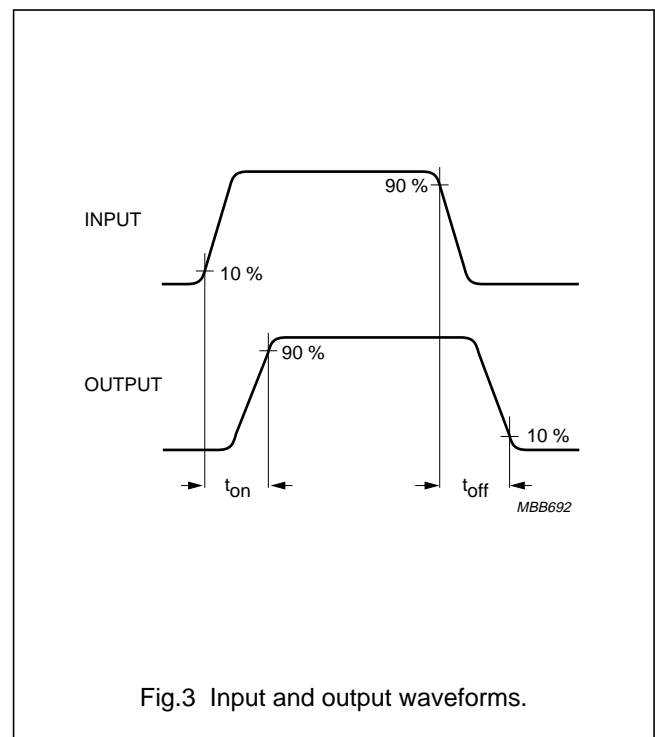
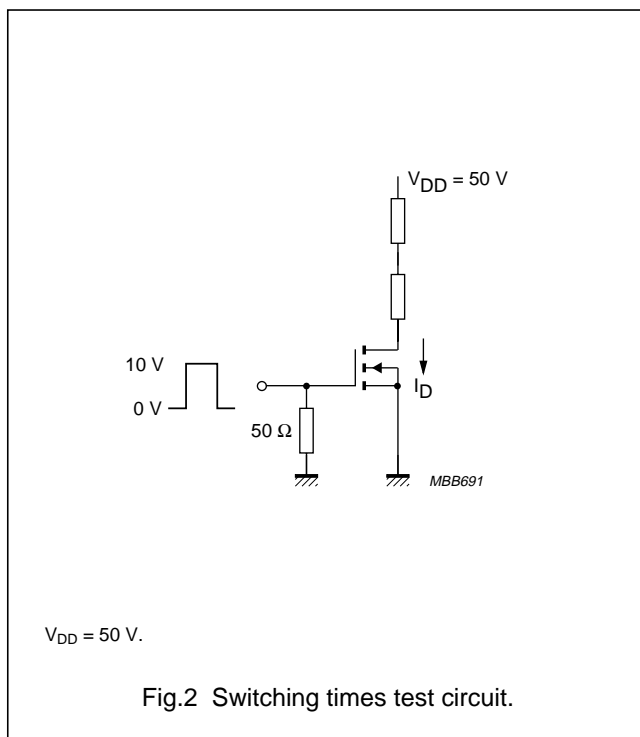
# N-channel enhancement mode vertical D-MOS transistor

BSP127

## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$	270	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 220\text{ V}; V_{GS} = 0$	–	–	1	$\mu\text{A}$
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{GS} = V_{DS}$	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	–	6.5	8	$\Omega$
		$I_D = 20\text{ mA}; V_{GS} = 2.4\text{ V}$	–	9	14	$\Omega$
$ Y_{fs} $	transfer admittance	$I_D = 250\text{ mA}; V_{DS} = 25\text{ V}$	200	400	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$	–	55	80	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$	–	20	30	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$	–	5	10	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$I_D = 250\text{ mA}; V_{DD} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	–	5	10	ns
$t_{off}$	turn-off time	$I_D = 250\text{ mA}; V_{DD} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	–	20	30	ns



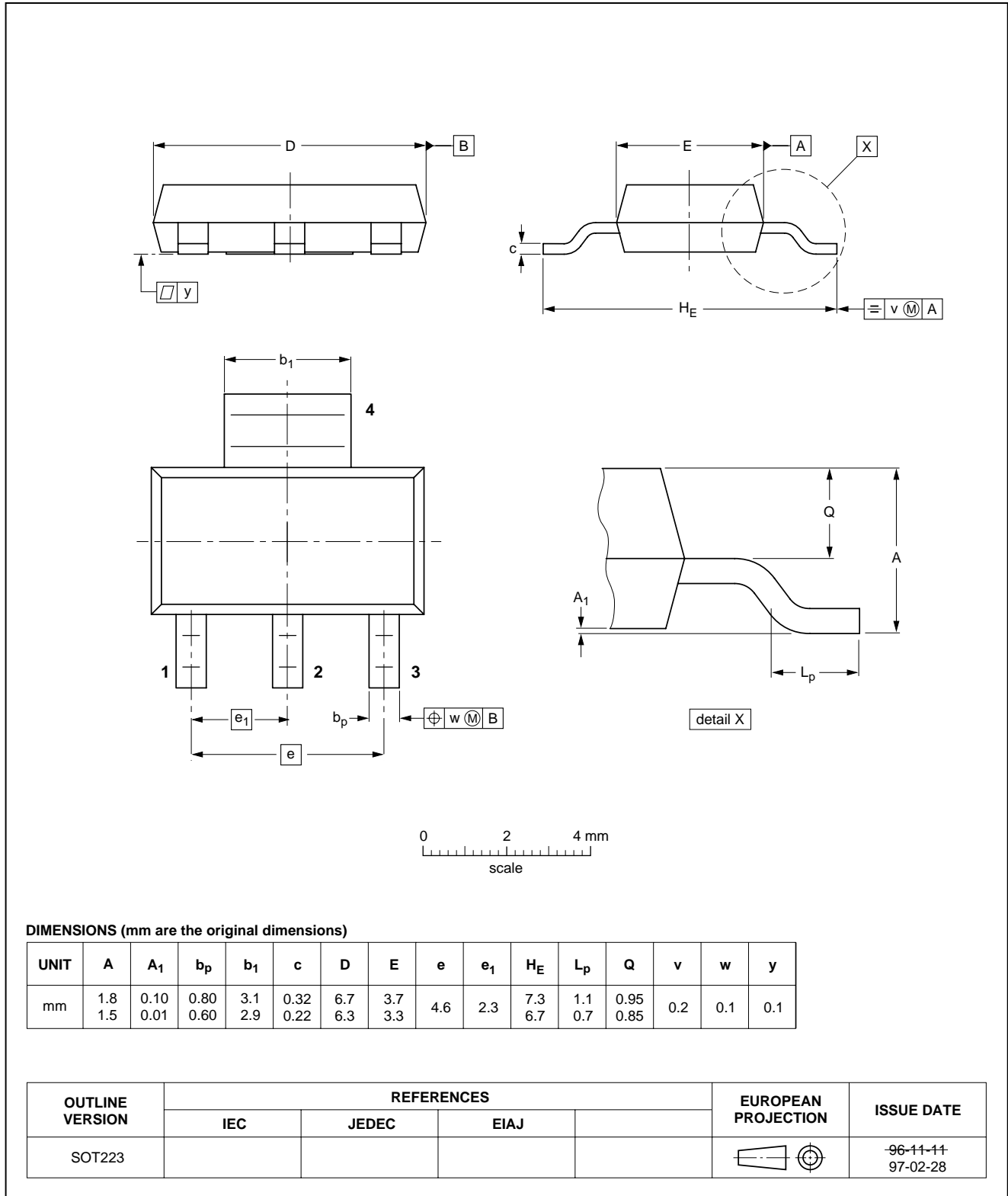
# N-channel enhancement mode vertical D-MOS transistor

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## PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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**BSP127****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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D-MOS transistor

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**NOTES**

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**NOTES**

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