Single Chip 10 Gigabit Ethernet LAN PHY

GENERAL DESCRIPTION

The S/UNI 1x10GE is a single chip 10 Gigabit Ethernet LAN PHY operating at 10.3 Gbit/s. The S/UNI 1x10GE is intended for application in 10 Gigabit Ethernet LAN PHY port cards. The S/UNI 1x10GE uses the POS-PHY Level 4™ system-side interface and the XSBI line-side interface.

FEATURES

- Implements 10 Gigabit Ethernet LAN PHY according to the IEEE P802.3ae standard currently under development.
- Provides direct connection to optics via a 16-bit by 645 MHz IEEE P802.3ae XSBI line-side interface.
- Provides SATURN® POS-PHY Level 4™ 16-bit LVDS system-side interface (clocked at 700 MHz nominal).
- Provides standard IEEE 802.3ae 10 Gigabit Ethernet Media Access Controller (10GMAC) for frame verification.
- Implements IEEE P802.3ae 64B/66B Physical Coding Sublayer (PCS).
- Internal 128 KB ingress FIFO and 16 KB egress FIFO to accommodate system latencies and provide lossless flow control up to 5 km for regular size frames.
- Line-side and system side loopback for system level diagnostic capability.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Standard 5 signal P1149.1 JTAG test port.
- Low-power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs.
- Industrial temperature range (-40 °C to +85 °C).
- 896-pin FCBGA package.

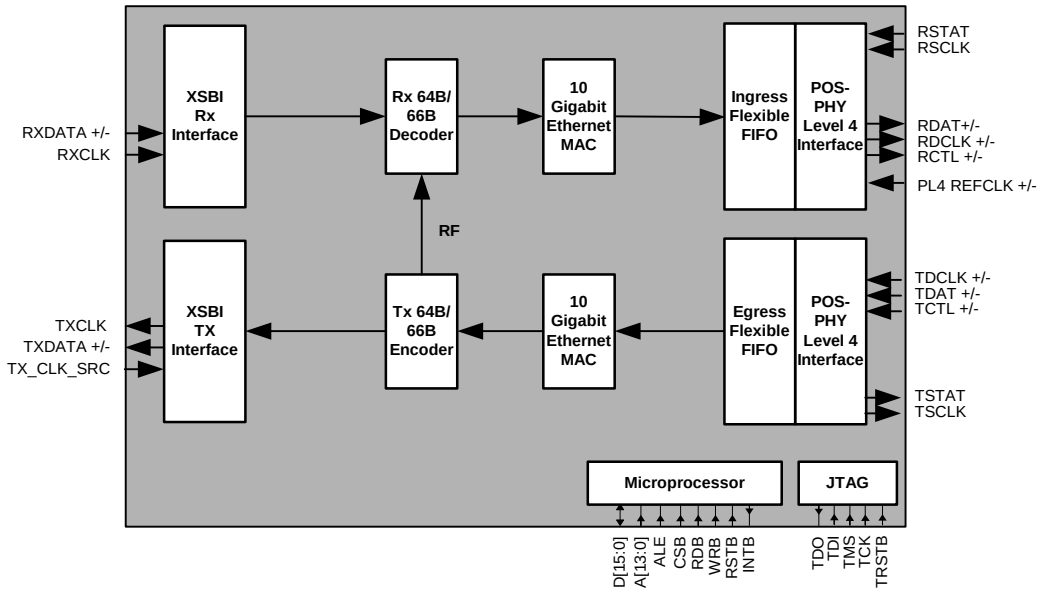
10 GIGABIT ETHERNET MAC

- Verifies frame integrity (FCS and length checks).
- Egress Ethernet frame encapsulation (pads to minimum size, add preamble, IFG and CRC generation).
- Support for VLAN tagged frames.
- Provides eight exact-match address filters to filter frames based on SA, SA/VID, DA, or DA/VID.
- Provides 64-bin hash based algorithm to filter multicast addresses.
- Minimum frame size of 64 bytes.
- Provides statistics counters to support RMON/SNMP.
- Supports jumbo frames up to 9.6 kbytes.
- Programmable inter-packet gap (IPG).
- Implements in-band PAUSE flow-control and provides support for out-of-band flow control.
- Upper layer device can flow-control using dedicated pins or host signaling to cause generation of a PAUSE frame.

DEVICE INTERWORKING

- Other PMC-Sierra devices that implement the POS-PHY Level 4™ interface include:
  - S/UNI 9953.
  - S/UNI 9953-POS.
  - S/UNI 10xGE.

BLOCK DIAGRAM



Single Chip 10 Gigabit Ethernet LAN PHY

POS-PHY LEVEL 4™ INTERFACE

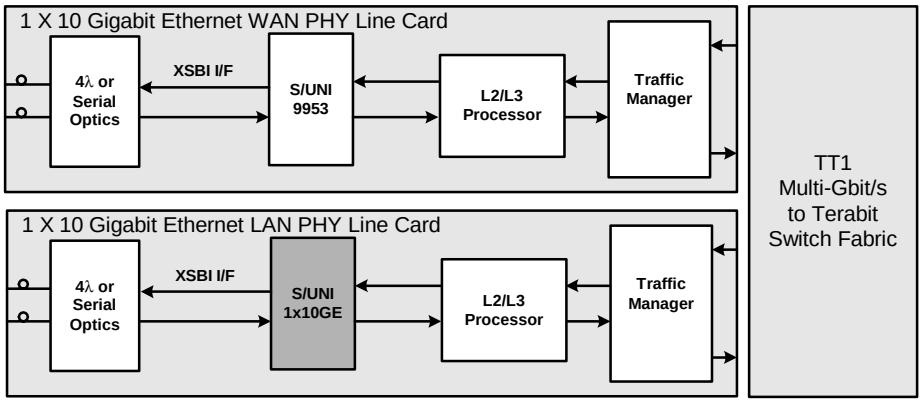
- Designed to transmit cells, packets, or frames between physical and data-link layer devices.
- Requires fewer pins and draws less power than other 10 Gigabit interface options.
- Compliant with the following standards:
  - Optical Internetworking Forum – System Physical Interface Level 4 Phase II (SPI-4 Phase II).
  - ATM Forum – Frame Based ATM Interface Level 4 (ATMF0161.00).
  - SATURN® POS-PHY™ Level 4, Issue 6, March 2001.

APPLICATIONS

- Edge and Core Routers.
- Multi-Service (Multi-Protocol) Switches.
- Internet POP and Transport POP L2 Ethernet Switches.
- Uplink cards.
- 10 Gigabit Ethernet test equipment.

TYPICAL APPLICATION

10 GIGABIT ETHERNET ROUTER PORT APPLICATIONS



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All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

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