Description

The TSEV8308500GL Evaluation Board (EB) is a prototype board which has been designed in order to facilitate the evaluation and the characterization of the TS8308500GL device (in CBGA68) up to its 1.3 GHz full analog power bandwidth at up to 500 Msps in the extended temperature range.

The high speed sampling rate of the TS8308500GL requires careful attention to circuit design and layout to achieve optimal performance. This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the TS8308500GL ADC performances over the temperature range.

The TS8308500GL Evaluation Board (EB) is very straightforward as it only implements the TS8308500GL ADC device, SMA connectors for input/output accesses and a 2.54 mm pitch connector compatible with standard high frequency probes.

The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the inputs microstrip lines, and a die junction temperature measurement setting.

The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the TS8308500GL installed and heatsink.

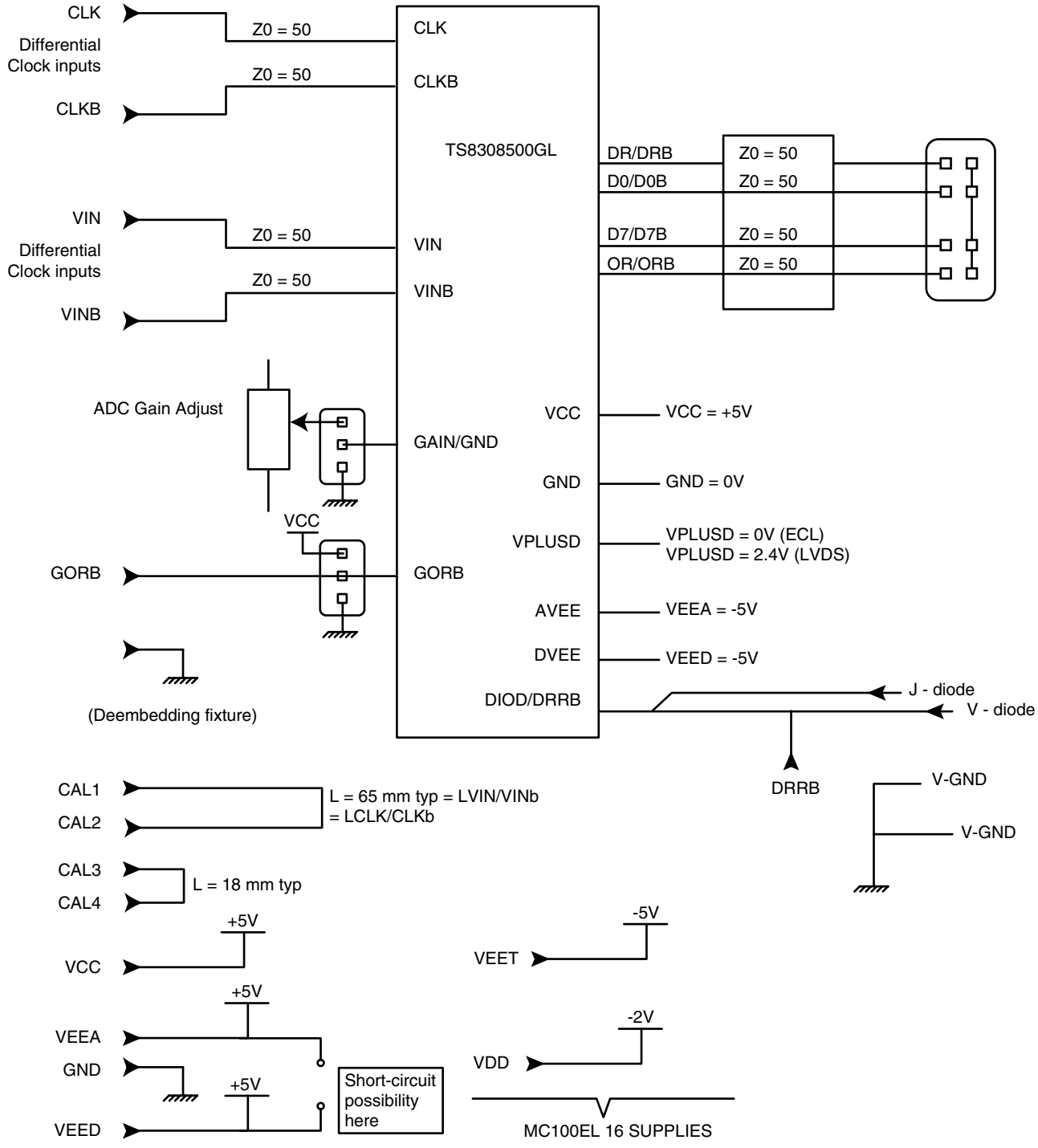
ADC 8-bit 500 Msps Evaluation Board

TSEV8308500GL

Rev. 2165A–BDC–10/02

Block Diagram

Figure 1. TSEV8308500GL Block Diagram



Detailed Description

Board Mechanical Characteristics

Board Layers Thickness Profile

The board layers number, thickness, and functions are given below, from top to bottom.

Table 1. Board Layers Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 35 µm AC signals traces = 50 Ω microstrip lines DC signals traces (GORB, GAIN, DIODE)
Layer 2 RO4003 dielectric layer (Hydrocarbon/Wovenglass)	Layer thickness = 200 µm Dielectric constant = 3.4 at 10 GHz -0.044 dB/inch insertion loss at 2.5 GHz -0.318 dB/inch insertion loss at 18 GHz
Layer 3 Copper layer	Copper thickness = 35 µm Upper ground plane = reference plane 50 Ω microstrip return
Layer 4 BT/Epoxy dielectric layer	Layer thickness = 630 mm
Layer 5 Copper layer	Copper thickness = 35 µm Lower ground plane (board mechanical rigidity)
Layer 6 BT/Epoxy dielectric layer	Layer thickness = 630 mm
Layer 7 Copper layer	Copper thickness = 35 µm Power planes = V_{EEA}, V_{EED}, V_{EET}, V_{DD}, V_{CC}, V_{PLUSD} ground plane

The TSEV8308500GL is a seven layer PCB constituted by four copper layers and three dielectric layers.

The four metal layers correspond respectively from top to bottom to the AC and DC signals layer (layer 1) (Figure 10 on page 17), two ground layers (layers 3 and 5) (Figure 11 on page 17), and one supply layer (layer 7) (Figure 12 on page 17).

The upper inner ground plane (layer 3) constitutes the reference plane for the 50Ω impedance signal traces. The lower inner ground plane (layer 5) is used for dielectric substrate rigidity and is a replica of the upper ground plane.

The backside metal layer is dedicated to the power supplies planes, surrounded by a ground plane.

The three dielectric layers are respectively (from top to bottom) constituted by a low insertion loss dielectric layer (RO4003) (layer 2) and two parallel BT/Epoxy dielectric layers (layers 4 and 6).

Considering the severe mechanical constraints due to the wide temperature range and the high frequency domain in which the board is to operate, it was necessary to use a sandwich of two different dielectric materials, with specific characteristics:

- A low insertion loss RO4003 Hydrocarbon/wovenglass dielectric layer of 200 µm thickness, chosen for its low loss (-0.318 dB/inch) and enhanced dielectric consistency in the high frequency domain. The RO4003 dielectric layer is dedicated to the routing of the 50Ω impedance signal traces. (The RO4003 typical dielectric constant is 3.4 at 10 GHz). The RO4003 dielectric layer characteristics are very close to PTFE in terms of insertion loss characteristics.
- A BT/Epoxy dielectric layer of 1.2 mm total thickness which is sandwiched between the upper ground plane and the back-side supply layer.

The BT/Epoxy layer has been chosen because of its enhanced mechanical characteristics for elevated temperature operation. The typical dielectric constant is 4.5 at 1 MHz.

More precisely, the BT/Epoxy dielectric layer offers enhanced characteristics compared to FR4 Epoxy, namely:

- higher operating temperature value: 170°C (125°C for FR4),
- better withstanding of thermal shocks (-65°C up to 170°C).

Reference: VITELEC 142 0701 851.

The total board thickness is 1.6 mm.

The previously described mechanical and frequency characteristics makes the board particularly suitable for the device evaluation and characterization in the high frequency domain and in the military temperature range.

Analog Input, Clock Input, De-embedding Fixture Accesses

The Analog, Clock and De-embedding fixture differential active inputs are provided by SMA connectors.

Digital Outputs Accesses

Access to the differential output data port is provided by a 2.54 mm pitch connector, compatible with standard Digital Acquisition System. It enables access to the converter output data, as well as proper 50Ω differential termination.

Power Supplies and Ground Accesses

The power supplies accesses are provided by five 4 mm section banana jacks respectively for V_{EEA}, V_{EED}, V_{EET}, V_{DD}, V_{PLUSD} and V_{CC}.

The Ground accesses are provided by 4 mm and two 2 mm banana jacks.

ADC Functions Settings Accesses

For ADC functions settings accesses (GORB, Die junction temp., ADC Gain adjust), smaller 2 mm section banana jacks are provided. A potentiometer is provided for ADC gain adjust.

Layout Information

Board

The TS8308500GL requires proper board layout for optimum full speed operation.

The following information explains the board layout recommendations and demonstrate how the Evaluation Board fulfills these implementation constraints.

A single low impedance ground plane is recommended, since it allows laying out signal traces and power planes without interrupting the ground plane.

Therefore a multi-layer board structure has been retained for the TSEV8308500GL.

Four copper metal layers are used, dedicated respectively (from top to bottom) to the signal traces, ground planes and power supplies.

The input/output signals traces occupy the top metal layer.

The ground planes occupy the second and third copper metal layers.

The bottom metal layer is dedicated to the power supplies.

AC Inputs/Digital Outputs

The board uses 50Ω impedance microstrip lines for the differential analog inputs, clock inputs, and differential digital outputs, (including the Out of Range Bit and the data ready output signal).

The input signals and clock signals must be routed on one layer only, without using any through-hole vias. The line lengths are matched to within 2 mm.

The analog and clock input lines are properly reverse terminated by 50Ω surface mount chip resistors placed very close to the ADC device.

The digital output lines are 50Ω differentially terminated.

The output data trace lengths are matched to within 0.25 inch (6 mm) to minimize the data output delay skew.

For the TSEV8308500GL the propagation delay is approximately 6.1 ps/mm (155 ps/inch).

(The RO4003 typical dielectric constant is 3.4 at 10 GHz).

For more information about different output termination options refer to the specification application notes.

DC Function Settings (GORB, Gain, Die Junction Temperature Measurement)

The DC signals traces are low impedance. They have been routed with 50 Ω impedance near the device because of room restriction.

Power Supplies

The bottom metal layer 7 is dedicated to the power supply traces (V_{EEA}, V_{EED}, V_{EET}, V_{CC}, V_{DD}, V_{PLUSD}) (See Figure 12 on page 17).

The supply traces are approximately 6 mm wide in order to present low impedance, and are surrounded by a ground plane connected to the two inner ground planes.

The Analog and Digital negative power supply traces are independent, but the possibility exists to short-circuit both supplies on the top metal layer (See Figure 10 on page 17).

No difference in ADC high speed performance is observed when connecting both negative supply planes together. Obviously one single negative supply plane could be used for the circuit.

Each power supply incoming is bypassed by a 10 µF Tantalum capacitor in parallel with 10 nF chip capacitor.

Each power supply access is decoupled very close to the device by a 10 nF and 100 pF surface mount chip capacitors in parallel.

Note: The decoupling capacitors are superposed. In this configuration, the 100 pF capacitors must be mounted first.

TS8308500GL on Board Implementation

Surface-mount resistors and chip capacitors allow the closest possible connections to the device pins, for microstrip line back termination and bypassing.

- Connecting the positive supply pads:
  - The positive supply pads denoted V_{CC}:

  The corresponding V_{CC} pad numbers are A4, A6, B2, B4, B6, H1, H2, L6, L7.

  Each V_{CC} power supply pad is decoupled as closely to the device as possible by a 10 nF and 100 pF chip capacitor.

  The V_{CC} supply pads are connected to the back side V_{CC} plane of the CEB.

  - The positive digital supply pads are denoted V_{PLUSD} (0V or 2.4V).

  The corresponding V_{PLUSD} pad numbers are B11, C10, J10, K11.

  Each V_{PLUSD} power supply pad is decoupled very close to the device by a 10 nF and 100 pF chip capacitor.

  The V_{PLUSD} supply pads are connected to the back side V_{PLUSD} plane of the evaluation board.

- Connecting the negative supply pads:
  - The TS8308500GL has separate analog and digital -5V supplies:

  The negative analog supply pads are denoted V_{EE}.

  The V_{EE} corresponding pad numbers are A3, B3, G1, G2, J1, J2.

  The negative digital supply pad is denoted DV_{EE}.

  The DV_{EE} corresponding pad numbers are F10, F11.

  The DV_{EE} supply pad is dedicated to the digital output buffers only.

  Each V_{EE} and DV_{EE} power supply pad is decoupled as closely as possible near the device by a 10 nF and 100 pF chip capacitor.

  - The V_{EE} and DV_{EE} supply pads are respectively connected to the backside layer 7 V_{EE} and V_{EED} supply planes.

- Ground pad connections:
  - The analog ground pads are denoted GND. The corresponding GND pad numbers are A2, A5, B1, B5, B10, C2, D2, E1, E2, E11, F1, F2, G11, K2, K3, K4, K5, K10, L2, L5.

Thermal Characteristics

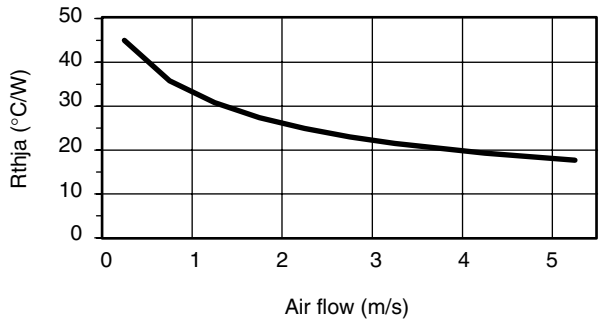
Thermal Resistance from Junction to Ambient: Rthja

The following table lists the converter thermal performance parameters of the device itself, with no external heatsink added.

Table 2. Thermal Resitance

Air Flow (m/s)	Estimated ja Thermal Resistance (°C/W)
0	45
0.5	35.8
1	30.8
1.5	27.4
2	24.9
2.5	23
3	21.5
4	19.3
5	17.7

Figure 2. Thermal Resistance from Junction to Ambient: Rthja



Thermal Resistance from Junction to Case: Rthjc

Typical value for Rthjc is given to 6.7°C/W (8°C/W max).

This value does not include thermal contact resistance between package and external component (heatsink or PCBoard).

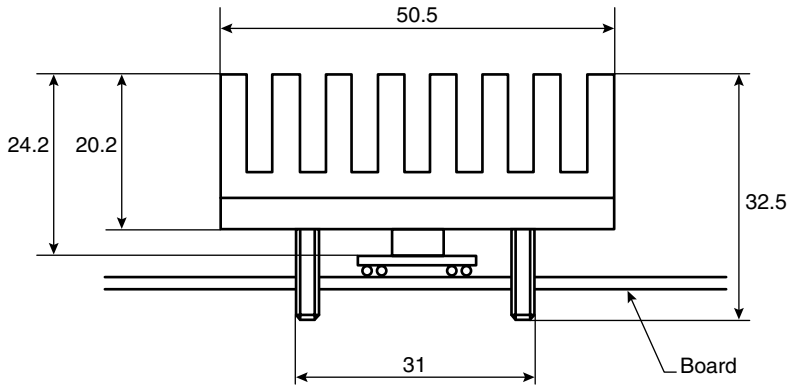
As an example, 2.0°C/W can be taken for 50 µm of thermal grease.

CBGA68 Board Assembly with External Heasink

It is recommended to use an external heatsink or PCBoard special design.

Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

Figure 3. CBGA68 Board Assembly



Note: Units in mm.

Application Information

For this section, refer also to the product Specification application notes (TS8308500 Datasheet). More particularly, refer to sections related to single-ended and differential input configurations.

Analog Inputs

The analog inputs can be entered in differential or Single-ended mode without any high speed performance degradation.

The board digitizes Single-ended signals by choosing either input and leaving the other input open, as the latter is on-board 50Ω terminated. Nominal In-phase inputs is V_{IN} (See “Operating Procedure, Quick Start, Recommandations of Use” on page 12.).

Clock Inputs

The clock inputs can be entered in differential or Single-ended mode without any high speed performance degradation. Moreover, the clock input common mode may be 0V, or -1.3V if ECL input format is used for the clock inputs.

As for the analog input, either clock input can be chosen, leaving the other input open, as both clock inputs are on-board 50Ω terminated. Nominal in-phase clock input is CLK (See “Operating Procedure, Quick Start, Recommandations of Use” on page 12.).

Setting the Digital Output Data Format

For this section, refer to the Evaluation Board Electrical schematic and to components placement document (respectively Figure 7 on page 15).

Refer also to the TS8308500 specification pages about digital output coding.

The TS8308500 delivers data in natural binary code or in Gray code. If the “GORB” input is left floating or tied to V_{CC} the data format selected will be natural binary, if this input is tied to ground the data will follow Gray code.

Use the jumper denoted ST2 for selecting the output data port format:

- If ST2 is left floating or tied to V_{CC}, the data output format is true Binary,
- If ST2 is tied to GND, the data outputs are in Gray format.

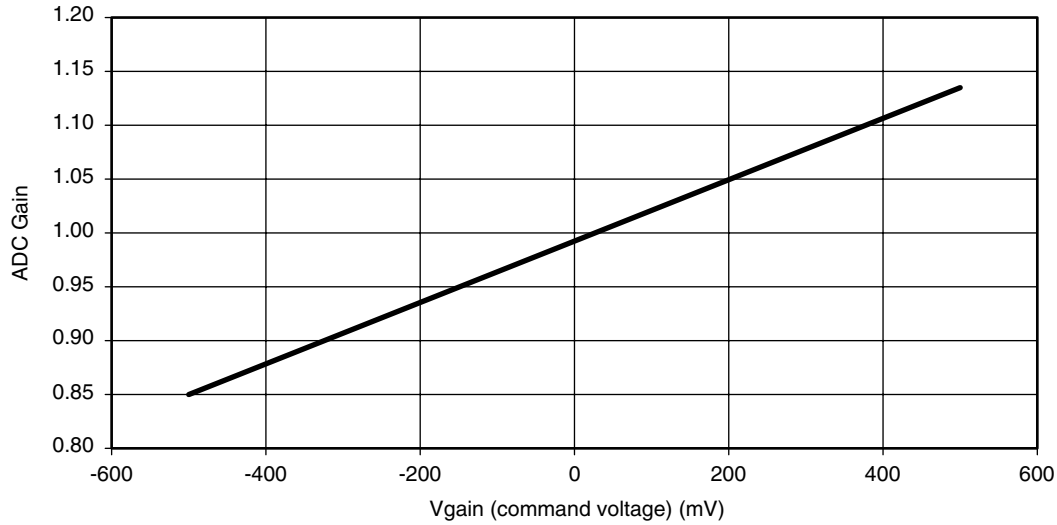
The V_{PLUSD} positive supply voltage allows the adjustment of the output common mode level from -1.2V (V_{PLUSD} = 0V for ECL output compatibility) to +1.2V (V_{PLUSD} = 2.4V for LVDS output compatibility).

Each output voltage varies between -1.02V and -1.35V (respectively +1.38V and +1.05V), leading to ±0.33V = 660 mV in differential, around -1.8V (respectively +1.21V) common mode for V_{PLUSD} = 0V (respectively 2.4V).

ADC Gain Adjust

The ADC gain is adjustable by the means of the pin (K6) (pad input impedance is 1 MΩ in parallel with 2 pF). A jumper denoted ST1 has been foreseen in order to have access to the ADC gain adjust pin. The P1 potentiometer is dedicated for adjusting the ADC Gain from approximately 0.85 up to 1.15. The gain adjust transfer function is given below.

Figure 4. ADC Gain Adjust



SMA Connectors and Microstrip Lines De-embedding Fixture

Attenuation in microstrip lines can be found by taking the difference in the log magnitudes of the S21 scattering parameters measured on two different lengths of meandering transmission lines. Such a difference measurement also removes common losses such as those due to transitions and connectors.

The scattering parameter S21 corresponds to the amount of power transmitted through a two-port network. The characteristic impedance of the microstrip meander lines must be close to 50Ω to minimize impedance mismatch with the 50Ω network analyzer test ports.

Impedance mismatch will cause ripple in the S21 parameter as a function of both the degree of mismatch and the length of the line.

Temperature Monitoring and Data Ready Reset Function

One single pad is used for both the DRRB input command and die junction monitoring. The pad denomination is DRRB/DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

TS8308500GL ADC Die Junction Temperature Measurement Setup

For operation in the extended temperature range, forced convection is required, to maintain the device junction temperature below the specified maximum value (Tj max = 125°C).

A die junction temperature measurement setting has been included on the board, for junction temperature monitoring.

Four 2 mm section banana jacks (J9, J10, J11, J12) are provided to force current and measure the VBE voltage across the dedicated transistor connected between pad (PIN K1 and GND).

The measurement method consists in forcing a 3 mA current flowing into a diode mounted transistor, connected between pad K1 and GND (pad K1 is the emitter and GND is the shorted base-collector).

CAUTION:

Respect the current source polarity. In any case, make sure the maximum voltage compliance of the current source is limited to maximum 1V or use resistor mounted in serial with the current source to avoid damage to the transistor device. This may occur for instance if current source is reverse connected.

The measurement setup is described in Figure 5. The diode VBE forward voltage versus junction temperature (in steady state conditions) is given in Figure 6.

Figure 5. TS8308500GL Die Junction Temperature Measurement Setup

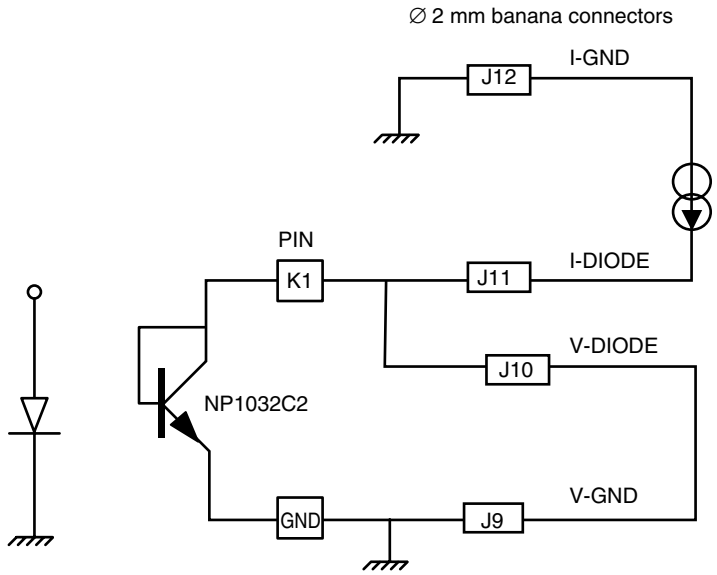
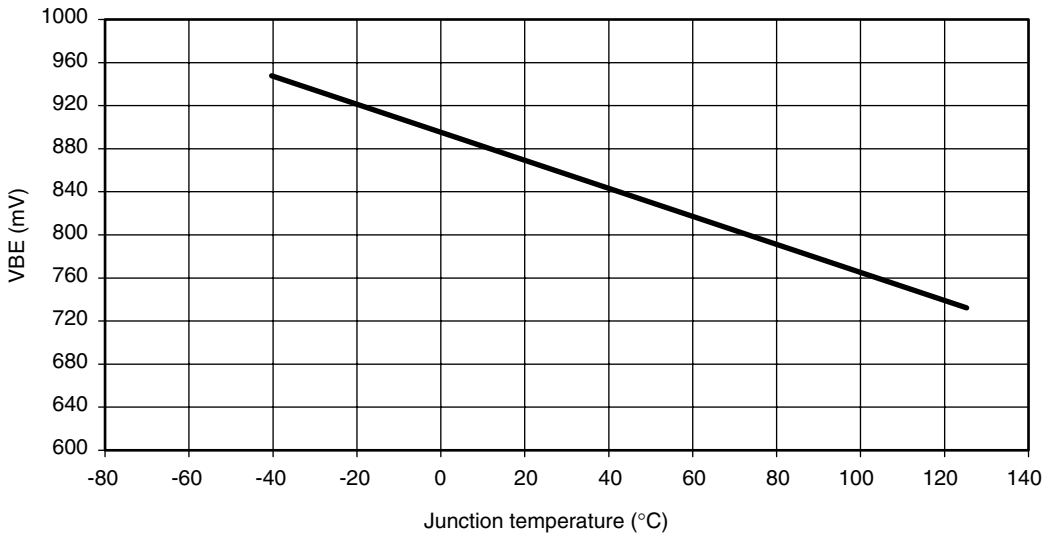


Figure 6. Transistor VBE Forward Voltage Versus Junction Temperature (I=3 mA)



Data Ready Output Signal Reset

A subvis connector is provided for DRRB command.

The Data ready signal is reset on falling edge of DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to V_{EE} = -5V for Data Ready output signal master Reset. So long DRRB remains at logical low level, (or tied to V_{EE} = -5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typical.

TRDR is measured between the -1.3V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data ready Reset command may be a pulse of 1 ns minimum time width.

The Data ready output signal restarts on DRRB command rising edge, ECL logical high levels (-0.8V).

DRRB may also be grounded, or is allowed to float, for normal free running Data ready output signal.

Electrical Operating Characteristics

The power supplies denoted V_{CC}, V_{EEA}, V_{EED} and V_{PLUSD} are dedicated for the TS8308500GL ADC.

The power supplies denoted V_{EET}, V_{DD} are dedicated to the optional MC100EL16 asynchronous differential receivers.

Table 3. Electrical Specifications

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Positive supply voltage (dedicated to TS8308500GL ADC only)	V_{CC}	4.75	5	5.25	V
	V_{PLUSD}	LVDS: 1.4	ECL: 0 LVDS: 2.4	LVDS: 2.6	V V
	V_{EEA}	-5.25	-5	-4.75	V
	V_{EED}	-5.25	-5	-4.75	V
Positive supply current (dedicated to TS8308500GL ADC only)	I_{CC}	–	400	425	mA
	I_{PLUSD}	–	120	130	mA
	I_{EEA}	–	170	185	mA
	I_{EED}	–	140	160	mA
Positive supply voltage not used by default – If installed (dedicated to MC100EL16 differential Receivers)	V_{EET}	-5.25	-5	-4.75	V
	V_{DD}	-2.15	-2	-185	V
Positive supply current not used by default – If installed (dedicated to MC100EL16 differential Receivers)	I_{EET}	–	150	–	mA
	I_{DD}	–	390	–	mA
Nominal power dissipation (without receivers)	PD	–	3.8	3.9 (Tj = 125°C)	W

Table 3. Electrical Specifications (Continued)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Analog input impedance	Z_{IN}	–	50	–	Ω
Full Power Analog Input Bandwidth (-3 dB)	–	1.3	1.3	–	GHz
Analog Input Voltage range (differential mode)	V_{IN}	-125	–	125	V
Clock input impedance	–	–	50	–	Ω
Clock inputs voltage compatibility (Single-ended or differential) (See Application Notes)	–	ECL levels or 4 dBm (typ.) into 50Ω			–
Clock input power level into 50Ω termination resistor	–	-2	4	10	dBm

Operating Procedure, Quick Start, Recommandations of Use

Introduction

This section describes a typical Single-ended configuration for analog inputs and clock inputs.

The single-ended configuration is preferable, as it corresponds to the most straightforward and quickest TSEV8308500GL board setting for evaluating the TS8308500GL at full speed in its temperature range.

The inverted analog input V_{INB} and clock input CLKB common mode level is Ground (on-board 50Ω terminated).

In this configuration, no balun transformer is needed to convert properly Single-ended mixer output to balanced differential signals for the analog inputs.

In the same way, no balun is necessary to feed the TS8308500GL clock inputs with balanced signals.

Connect the RF sources directly to the in-phase analog and clock inputs of the converter.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

Operating Procedure

1. Connect the power supplies and Ground accesses

   (V_{CC} = +5V, GND = 0V, V_{PLUSD} = 0V, V_{EEA} = V_{EED} = -5V) through the dedicated banana jacks.

   The -5V power supplies should be turned on first.

   Note: One single -5V power supply can be used for supplying the digital V_{EED} and analog V_{EEA} power planes.

2. The board is set by default for digital outputs in binary format.

3. Connect the CLK clock signal.

   The inverted phase clock input CLKB may be left open (as on board 50Ω terminated).

   Use a low phase noise RF source.

   The clock input level is typically 4 dBm and should not exceed +10 dBm into the 50Ω termination resistor (maximum ratings for clock input power level is 15 dBm).

   Clock frequency can range between 10 MHz and 700 MHz.

4. Connect the analog signal V_{IN}.

   The inverted phase clock input V_{INB} may be left open (as on board 50Ω terminated).

   Use a low phase noise RF source.

   Full Scale range is 0.5V peak to peak around 0V, (±250 mV), or -2 dBm into 50Ω.

   Input frequency can range from DC up to 1.3 GHz.

   At 1.3 GHz (TBC), the ADC attenuates by -3 dB the input signal. The board insertion loss (S21) will be furnished in definitive document release.

5. Connect the high speed data acquisition system probes to the output connector.

   The connector pitch (2.54 mm) is compatible with High Speed Digital Acquisition System probes.

   The digital data are on-board differentially terminated.

   However, the output data can be picked up either in single-ended or differentially mode.

6. Board functionality verification and proposed product evaluation procedure:
   - A first test can be run at 500 Msps/250 MHz Nyquist: about 7.1 Effective Bits (typ) should be obtained.
   - At 500 Msps/20 MHz: about 7.2 Effective Bits (typ) should be obtained.
   - At 500 Msps/500 MHz and -1 dB Full Scale analog input, 7.0 bits and -52 dBc SFDR should be obtained.

7. The devices operate respectively from 10 Msps up to 500 Msps in binary output format and 10 Msps up to 500 Msps in Gray output format. It is capable of sampling analog input waveforms ranging from DC up to 1.3 GHz.

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE} (2)		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND -0.3 to 2.8	V
Negative supply voltage	V_{EE} (2)		GND to -6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1 to +1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-2 to +2	V
Digital input voltage	V_D	GORB	-0.3 to V_{CC} +0.3	V
Digital input voltage	V_D	DRRB	V_{EE} -0.3 to +0.9	V
Digital output voltage	V_O		V_{PLUSD} -3 to V_{PLUSD} -0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		-3 to +1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-2 to +2	V
Maximum junction temperature	T_j		+145	°C
Storage temperature	T_{stg}		-65 to +150	°C
Lead temperature (soldering 10s)	T_{leads}		+300	°C

Notes: 1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. The use of a thermal heat sink is mandatory.

2. In case only one supply is used for supplying the -5V negative power planes, apply the DV_{EE} absolute maximum ratings.

TSEV8308500GL
Electrical Schematic

Figure 7. TSEV8308500GL Electrical Schematic

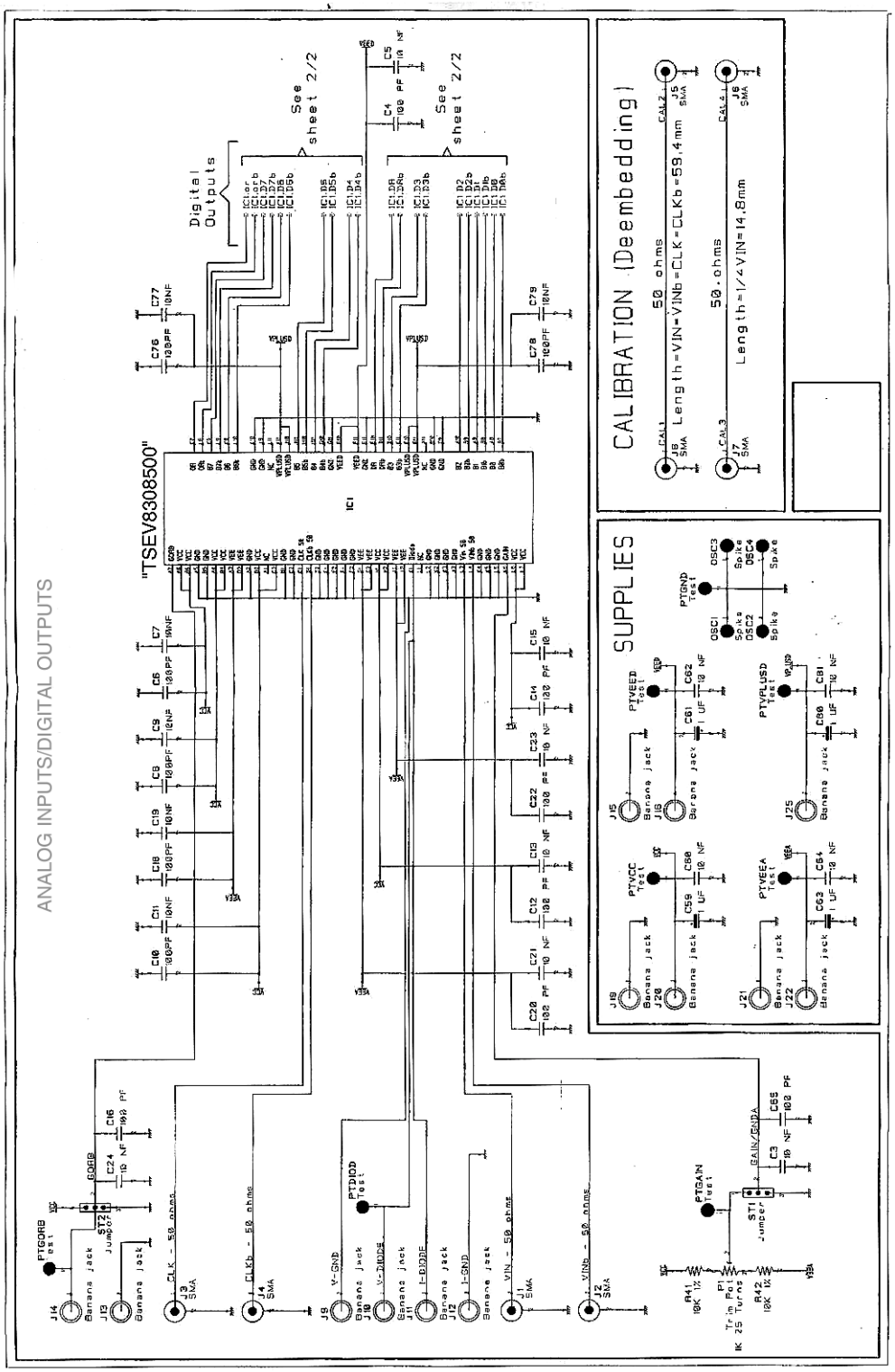


Figure 8. Board Digital Outputs Default Option

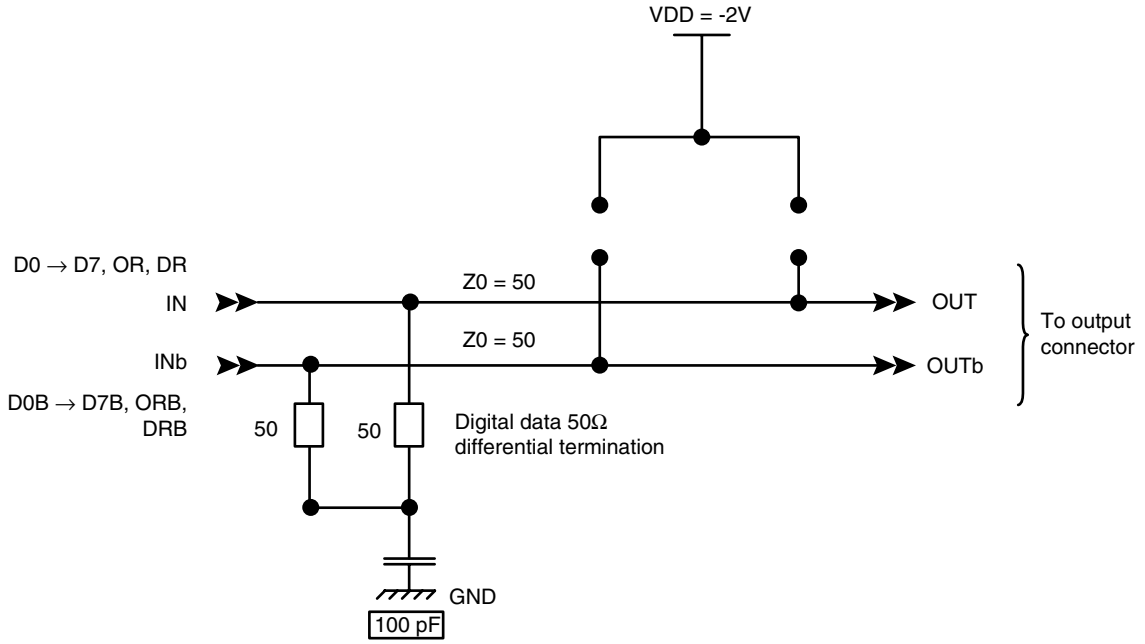


Figure 9. Board Digital Outputs Option Using MC100EL16 Differential Receivers

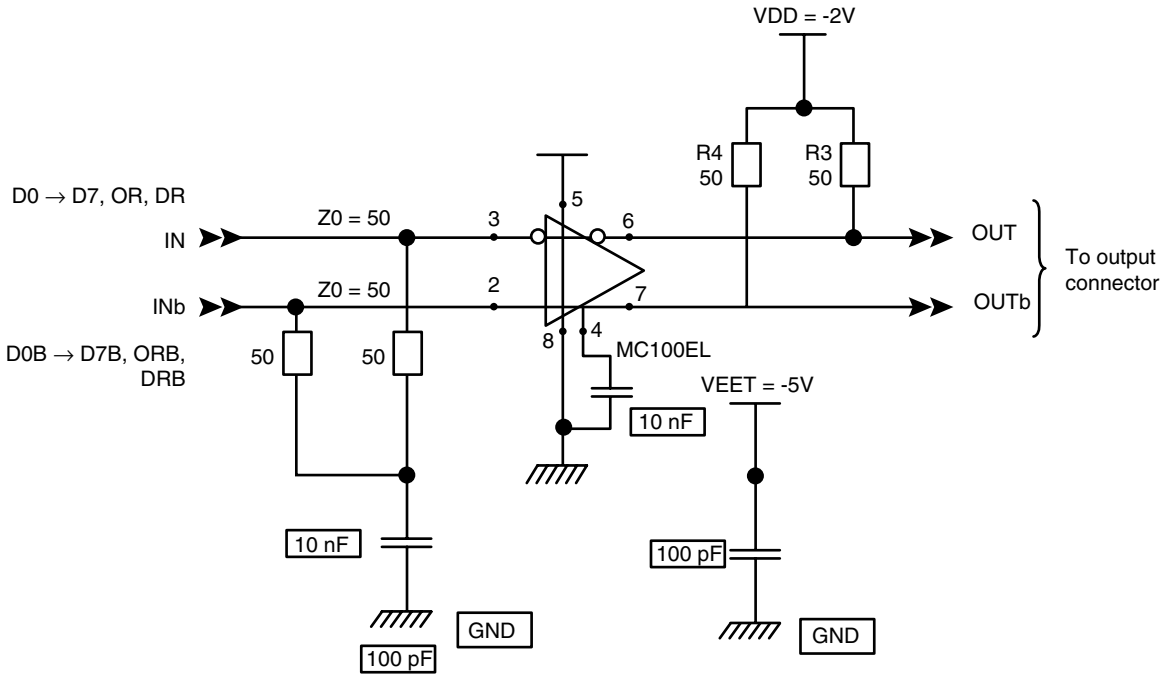


Figure 10. Component Side Description

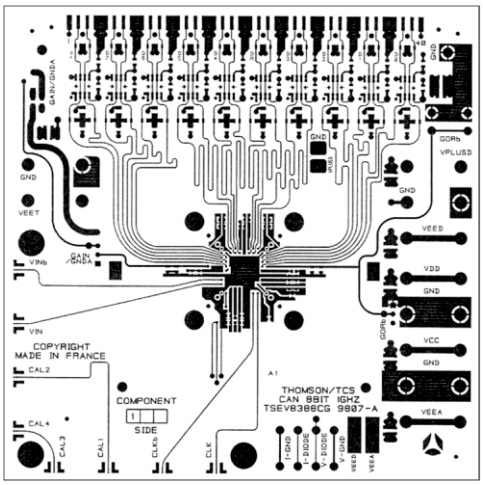


Figure 11. Ground Plane

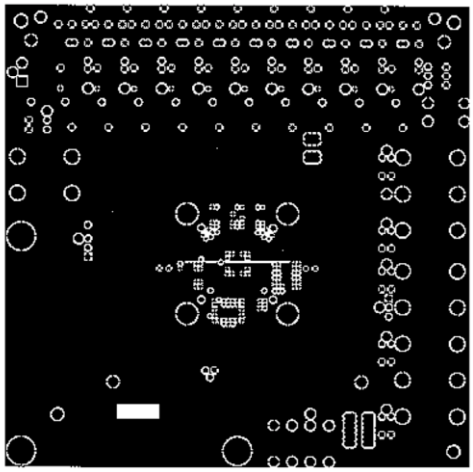


Figure 12. Power Supplies Planes

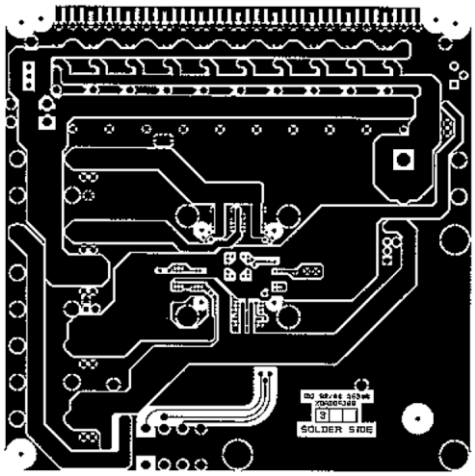
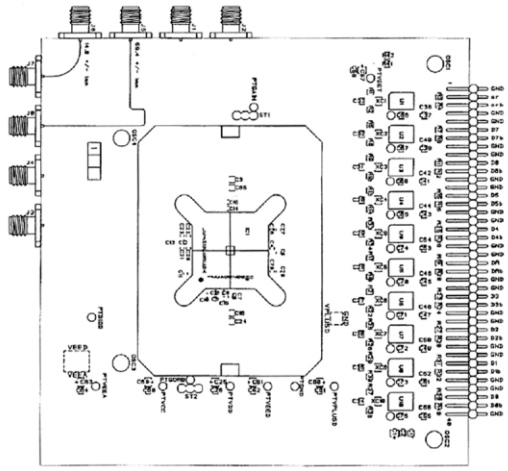


Figure 13. TSEV8308500GL Evaluation Board: Components Placement



Test Bench Description

Figure 14. Differential Analog and Clock Inputs Configuration

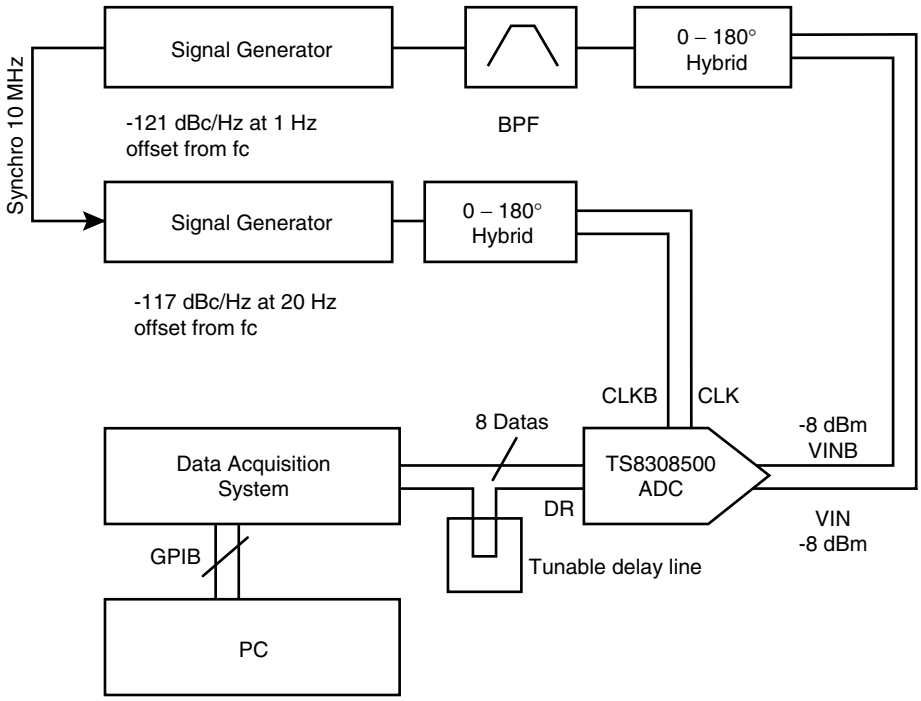
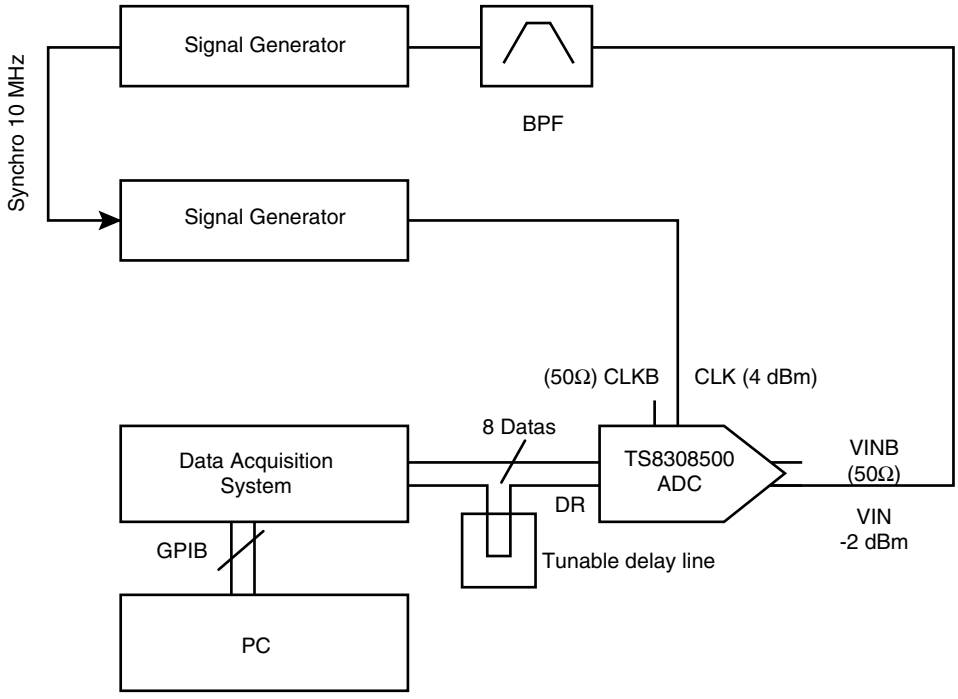
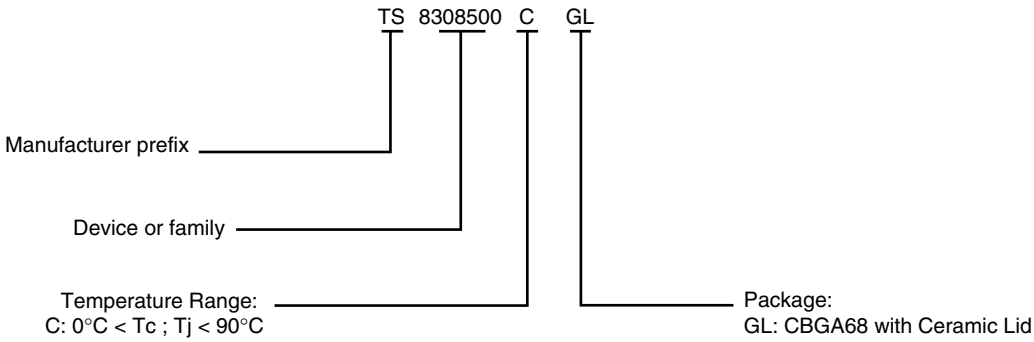


Figure 15. Single-ended Analog and Clock Input Configuration

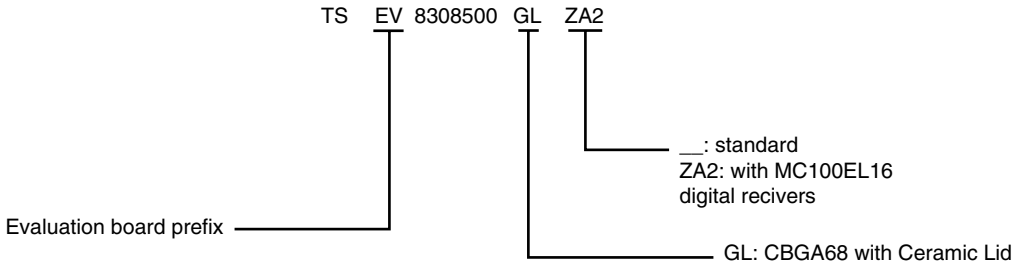


Ordering Information

Package Device



Evaluation Board



The evaluation board is delivered with an ADC and includes the heat sink.

Package Description

Package Pin Description

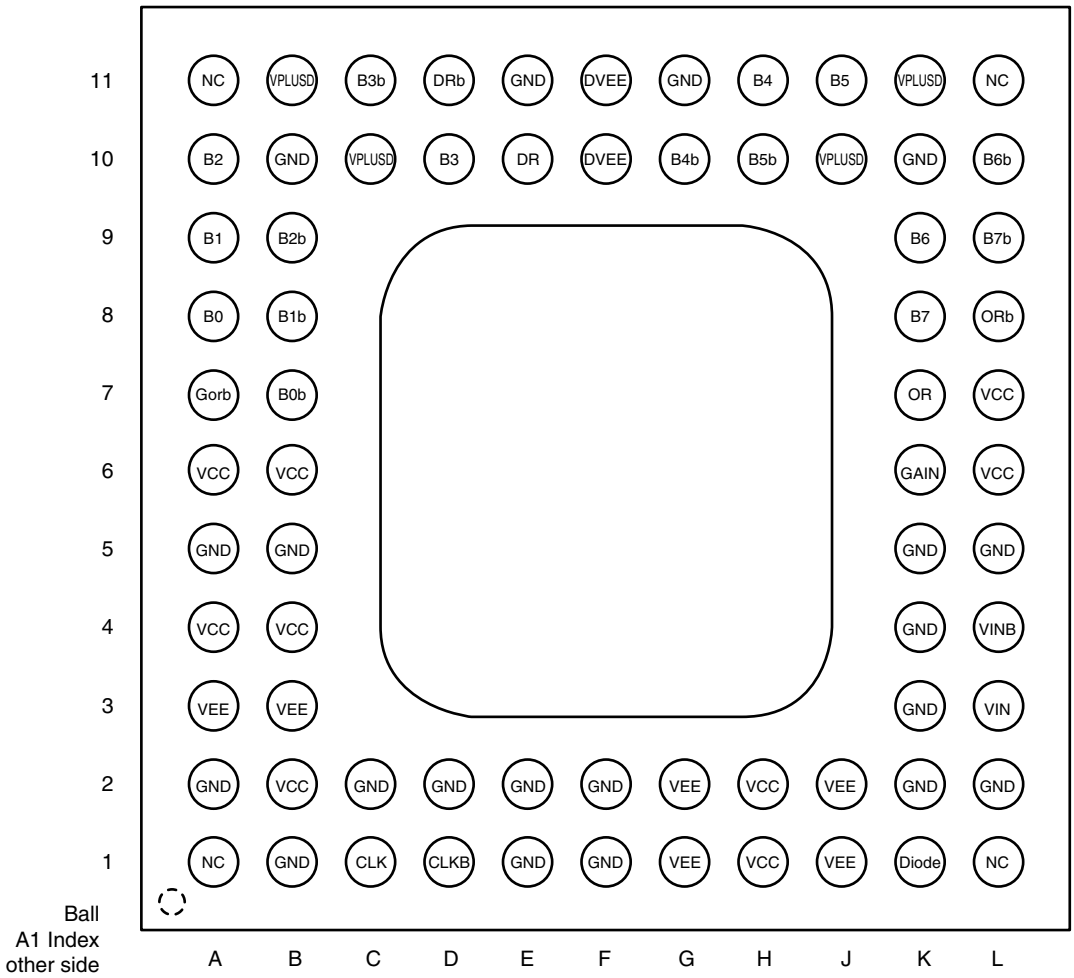
Table 5. TSEV8308500GL Pin Description

Symbol	Pin Number	Function
GND	A2, A5, B1, B5, B10, C2, D2, E1, E2, E11, F1, F2, G11, K2, K3, K4, K5, K10, L2, L5	Ground pins. To be connected to external ground plane.
V_{CC}	A4, A6, B2, B4, B6, H1, H2, L6, L7	+5V positive supply.
V_{EE}	A3, B3, G1, G2, J1, J2	5V analog negative supply.
DV_{EE}	F10, F11	-5V digital negative supply.
V_{IN}(1)	L3	In phase (+) analog input signal of the sample and Hold differential preamplifier.
V_{INB}(1)	L4	Inverted phase (-) of ECL clock input signal (CLK).
CLK	C1	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	D1	Inverted phase (-) of ECL clock input signal (CLK).
B0, B1, B2, B3, B4, B5, B6, B7	A8, A9, A10, D10, H11, J11, K9, K8	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.
B0B, B1B, B2B, B3B, B4B, B5B, B6B, B7B	B7, B8, B9, C11, G10, H10, L10, L9	Inverted phase (-) Digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	K7	In phase (+) Out of Range Bit. Out of Range is high on the leading edge of code 0 and code 256.
ORB	L8	Inverted phase (+) of Out of Range Bit (OR).
DR	E10	In phase (+) output of Data Ready Signal.
DRB	D11	Inverted phase (-) output of Data Ready Signal (DR).
GORB	A7	Gray or Binary select output format control pin. - Binary output format if GORB is floating or V_{CC}. - Gray output format if GORB is connected at ground (0V).
GAIN	K6	ADC gain adjust pin. The gain pin is by default grounded, the ADC gain transfer function is nominally close to one.
DIOD/DRRB	K1	Die function temperature measurement pin and asynchronous data ready reset active low, single ended ECL input.
V_{PLUSD}	B11, C10, J10, K11	+2.4V for LVDS output levels otherwise to GND(1)
NC	A1, A11, L1, L11	Not connected.

Note: 1. The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

TS8308500GL
Pinout

Figure 16. TS8308500GL Pinout of CBGA68 Package



Datasheet Status Description

Table 6. Datasheet Status

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later; could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet contains also characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specification.	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

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